GE Vingmed Ultrasound

Service Manual - Rev. I

– Online –

System FiVe
Sw.: Up to v.1.9.x

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The SYSTEM FIVE Service Manual

Main Overview

Introduction

This page lists the main topics covered by the SYSTEM FIVE Service Manual.

Topics described in this manual

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GE Vingmed Ultrasound

Service Manual

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Up to v.1.9.x**.**

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SYSTEM FIVE

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COMPANY DATA:	
GE Vingmed Ultrasound A/S , P. O. Box 141, N-3191 Horten, Norway	Telephone: (+47) 3302 1100 Telefax: (+47) 3302 1350 Telex: 70405 sound n Internet email: *NORWAYSERV@euromsx.gemse.fr*

Introduction - rev. 11

1 Warnings and Cautions

The following safety precautions must be observed during all phases of operation, service and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture and intended use of the equipment.

1.1 Authorization

Operating personnel must not remove the system covers. Servicing should be performed by authorized personnel only. Only personnel who have participated in a System FiVe Training Seminar are authorized to service the equipment.

1.2 Electric Shock Hazard

To minimize shock hazard, the equipment chassis must be connected to an electrical ground. The system is equipped with a three-conductor AC power cable. This must be plugged into an approved electrical outlet with safety ground. If an extension cord is used with the system, make sure that the total current rating of the system does not exceed the extension cord rating.

The power outlet used for this equipment should not be shared with other types of equipment.

Both the system power cable and the power connector meet international electrical standards.

1.3 Dangerous Procedure Warnings

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing and adjusting.

1.4 Explosion Warning

Do not operate the equipment in an explosive atmosphere. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

1.5 Electrostatic Discharge Warning

Do not touch any boards with integrated circuits prior to taking the necessary ESD precautions:

1. Always connect yourself, via an arm-wrist strap, to the advised ESD connection point located on the card rack.
2. Follow general guidelines for handling of electrostatic sensitive equipment.

1.6 Do not substitute parts or modify equipment

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment.

Regulatory Information

The GE Vingmed Ultrasound product families are tested to meet all applicable requirements in relevant EU Directives and European/International standards. (See “Standards used” below.) Any changes to accessories, peripheral units or any other part of the system must be approved by the manufacturer; GE Vingmed Ultrasound. **Ignoring this advice may compromise the regulatory approvals obtained for the product.**

Please consult your local GE Vingmed Ultrasound representative for further details.

Standards used

Our ultrasound scanners are class I devices, according to Clause 14 of IEC 60601-1 (1988).

To fulfill the requirements of relevant EC directives and/or European Harmonized/International standards, the following documents/standards have been used:

STANDARD/DIRECTIVE	SCOPE
93/42/EEC	Medical Devices Directive (MDD)
IEC 801-2/ 4.1991	Electrostatic Discharge
IEC 801-3/ 1984	Radiated Electromagnetic Field
IEC 801-4/ 1988	Electrical Fast Transient/Burst
IEC 801-5/ 1.1993(draft)	Surge
EN 55011/CISPR 11/ 3.1991	Emitted noise according to Class B requirements + Electromagnetic Susceptibility
IEC 60601-1 (1988) EN 60601-1/ 1990 UL2601-1/ 8.1994	Medical Electrical Equipment, Part 1; General Requirements for Safety “CLASSIFIED BY UNDERWRITERS LABORATARIES INC WITH RESPECT TO ELECTRICAL SHOCK, FIRE AND MECHANICAL HAZARDS ONLY IN ACCORDANCE WITH UL2601-1 AND CAN/CSA C22.2 NO.601.1”
IEC 1157/ EN 61157/ 1994	Requirements for the declaration of the acoustic output of medical diagnostic ultrasonic equipment.
IEC EN 60601-1-2 /1993	Medical Electrical Equipment - part 2. Collateral standard: Electromagnetic compatibility - Requirements and tests.

NOTE:
1) Any rest energy within our scanners or their components will be below 60V DC or 2 mJ.
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CE 0301

2 About This Manual

2.1 Abstract

The purpose of this manual is to provide information which will enable the technician to diagnose and repair most problems encountered in the use of System FiVe. It is not a guide to operation. Information pertaining to this is found in the System FiVe User Manual.

The manual is not intended to be used for troubleshooting on board level. This will be done on the factory. Some of the modules in the System FiVe are older designs, thus occasionally signal names on the module might not be the same on another module, even though the signal is the same. This is done to ease troubleshooting on board level at the factory.

2.2 Overview

The service manual is divided into several main chapters:

- The Theory of Operation chapter consists of two major sections; a Principles of Operation section which gives a lesson in the basics of ultrasound, and a System (and subsystem) Description section detailing how the system works, down to board level.
- The Block Schematics chapter contains all block schematics for the system, the boards and other assemblies. They are all referenced in the Descriptions section of the Theory of Operation chapter.
- The Cables chapter contains drawings and signal lists of cables within the system.
- The Mechanical Subassemblies chapter gives exploded view drawings.
- The Probes chapter includes a listing of all System FiVe probes; types, frequencies, color codes etc.
- The I/O Signals lists signal names and technical data for the I/O signals.
- The Troubleshooting Guide chapter is an aid in the process of diagnosing problems, and gives guidance for most types of errors.
- The Configurations chapter lists the different software and hardware revisions on the subassemblies, and links them to a system level revision and/or software version.
- The Maintenance Procedures and Replacement Procedures chapter also gives you installations procedures for e.g. software upgrades.
- The Peripherals chapter contains all necessary information required to install any peripheral listed in the beginning of the section; location, power connection, signal interface, user setup, switch settings etc.
- The Part Number List chapter lists all part numbers on all assemblies and subassemblies likely to be replaced.

2.3 How to Use the Manual Effectively

In order to use the manual effectively, it is essential that you have read or at least browsed through the whole book. When using the manual for troubleshooting, the following sequence should be followed.

1. Characterize the fault symptoms as specifically as possible.
2. Use the troubleshooting guide as a reference, and try and isolate the problem down to board level if possible. The guide will have references to other parts of the manual. In most cases fault isolation would imply running a test software routine.

   Note: One part of the diagnostic software will be accessible for the user.
3. Replace the indicated part(s).

2.4 Technical Skills Required

The manual is intended for use by qualified technical personnel with knowledge and experience in servicing advanced medical instrumentation. The reader should have basic electronic knowledge, and should have an understanding of techniques generally used in troubleshooting and repair. As mentioned before, a System FiVe Training Seminar is a requirement for servicing the equipment.

2.5 Repair

No printed circuit boards nor power supplies must be repaired in the field. All such parts must be returned to the manufacturer, GE Vingmed Ultrasound, Norway for repair.

3 Test Equipment and Tools Required

3.1 General Tools

This is a list of the minimum required tools for service on GE Vingmed Ultrasound's products

- PC Laptop with MS Windows 95 or MS NT 4
  - Minimum 200 MB free disk space
  - Ethernet adapter
  - CD-ROM
- RS-232 Cable (crossed)
- Twisted Pair Ethernet Cable (crossed)
- Twisted Pair Transceiver (MAU)
- Service Floppy Disks
- Service MO-Disk, 1.3 GB
- Phillips Screw Drivers
- Flat screw drivers
- Box spanners
- Allen keys
- Oscilloscope
- Multimeter
- Service Manuals
- Anti static mat / wrist band
- IC removers
- Antistatic brush for PCBs
- APA Probe cable
- APA Probe (optional)
- PA Probe (optional)
- Macintosh Keyboard
- Macintosh Mouse
- USB to ADB converter
- Multi-voltage SCSI CD ROM drive from Apple
- SCSI cable for CD-ROM Drive/Mac
- Power Cable for Multi-voltage SCSI CD ROM drive
- Simple External Video Grabber Board (optional)

3.2 Tools, Mobility Kit (Changing Wheels)

(In addition to the tools above):

- Sax jack, GEVU Part Number: 098C0001

- Tri-pod stand (2x), GEVU Part Number: 098C0010
- Umbrako wrench, 5 mm (front wheels)
- Umbrako wrench, 6 mm (rear wheels)

Your Notes:

4 New Functions/ Features

4.1 Abstract

The purpose of this document is to give a listing of the system features/functions that are supported by the different software versions:

4.2 Document History

Rev.	Date	By	Description
01	1 Aug 1996	GRL	First version of document per V1.1 release
02	30 Apr 1997	GRL	Updated per V1.2 release.
03	17 Nov 1997	GRL	Updated per V1.3 release.
04	10 Jun 1998	GRL	Updated per V1.4 release
05	11 Nov 1998	GRL	Updated per V1.5 release
06	28 Feb 1999	LHS	Updated per V1.5.3 & V1.6 release
07	6 Aug 1999	LHS	Updated per V1.7 release
08	10 Sep 1999	LHS	Updated per V1.8 release
09	19. Nov. 1999	LHS	Included info for sw v.1.7.1. Support for new TX128-2 Board.
10	2. Dec. 1999	LHS	Included info for sw. v.1.9.
11	1. Oct. 2000	LHS	Included info for sw. v.1.9.x

4.3 Supported Features

Please see the table starting on page “Intro-13”.

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Feature	Comments	V1.0	V1.1	V1.2	V1.3	V1.4	V1.5	V1.5.3	V1.6	V1.7/ 1.7.1	V1.8	V1.9	V 1.9.x
2D													
Zoom			x	x	x	x	x	x	x	x	x	x	x
Compound	LA probes on Premium only	x	x	x	x	x	x	x	x	x	x	x	x
RF imaging				Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Contrast imaging	With contrast agents			Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Octave Imaging	Certain probes only			Opt.	x	x	x	x	x	x	x	x	x
Color Flow													
Zoom			x	x	x	x	x	x	x	x	x	x	x
TVI	Tissue Velocity Imaging		x	x	x	x	x	x	x Opt. on “Advantage”	x Opt. on “Advantage”	x Opt. on “Advantage”	x Opt. on “Advantage”	x Opt. on “Advantage”
Angio			x	x	x	x	x	x	x	x	x	x	x
Velocity Profiles				x	x	x	x	x	x	x	x	x	x
Anatomic Color M-Mode				x	x	x	x	x	x	x	x	x	x
Mosaic (“HP”) color map							x	x	x	x	x	x	x
M-Mode													
Anatomic M-Mode				x	x	x	x	x	x	x	x	x	x
Doppler													
Tracking Doppler	Only on Premium systems	x	x	x	x	x	x	x	x	x	x	x	x
Autotrace				x	x	x	x	x	x	x	x	x	x

Feature	Comments	V1.0	V1.1	V1.2	V1.3	V1.4	V1.5	V1.5.3	V1.6	V1.7/ 1.7.1	V1.8	V1.9	V 1.9.x
Different Doppler color maps	Red, blue, yellow, gray, black on white					x	x	x	x	x	x	x	x
M&A													
Cardiac		x	x	x	x	x	x	x	x	x	x	x	x
PV			x	x	x	x	x	x	x	x	x	x	x
Abdominal				x	x	x	x	x	x	x	x	x	x
Ob/gyn.													
EchoPAC													
EchoPAC support		x	x	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
24 bit frame grabbing				Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Integrated EP support				Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
EchoPAC 3D support				Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Continuous Capture support	Including Frame Grabber III and RGB/S-VHS switch box						Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Other:													
Patient archive				x	x	x	x	x	x	x	x	x	x
Clipboard support				x	x	x	x	x	x	x	x	x	x
User defined defaults				x	x	x	x	x	x	x	x	x	x
Annotation recall/ restore					x	x	x	x	x	x	x	x	x
Update function					x	x	x	x	x	x	x	x	x
3D acquisition	FLA, CLA			Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
VCR remote control				x	x	x	x	x	x	x	x	x	x

Feature	Comments	V1.0	V1.1	V1.2	V1.3	V1.4	V1.5	V1.5.3	V1.6	V1.7/ 1.7.1	V1.8	V1.9	V 1.9.x
M&A on playback					x	x	x	x	x	x	x	x	x
Foot switch support				x	x	x	x	x	x	x	x	x	x
2D Frame counter				x	x	x	x	x	x	x	x	x	x
Heart rate indicator				x	x	x	x	x	x	x	x	x	x
ECG trigging				x	x	x	x	x	x	x	x	x	x
Stress echo (raw data)				x	x	x	x	x	x	x	x	x	x
Up/down, left/right				x	x	x	x	x	x	x	x	x	x
Bodymarks					x	x	x	x	x	x	x	x	x
Biopsy Support					x	x	x	x	x	x	x	x	x
TEE temp. override ($43^{o}C$)					x	x	x	x	x	x	x	x	x
EchoMAT support					Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.	Opt.
Selectable phono filters						x	x	x	x	x	x	x	x

Your Notes:

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Abbreviations, Definitions, Glossary, Terminology, Nomenclature

Revision Status for the SYSTEM FIVE Service Manual

Date	Rev.	Edition #	Description and comments
11 Oct 1994	01	1	• First version, -Draft
20 Sep 1995	02	2	• Corrected errors. • New documents included.
1 Dec 1995	A	3	• Service Manual Release. • Corrected errors. • New documents included. • New Index.
14 Oct 1996	B	4	• Service Manual divided in three parts. • Corrected errors. • Updated documents. • New documents included.
19 Jun 1998	C	5	• Documents not needed for field service, have been removed. • Updated documents (sw 1.3). • New documents included. • Updated documents (sw 1.4).
14 Dec 1998	D	6	• Updated documents (sw 1.5) • Updated company name and logo.
5. Aug 1999	E	7	• Updated documents (sw 1.5.3, sw 1.6 & sw 1.7)
8. Sep 1999	F	8	• Updated documents per sw 1.8 release (BT-99)
18. Oct 1999	G	9	• Included info for sw. 1.7.1.
23. Dec 1999	H	10	• Included info for sw. 1.9.
1. Oct. 2000	I	11	•Updated documents per sw. 1.9.x release.

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Your Notes:

SYSTEM FIVE Theory of Operation

Overview

Introduction

This part of the SYSTEM FIVE Service manual gives you the theoretical background to understand how the instrument works.

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The table below gives you an overview for this part of the Service Manual:

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Notes.

SYSTEM FIVE System Overview

Overview

Introduction

This part of the SYSTEM FIVE Service manual gives you the theoretical background to understand how the instrument works.

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Your Notes:

Principles of Operation – rev. 06

1 Introduction

1.1 Abstract

The purpose of this document, “Principles of Operation”, is to give the service technician/ engineer the theoretical background to understand how System FiVe works, both with respect to functionality, data flow and control. This knowledge together with the System Description, block diagrams and the aid from the “Troubleshooting” chapter, should enable the engineer to diagnose, localize and repair any service problem that might occur.

1.2 Overview

The document starts with definitions and descriptions of various terms and techniques used in the system. This section describes the operation of phased and linear array imaging including digital beamforming, annular array imaging, tissue processing methods, spectrum analysis and color flow processing techniques and post processing methods.

1.3 Revision History

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Rev.	Date	Sign.	Description
01	15 June 1994	GRL	First version.
02	2 Jan. 1995	LHS	Updated layout. Corrected some minor errors.
03	30 May 1996	GRL	Added Scan Seq. diagrams for PA and AA
04	28 Feb. 1999	LHS	Fixed a few grammatical and spelling errors
05	19 Oct. 1999	LHS	Updated to include changes from sw. 1.7.1.
06	20 Jun. 2000	LHS/ JB	Corrected errors.

1.4 Terminology

A number of different terms are used when describing medical ultrasound; how it is implemented, how probes are made, basics on the ultrasound beam, image quality etc. This section is provided to give a short explanation of the terminology used in the field. Later, some of the terms are outlined in more detail.

Transducer:

A device made of piezoelectric material that will vibrate at its resonance frequency when a voltage is applied to it, emitting a wave.

Aperture:

Size of the transducer, with respect to number of wavelengths or in millimeters.

Expanding Aperture:

The number of elements in the receiver is reduced for shallow depths and gradually increased with depth in order to obtain a uniform focus width throughout the image field.

Effective Aperture:

The projected aperture when angling the beam using phased arrays.

Apodization:

Weighting of the contribution from elements at the edges in an array transducer. Can be used both on transmit and receive.

Propagation velocity:

The speed of the ultrasound wave through the body. Is different for different types of structure (tissue, blood, fat etc.).

Far field:

The area of the ultrasound beam where it expands beyond the aperture of the transducer.

Near field:

The area of the ultrasound beam where its width is less than the aperture of the transducer.

Main lobe:

The area of where the ultrasound beam travels where the signal intensity is within a certain limit.

Side lobe:

Small fields outside the main lobe, caused by the nature of the transmitted signal.

Reflector:

A plane and large (compared to the wavelength) interface reflecting portions of the transmitted signal back towards the transmitter, straight or in an angle.

Scatter:

A small object (compared to the wavelength) spreading the transmitted signal in all directions, reflecting a small portion.

Geometrical focus:

The center of the curvature in a curved transducer.

Depth of focus:

The distance on each side of the focal point where the beam intensity is above a certain number.

Dynamic focus:

Tracking of the focus point during receive, from close to far depths.

Composite Transmit Focus:

A vector is constructed from samples from several transmit pulses with different focal points.

Contrast resolution:

The ability to show a signal from a weak target close to a strong target (also called local dynamic range).

Axial resolution:

The ability to separate two neighboring reflectors in the beam direction (vertically). Proportional to frequency.

Lateral resolution:

The ability to separate two neighboring reflectors transverse to the beam (horizontally). Inversely proportional to beam width.

Reverberations:

Multiple reflections between materials (e.g. tissue and fat) with different propagation velocity, causing “ghosts”, artifacts and noise in the image.

TGC:

Time Gain Compensation used in the receiver to compensate for the fact that reflections from larger depths are attenuated more than reflections from shallower depths.

Speckle:

Texture from a homogeneous material (e.g. tissue). Will be finer grained with higher frequency.

Penetration:

A measure for how deep one can visualize structures.

Compression:

Amplification of low level echoes and attenuation of high level echoes, so that both can be displayed and visualized at the same time.

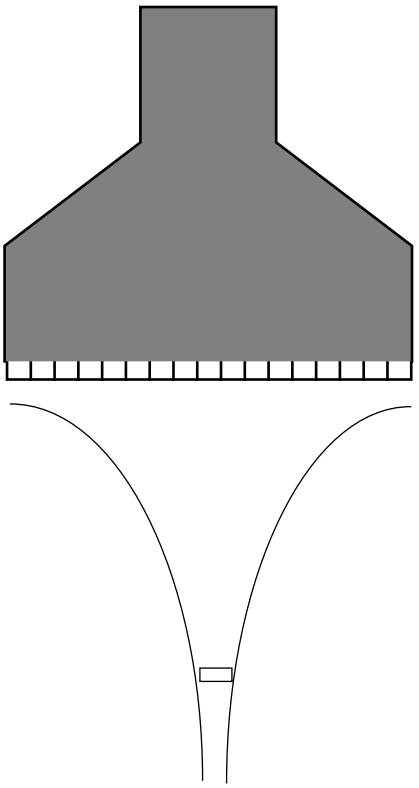
Compound scanning:

Using linear arrays, an object can be scanned from different directions. By combining the data acquired from these directions, an image with better resolution and finer speckle can be obtained.

2 Phased-, Linear- and Curved Linear Array Imaging

2.1 Introduction

Phased array, linear array and curved linear array probes consist of several transducer elements (e.g. 64, 128, 192) which all can be excited independently for the purpose of both steering the ultrasound beam and focusing the beam at desired depth. For receive focus purposes, the returning echoes from the different elements can be delayed accordingly in the beamformer, thus receiving echoes from different depths at the same direction as the transmit beam was fired.



2.2 Array Types

Arrays are typically divided into plane and curved. Phased- and linear arrays are plane, while curved linear- and annular arrays are curved. Phased arrays and linear arrays have the same basic construction; though linear arrays usually have larger and more elements due to the nature of the scan types used.

Plane Arrays

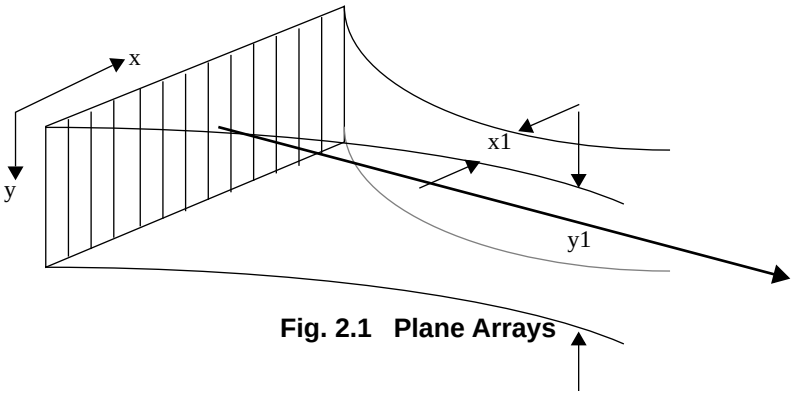


Fig. 2.1 Plane Arrays

The above array has electronic focusing in one dimension only, x1, not in the elevation plane, y1. By curving the element in the y-direction a fixed (not electronic) focus can be obtained in this direction also. This is how the System 5 probes are designed.

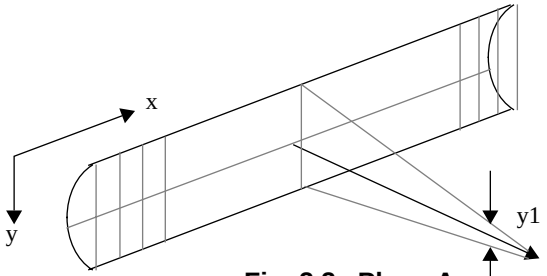
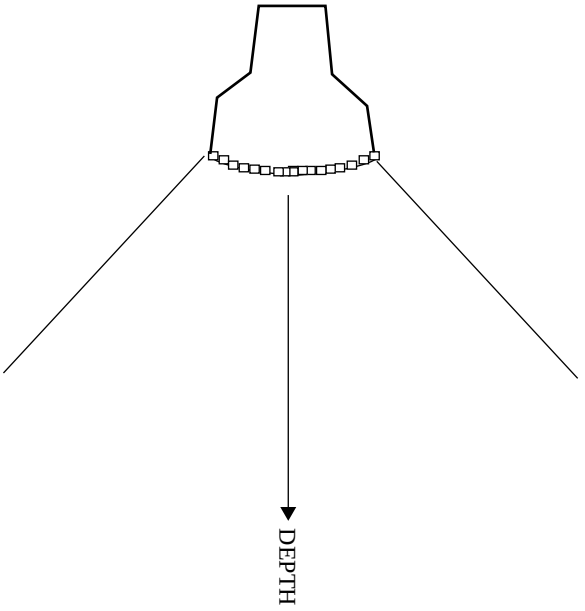


Fig. 2.2 Plane Arrays, curved in y-direction

Curved Linear Arrays

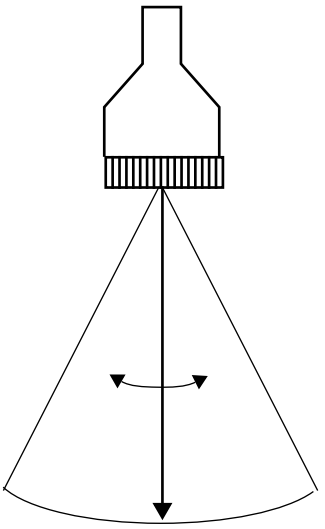
A curved linear array is shown below. This type of array has a fixed value (negative) for the geometrical focus but with the use of electronic focusing and stepping of the elements (see later) each line can be focused.



2.3 Image Formats

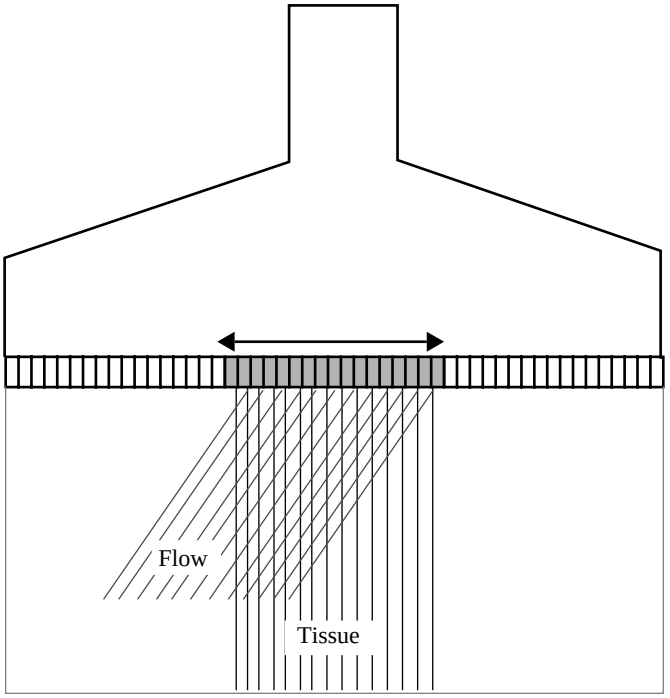
Some of the most common scan formats for the different array probes are shown. Type of scan will depend on application and mode.

A phased array scan is typically used for cardiac applications, where one has to access the area of interest (the heart) through the ribs. The elements must have a small width (=< l/2, l is wavelength), e.g. ~3 mm for a 128 element / 2.5 MHz probe. The ultrasound beam is steered in a sector by delaying transmit time for the various elements.

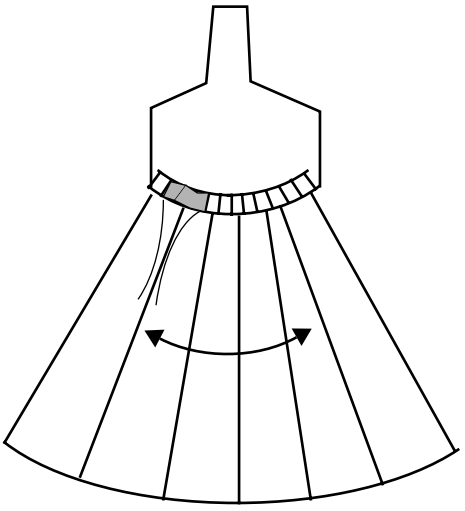


A linear array scan is typically used for abdominal, peripheral and ob/gyn. applications. In these cases the ultrasound beam is steered in the same direction (modewise) and only a subset of elements is used to generate the beam. By switching to another subset, the beam can be swept horizontally. Beams for 2D Flow and Doppler are usually angled compared to 2D Tissue in order to obtain optimal access for acquiring the different types of data (blood flow and tissue structure).

Due to the relatively large elements (1 - 3 l), the beam for each element is quite narrow and angling of the vectors is limited. The linear array images are displayed in a rectangle or parallelogram.



Curved linear array probes can be used for all the previously mentioned applications. It is operated the same way as a linear array probe, however, due to the geometrical shape of the aperture, the scan format resembles that of a phased array. The beam is swept in an arc by gradually switching the subsets of the curved array. It has a major advantage in a wider image field and better skin contact than linear array.



2.4 Electronic Steering of Probe / Transmit Focusing

2.4.1 Transducer element basics

As mentioned in the introduction, the electronically steered transducers are constructed of several elements, isolated from each other. The element size and interspacing (pitch) depends on probe type, and is usually <= 0.5 l for phased arrays where l is the wavelength given by

$$l = c / f \quad (2.1)$$

(c is propagation velocity in tissue ~ 1540 m/s and f is transducer frequency).

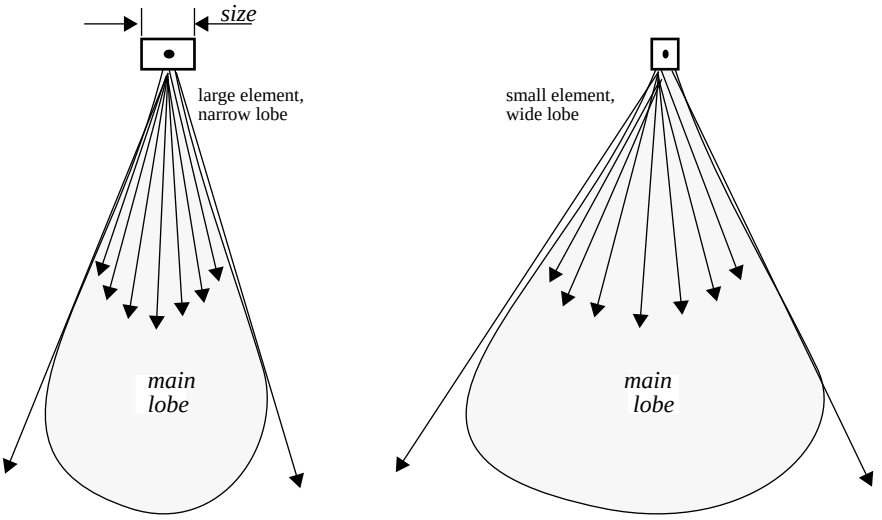


Fig. 2.3 Main Lobes

One of the criteria for selecting the pitch- and element size is given by the maximum angle one wants to steer the beam, and at the same time avoid having reflections from the so-called grating lobe (which is a mirror of the main lobe at an angle given by the element pitch and the steering angle). The main lobes for one element with two different sizes are shown on the figure above. When firing the element, such a lobe can be defined as the area where the acoustic intensity is above a certain limit (e.g. > -12dB) compared to the intensity at the center of the lobe. The shape of the main lobe gives the maximum angle one can steer a beam without loosing too much sensitivity (e.g < -12dB). From this can be seen that linear and curved linear have can have larger element size and pitch since it is not necessary to steer the angle as far out as for phased arrays.

2.4.2 Steering the beam

When firing a pulse into an element, an ultrasound wave will start to travel from the element into the body. It will spread out inside the main lobe. If all elements in an array are fired simultaneously, the resulting main wave from all elements will travel perpendicular to the array surface.

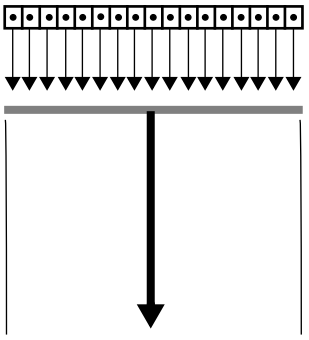


Fig. 2.4 Simultaneous firing

However, if the elements are fired with certain delays, the beam can be steered in an angle. In the figure below, the right element is fired first and, then with a small delay the element next right etc. until the left element is fired last and with the largest delay.

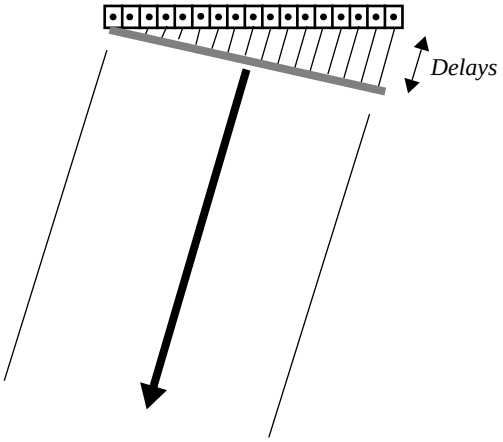


Fig. 2.5 Steering Delays

2.4.3 Transmit Focusing

So far we have achieved to steer the beam in the direction we want to. The next step is to also focus the beam at a desired depth. This is done by introduction of so-called focus delays. The purpose of these is to form an electronically steered lens, where the ROC (Radius of Curvature) can be altered according to selected focal point.

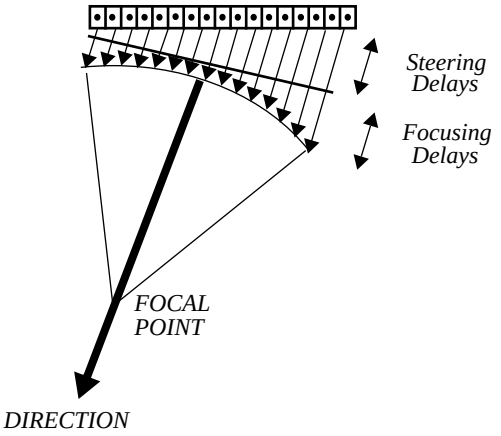


Fig. 2.6 Focus Delays

The steering delays and focus delays are added together to a total delay component. For each line (or angle) these delays are calculated when a probe is connected to the system. They will depend on probe frequency, number of elements, aperture probe, maximum allowed scan angle etc. and are stored in a memory on the Transmitter board ready to be used when the desired scan patterns are called for.

2.4.4 Effective (Projected) Aperture

A disadvantage with phased array probes is that the effective aperture of the transducer is reduced at larger angles.

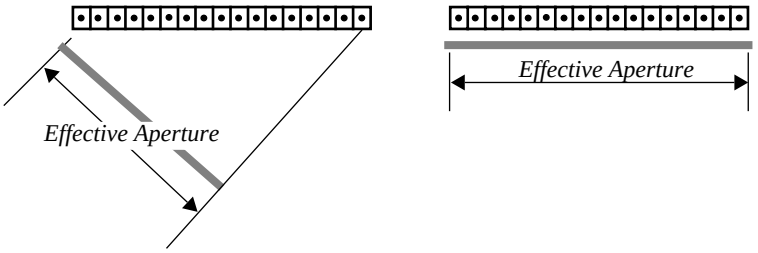


Fig. 2.7 Effective Aperture

Resulting problems are increased width of the ultrasound beam and decreased sensitivity on receive side, since we are now operating at the outer limits of the main lobes for each of the elements. In order to compensate for this, the beamformer has individual gain control for each beam (or line/angle).

2.4.5 Digital Beamforming / Receive Focusing

The purpose of having a digital beamformer is to discretely sum the received echoes from all transducer elements from each range (or depth), called true dynamic focusing. Parallel processing can be used to generate multiple beams simultaneously, so-called Multi Line Acquisition, see *section 2.4.7* for details on this. One can also have a higher frame rate than in analog systems due to the ability to quickly step from one angle to another.

When receiving echoes from a single reflector with a plane surface, they will be misaligned in time when added together, as shown in *Fig. 2.8* due to the uneven distance the beam has to travel before it hits the surface. This will result in an unfocused image.

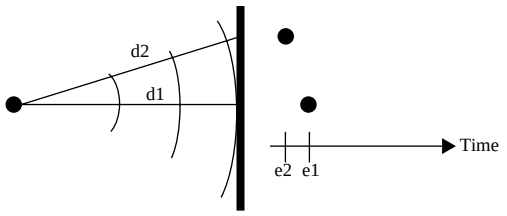


Fig. 2.8 Unfocused

If the reflected signal was received by a curved surface with the same curvature as the “reflected wave”, the echoes would be aligned in time when summed together. The effect of having a curved transducer can be obtained by delaying echoes from some elements, in the example above the echo travelling the distance, d1, would have to be delayed to be aligned with the one from d2.

In the Vingmed digital beamformer the delays are implemented in custom made integrated circuit, called FOCUSORs. One focusor handles the delays for four neighboring elements and also adds them together. Adding of focusor outputs is done by another custom made integrated circuit, called a BEAMADDER.

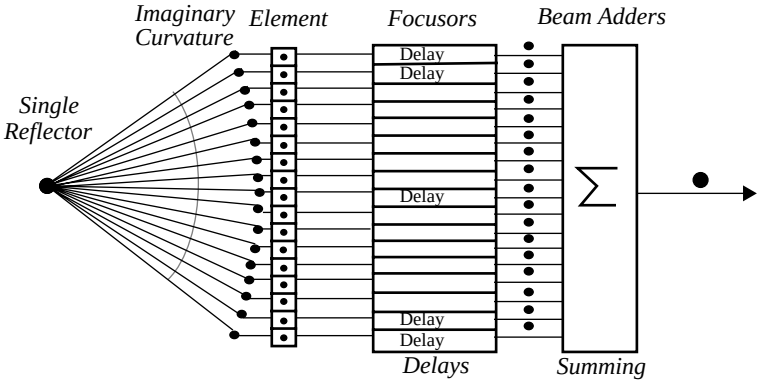
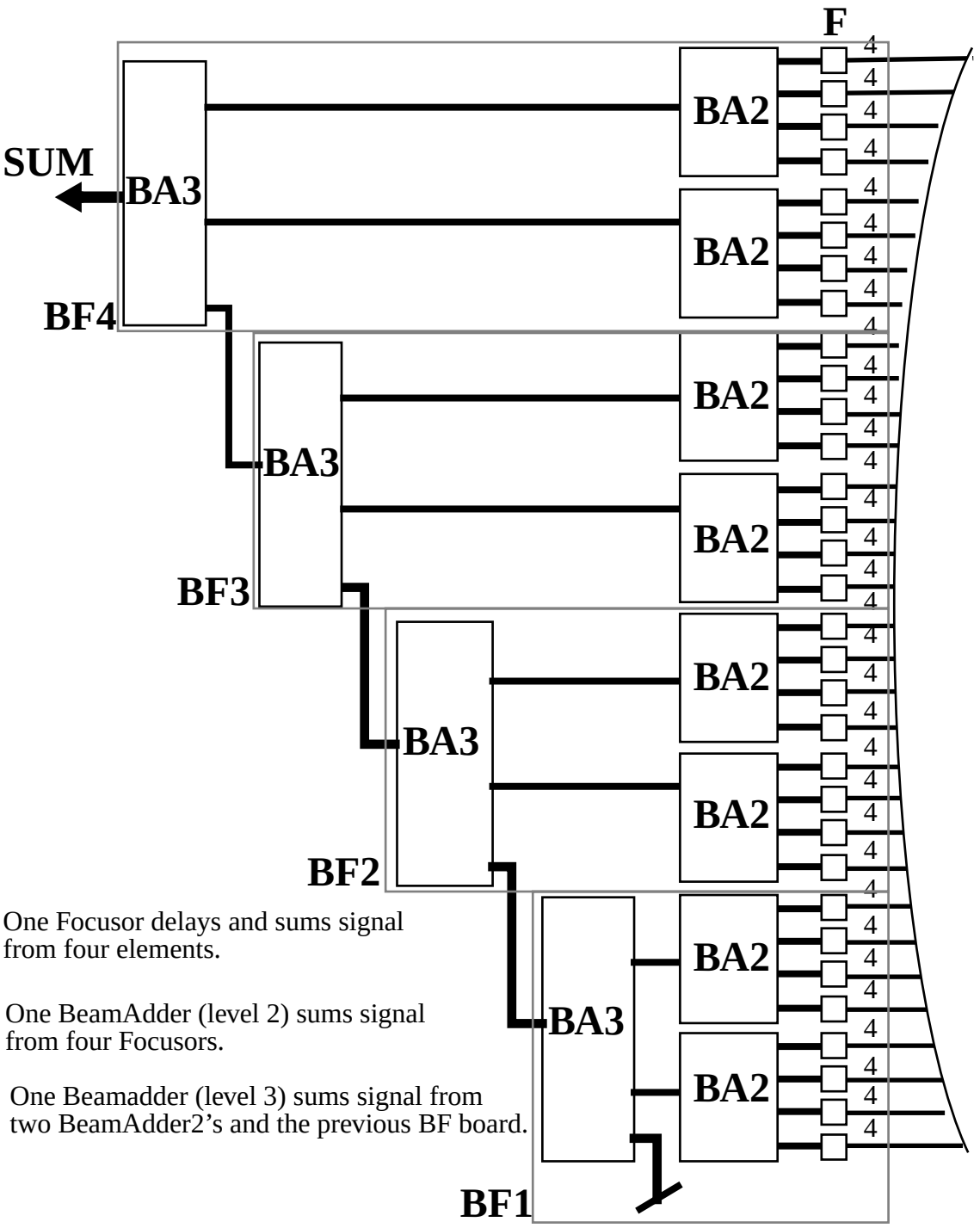


Fig. 2.9 Focused

It takes a total of 32 focusors and 8 beamadders to focus and sum the 128 channels in the beamformer.



One Focusor delays and sums signal from four elements.

One BeamAdder (level 2) sums signal from four Focusors.

One Beamadder (level 3) sums signal from two BeamAdder2's and the previous BF board.

2.4.5.1 Steering the beam

The same parameters are used for generating the steering delays for the beam during receive as during transmit.

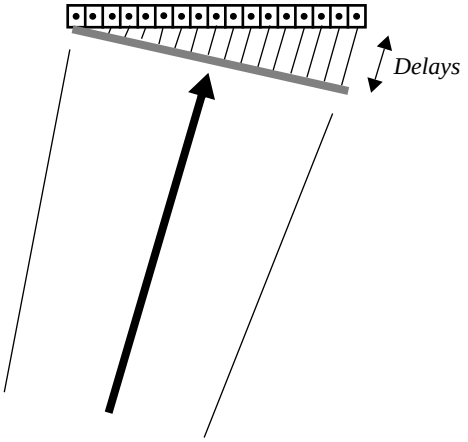


Fig. 2.10 Steering Delays

2.4.5.2 Receive Focusing

The same principles are used for generating the receive focus delays as the transmit focus delays. The purpose is to generate an electronically steered lens with a variable ROC. However, during receive the delays are updated (calculated inside the Focusors) for each range (or depth step) starting with large delays at the array edges focusing at a narrow range, gradually decreasing the delays to “open up” the lens until infinite focusing (straight lens) is obtained.

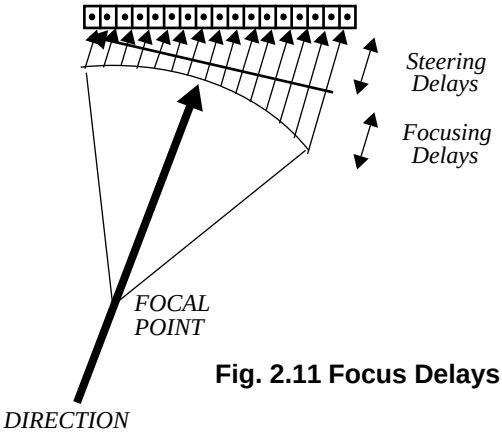


Fig. 2.11 Focus Delays

2.4.5.3 Apodization

In order to control the side lobe level of the beam, apodization is introduced. This is a windowing function applied to all channels, where the receive signal is gradually “attenuated” when approaching the outer elements of the transducer aperture. Apodization is used together with expanding aperture, see *section 2.4.5.4*.

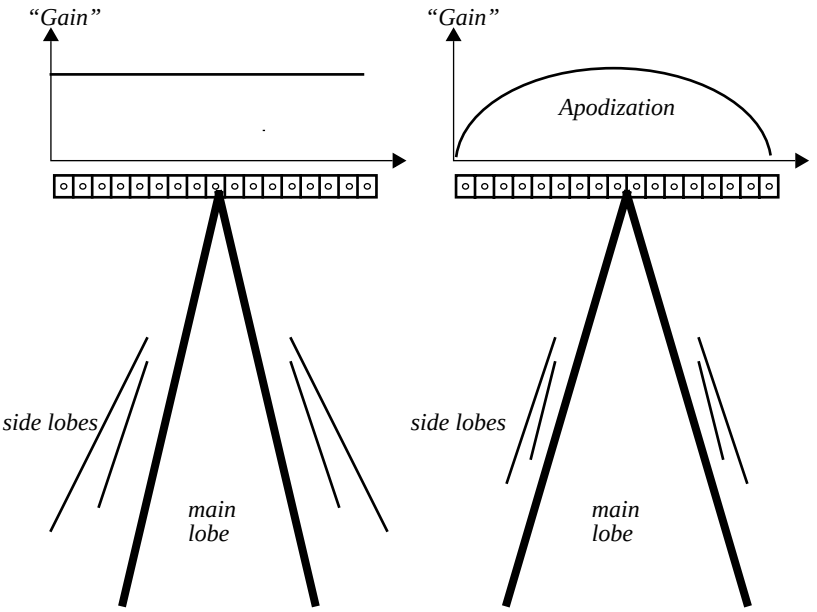


Fig. 2.12 Apodization

2.4.5.4 Expanding Aperture

The width of a focused ultrasound beam depends on the focal point and the size of the probe aperture according to the following formula:

$$D_F = k^*l^*F/D \qquad (2.2)$$

where F is distance to focal point, l is wavelength and D is transducer aperture. The beam width will

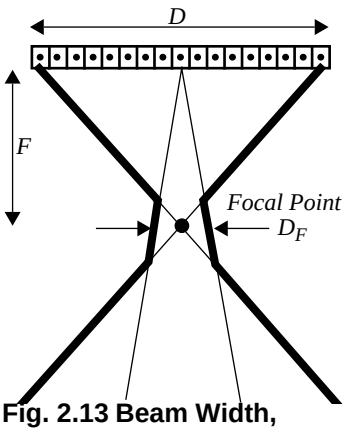


Fig. 2.13 Beam Width, Constant Aperture

with a constant aperture, be as shown on the figure above (the thick line) for that particular focal point. For a shallower focal point, the beam width will be narrower.

In order to maintain approximately the same width as far as possible from the transducer throughout the field of view, it is necessary to reduce the aperture when focusing at shallow depths (to widen the beam on purpose) and gradually increase it when focusing deeper (to narrow the beam), thus achieving a beam with constant width. This is called expanding aperture and causes the beam width to be fairly constant. It is achieved by controlling the number of active elements participating in receive. The purpose of keeping the beam width the same, is to obtain a uniformly focused image and to reduce side lobes in the near field.

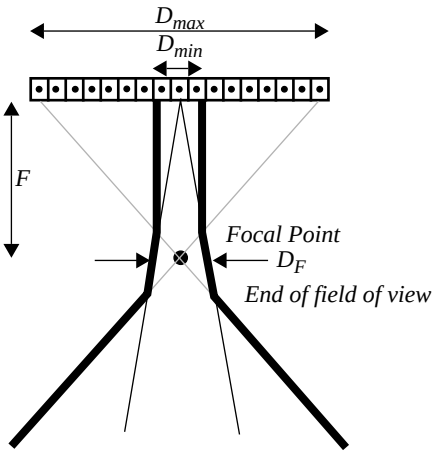


Fig. 2.14 Beam Width, Variable Aperture

2.4.6 Switching linear arrays

In order to obtain the excellent image quality which is required for most abdominal and peripheral applications, linear arrays are used. As mentioned in *2.3*, these arrays have large elements, focusing well straight down. Due to the large aperture, there is not enough delay to steer the beam out to e.g. 45 ^{o}, so the way to cover a sufficient field of view, is to use a few arrays to construct one vector, then switch in another set of arrays to construct the next vector, and so on. In this way the beam will sweep horizontally along the whole array surface. The switching of elements is done both on the transmitter and in the beamformer. In linear arrays with more than 128 channels (e.g. 192) there is a multiplexer (located inside the probe) continuously rerouting 128 of the 192 channels into the 128 receiver channels.

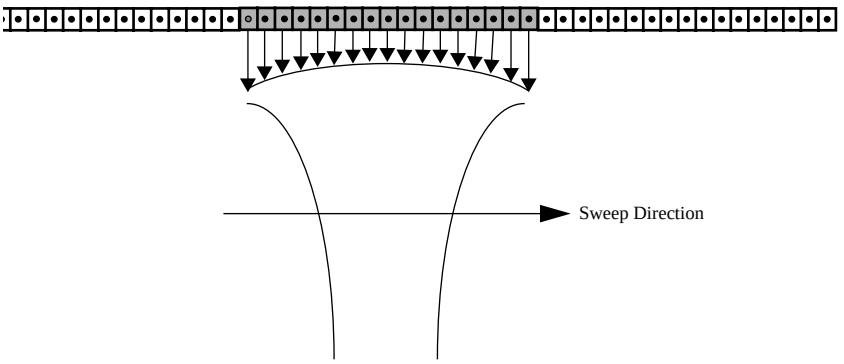


Fig. 2.15 Linear Array Sweeping

2.4.7 Multi-Line-Acquisition

The standard System 5 beamformer generates one vector or line when receiving data from one transmit pulse. Optionally, two additional beamformers can be implemented working in parallel with the first one, generating three simultaneous lines. Each of the beamformers will in this case have different steering delay parameters. The lines must be located relatively close together (within the main lobe of the transmitted beam). The advantage of Multi-Line-Acquisition is increased framerate.

MLA is implemented physically by installing more focusors and beamadders after the A/D converters on the Beamformer boards.

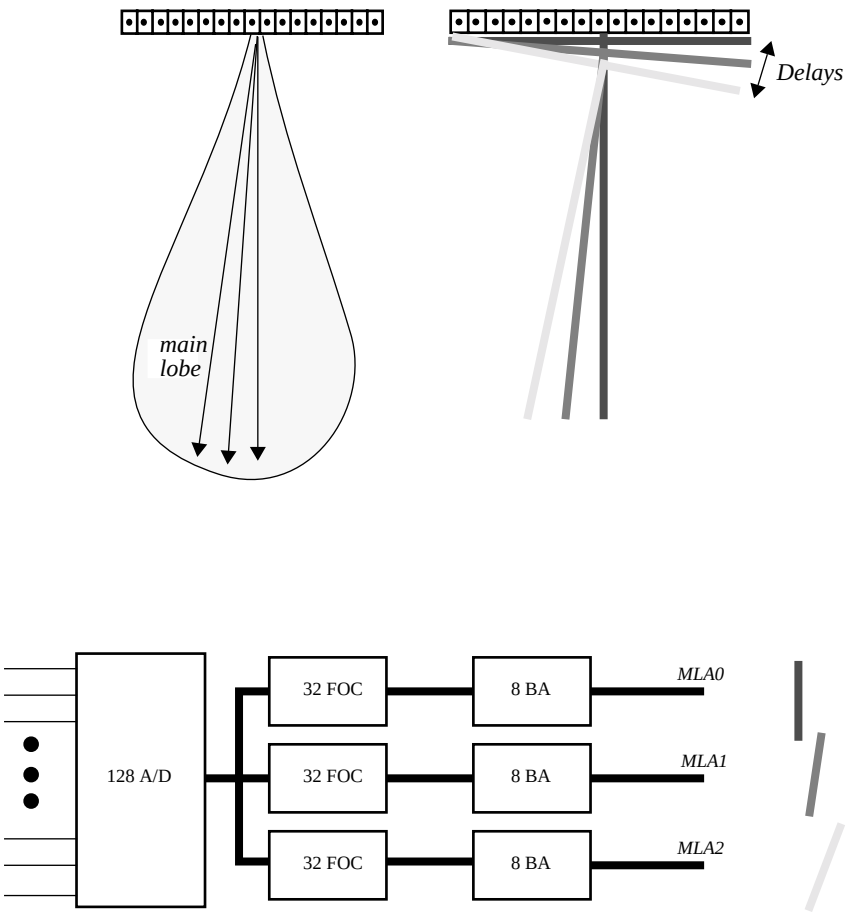
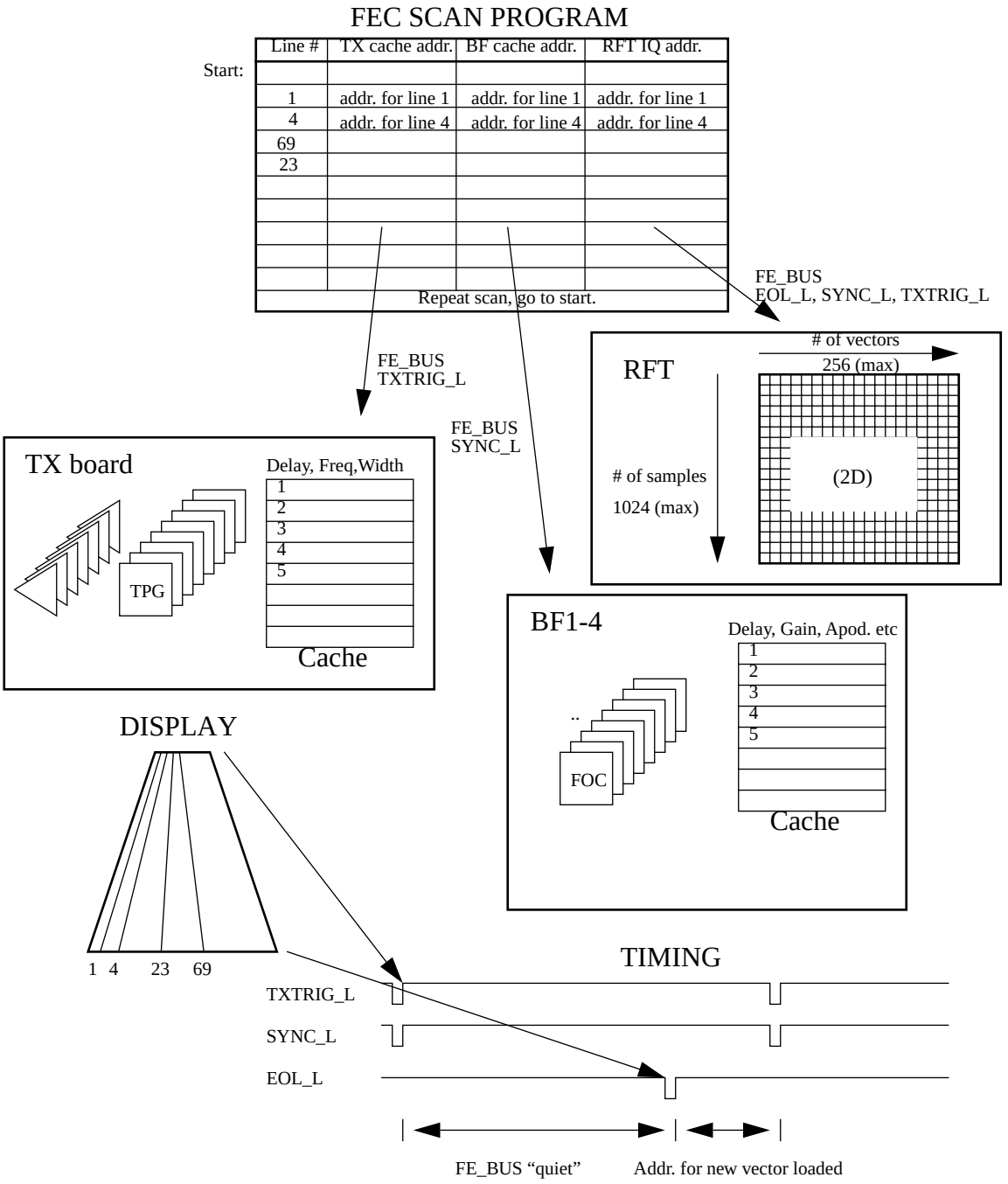


Fig. 2.16 Multi-Line-Acquisition

2.4.8 Scan Sequencing

Initially (before start of scan) FEC loads all parameters into TX and BF cache.
Then the scan program is started on FEC. FEC loads tx-parameters from TX cache into TPGs for vector # n (listed in program). Then it loads bf-parameters from BF cache into Focusor ASICs for vector # n. FEC tells RFT to start loading the preceding data for vector # n from start addr. FEC issues a TXTRIG_L to fire the transmitter, a SYNC to synchronize reception and a EOL_L (End Of Line) indicating that the bottom of FOV is reached.
After a tx pulse is fired, received data is continuously digitized, delayed, filtered and stored

in IQ memory. During this time, the FE_BUS is ‘dead’.
After EOL_L is reached, FEC loads data for another vector.

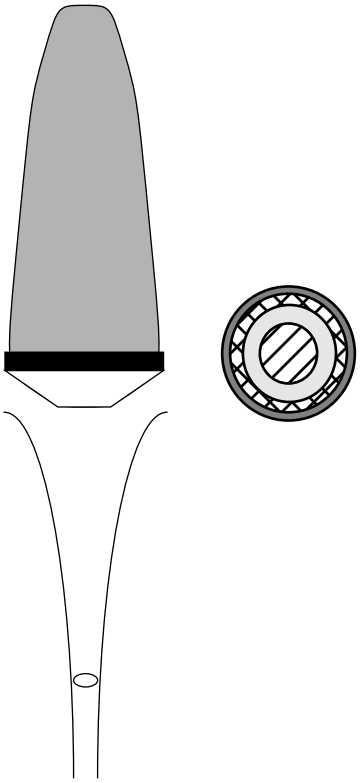


3 Annular Array Imaging

3.1 Introduction

The Vingmed Annular Array probes consist among other things of a transducer element built up by 2 -5 concentric rings, made by a piezoelectric material, where the rings are electrically isolated from each other.
High voltage ultrasound pulses in the range of 2 - 7.5 MHz are repeatedly applied to the different rings with a pulse repetition rate determined by the system setup (like depth and angle). These pulses forming an ultrasound beam, traverse into the body. Most of the energy is absorbed/attenuated (apprx. 1dB/MHz/cm) in the tissue, but some energy is reflected by

structures and moving blood cells. These reflections are used to generate Tissue- and Doppler/Flow images.
An advantage with the concentric rings in the annular array probes as opposed to phased array probes is the ability to focus also transverse to the scanning plane, in addition to the normal focus in the axial and lateral planes.



In order to obtain an image of a plane through the heart, the ultrasound beam must be swept in an arc. This is done mechanically by a motor driving the element back and forth while transmitting and receiving.

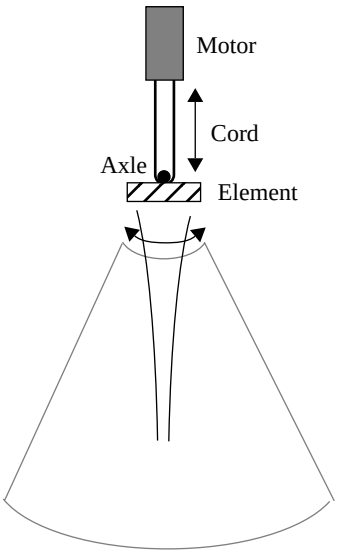


Fig. 3.1 Element Movement

3.2 Moving the Transducer Element

As outlined in the introduction, the transducer element is moved mechanically by a motor. The linear motor is driven by a controller in regulator loop. A reference sweep is generated on the controller. This sweep is compared to a position feedback signal (from the probe) reflecting the position of element. The difference between the reference and the position feedback is used to drive the element in the desired direction.

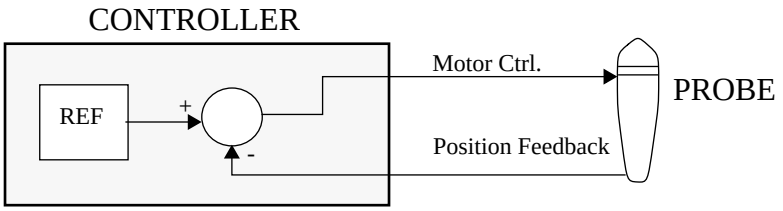


Fig. 3.2 Motor Controller

Type of sweep will depend on mode of operation and system setup. The frequency and amplitude of the reference sweep will determine the scan angle and framerate of the displayed sector. Below is shown a sweep used in Triplex mode, with a tissue scan going left, a flow scan going right and Doppler when element stands still. A tissue scan is usually significantly shorter than a flow scan due to the required data collection time in the two modes.

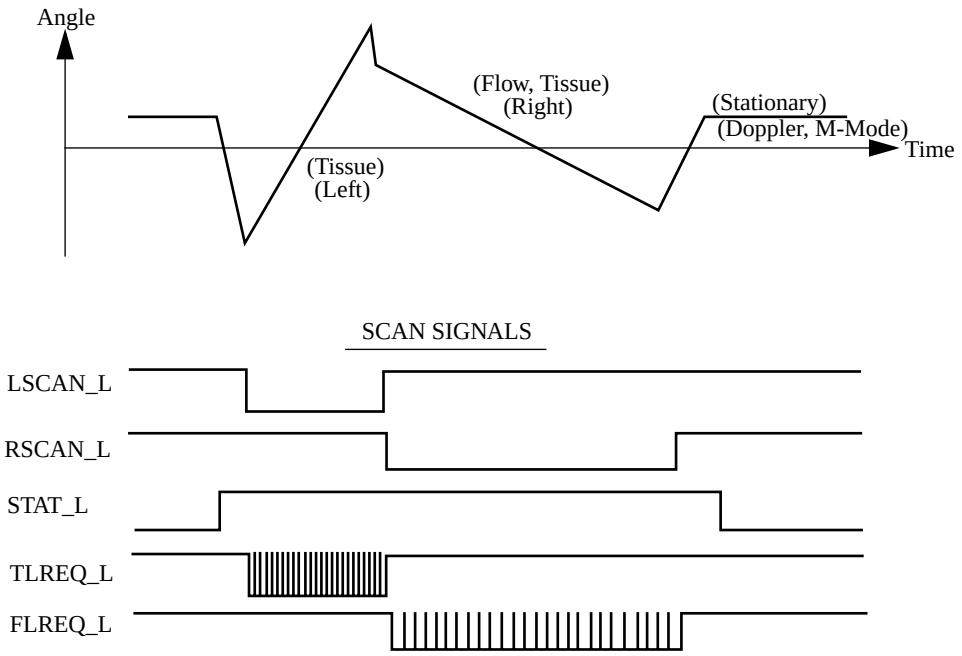


Fig. 3.3 Scan Signals

The controller generates several scan signals that will vary depending on the sweep type. These signals are used by the system to synchronize transmit firing and receive sampling of echoes.

LSCAN_L (Left Scan) is active when the element moves from right to left.

RSCAN_L (Right Scan) is active when the element moves from left to right.

STAT_L (Stationary) is active when the element is standing still.

TLREQ_L (Tissue Line Request) is pulsed active each time a tissue scan line should be generated (maximum 128 times per scan). It initiates the transmit firing sequence.

FLREQ_L (Flow Line Request) is pulsed active each time a flow scan line should be generated (maximum 64 times per scan).

3.3 The Ultrasound Beam

Resolution and Penetration

In order to obtain sharp, well-defined images, the ultrasound beam must be as narrow as possible in the region of interest. Lateral resolution (the ability to separate two adjacent horizontal reflectors) is directly proportional to the beam width which again is determined by the element radius and curvature, in addition to distance (depth) from transducer and frequency of the ultrasound. Axial resolution (the ability to separate two adjacent vertical reflectors) is inversely proportional to the ultrasound frequency, not affected by the beam width. Axial resolution will improve with increasing frequency. However, since tissue absorption of ultrasound increases with frequency the penetration will decrease. Penetration is a measure for how deep one can visualize structures.

Transmit Focusing

From the field of optics it is known that to focus a light beam, one uses curved lenses, (i.e. in glasses). Curved lenses will produce a focal point at a fixed distance from the lens. For ultrasound scanners where the area of interest can vary from e.g. 10 to 25 cm with the same type of probe, a fixed focus is not sufficient. One must be able to change it. This is done by controlling the transmit delay between the element rings. Each of the rings can be “fired” independently at different times during transmit. By exciting the outer ring first and then the inner rings with larger delays as time elapses, the focal point can be programmed to the desired depth as illustrated in the figure below. The time delays can be changed depending on depth setting, thus achieving a variable focal distance.

Using this method of firing transmit pulses gives the same effect as if the element was curved like a lens and the curvature could be changed.

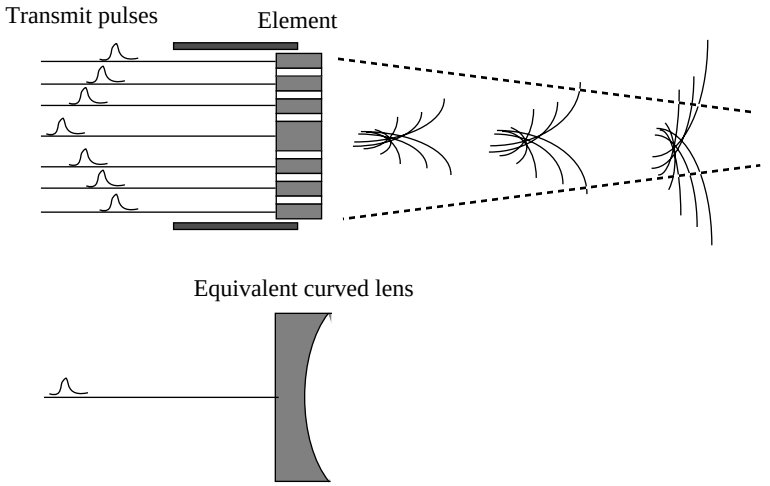


Fig. 3.4 Transmit Focusing

Receive Focusing

Focusing on receive is necessary due to the fact that the reflected signal from a target will not return to all probe rings at the same time, this due to the uneven distance it has to travel. In order to compensate for this, the signal returning to the center and inner rings are delayed with respect to the outer ring, thereby “aligning” the reflected echoes in time.

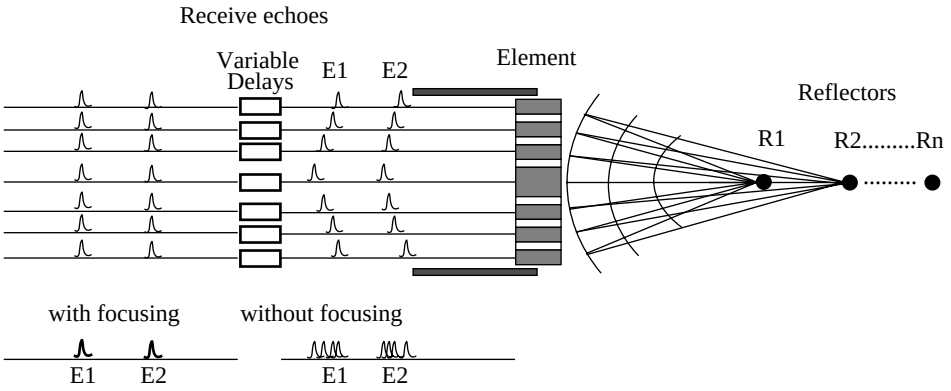


Fig. 3.5 Receive Focusing

In System 5 the reflected signal from each ring is fed to 16 different Focusors.

3.4 Image Formats

3.4.1 M-Mode

In M-Mode the probe element is standing still (in Stationary mode) pointing at the area of interest. M-Mode is displayed in the time domain with the time on the x-axis and depth along the y-axis. As time elapses one will see the movement of the targeted objects on the display.

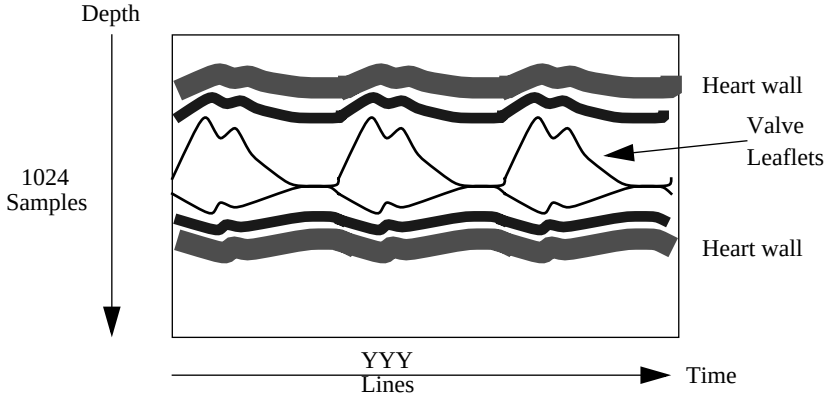


Fig. 3.6 M-Mode Display

3.4.2 2D Tissue

In 2D mode the probe scans through a sector while transmitting ultrasonic pulses and receiving echoes from structures and tissue. When doing one scan (from left to right or right to left), a total of maximum 128 transmit pulses are fired and 128 scan lines (or beams) are constructed. Each scan line consists of maximum 1024 samples.

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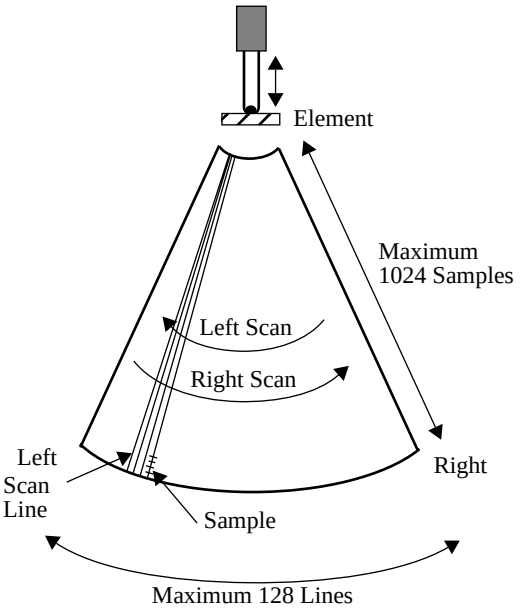

Fig. 3.7 2D Tissue Sector Display

3.4.3 Doppler

The probe element is standing still (in Stationary mode) pointing at the area of interest. The spectrum is, as M-Mode, displayed in the time domain with time along the x-axis and velocities along the y-axis. The spectrum analyzer can differentiate 256 different velocity components.

The spectrum display is organized as shown in *Fig. 3.8*.

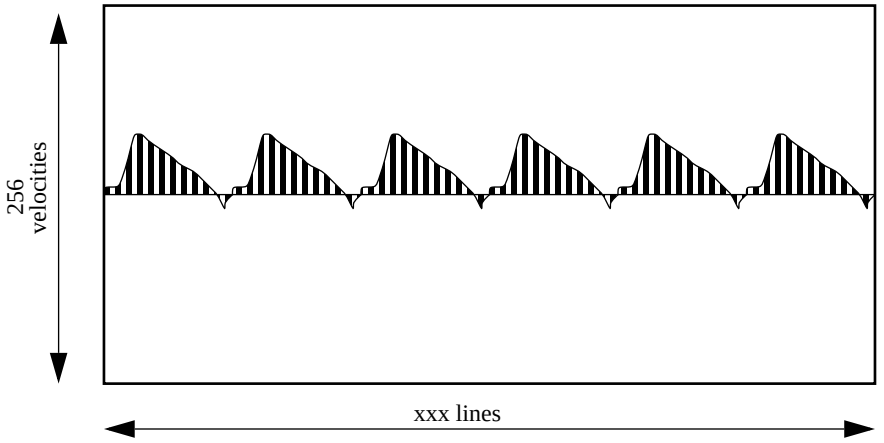

Fig. 3.8 Spectrum Display

3.4.4 Color Flow

The color sector is divided into yyy flow scan lines and maximum 256 samples per scan line as shown in *Fig. 3.9*. When collecting data for 2D Flow, the probe usually scans from left to right while transmitting the ultrasound pulses and receiving the Doppler shifts from moving objects.

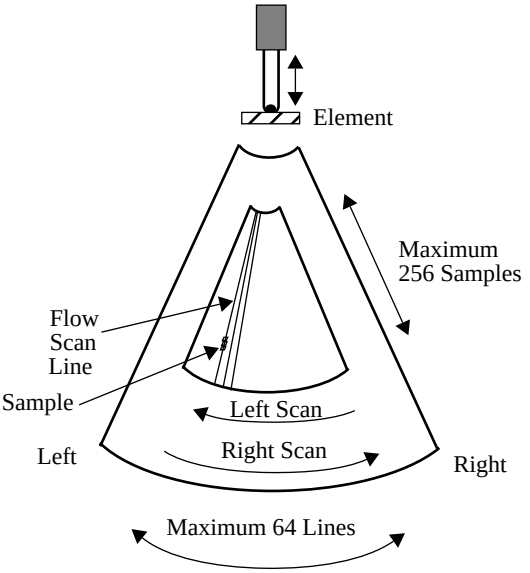

Fig. 3.9 2D Flow Sector Display

3.4.5 Color M-Mode

In Color M-Mode the flow information is superimposed on the tissue M-Mode display. Data is collected while the probe is standing still. Display is in the time domain. Tissue vectors along the depth-axis is constructed from maximum 1024 tissue samples, while color vectors are constructed from maximum 256 color samples.

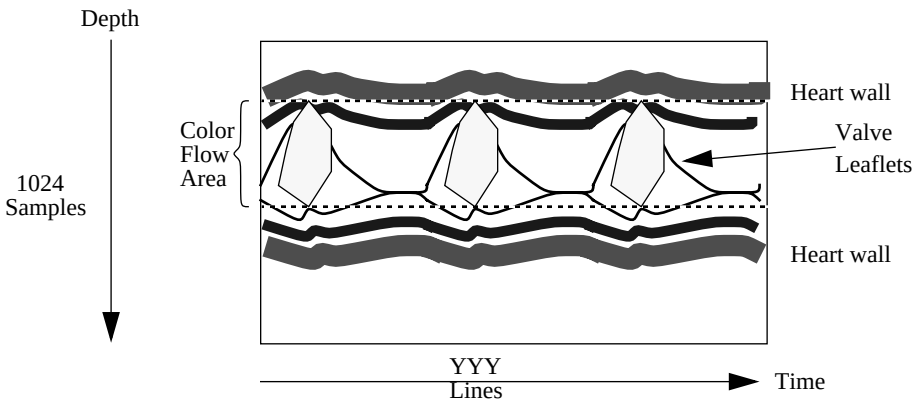

Fig. 3.10 Color M-Mode Display

4 Tissue Processing

4.1 General description

M-Mode

The pulse repetition rate of the transmit pulses in M-Mode is fairly high compared to 2D mode, and is limited by the acoustic velocity of sound in tissue (~1540 m/s) and the desired field of view / depth. After a pulse has been transmitted, a relatively long time is used for receiving the returning echoes from the body. The received echoes are amplified, A/D converted, focused, TGC controlled, filtered, detected, compressed, peak detected, edge enhanced and clipped before being stored in memory, scan converted and displayed. Maximum 1024 samples are constructed for each transmit pulse.

2D Tissue

One pulse is fired in one direction, then the received echoes from this pulse is amplified (ATGC), A/D converted, focused (receive focusing), digital TGC controlled, filtered, detected, compressed, offset is added and the signal is clipped, see functional block diagram, *Fig. 4.1*. A new pulse is fired, and the same sequence is repeated.

Below is shown a functional block diagram of the 2D Tissue data flow.

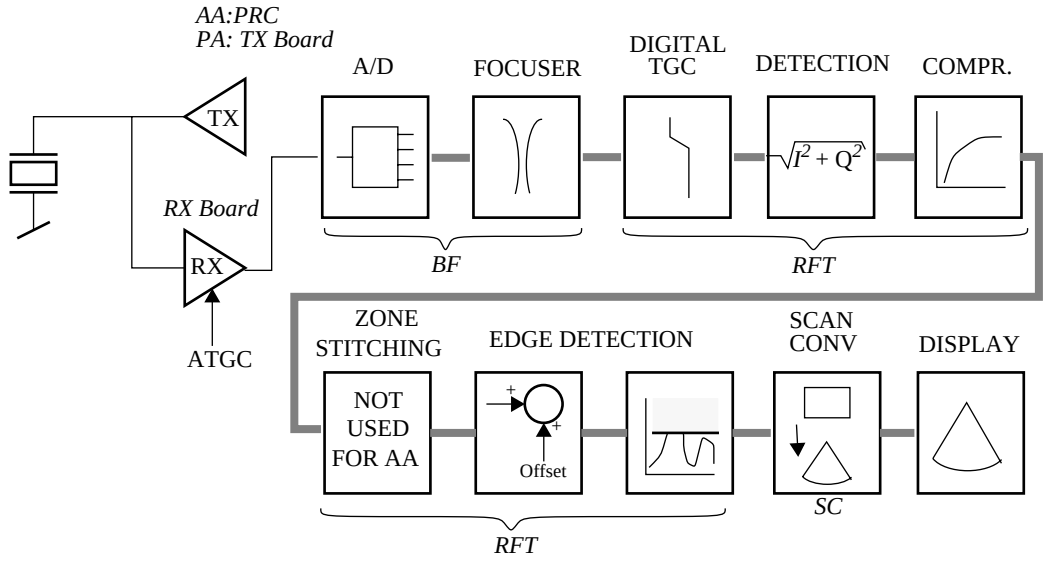

Fig. 4.1 2D Tissue Data Flow

4.2 Detailed descriptions of data processes

The different data processes after focusing and before the scan conversion will be described in this section.

4.2.1 Time Gain Compensation

Because of the attenuation of ultrasound in tissue (~ 1dB/cm MHz), the reflections from tissue at far depths are much weaker than reflections from structures at shallow depths. In order to compensate for this intensity drop, Time Gain Compensation is provided. The amplification is increased with increasing depth. In System 5 there are two types of this: Analog Time Gain Compensation with a 0 - 40 dB range is implemented on the Receiver board. The purpose of this is also to optimize the input voltage to the A/D converters. Digital Time Gain Compensation is implemented on the Tissue Processor board. This is the TGC which is user controlled via slide potentiometers on the front panel.

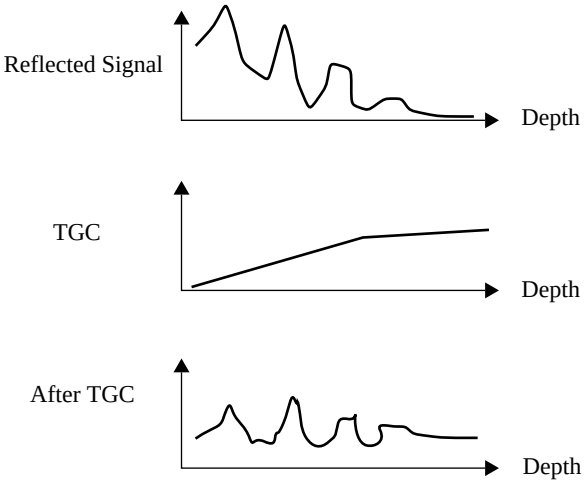

Fig. 4.2 Time Gain Compensation

4.2.2 RF Demodulation

An ultrasound burst with a certain length (a few us) is transmitted from the transducer elements into the body at a certain direction towards the area of interest.
As this burst propagates through the tissue it is attenuated and reflected, and when hitting moving objects (blood cells, leaflets, heart walls etc.), the reflected signal is modulated by the velocities of the objects.

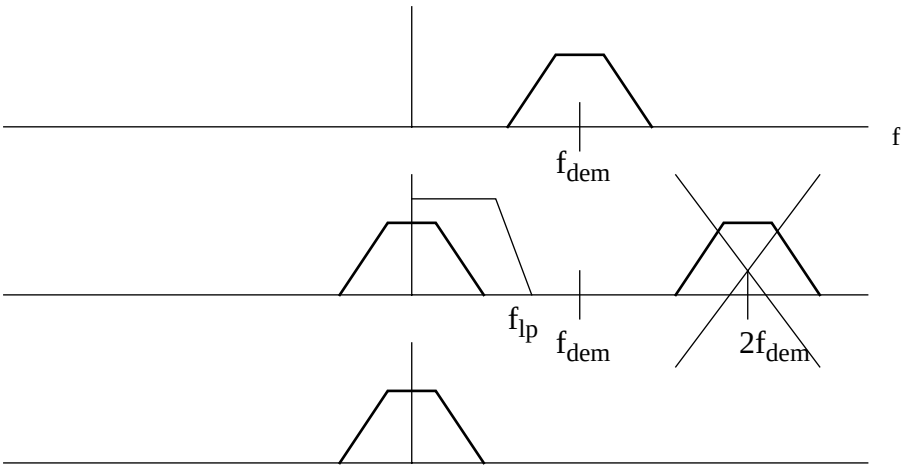

Fig. 4.3 RF Demodulation

RF demodulation or mixing, is a complex modulation with a frequency, f_{dem}, (which may vary with depth) followed by a low pass filter.
- A complex multiplication will move the signal up to 2 times the demodulation frequency and down to the base band.
- The low pass filter will remove the signal wrapped around 2 times the demodulation frequency.

4.2.3 RF filtering

As previously mentioned, high resolution images are obtained using high ultrasound frequencies (sacrificing penetration), and good penetration images are obtained using low frequencies (sacrificing resolution). These two facts are combined on the receiver side by using a so-called swept filter, i.e. after complex multiplication, a low pass filter is swept from a high cutoff at shallow depths gradually down to a low cutoff at deeper depths. An analogy using swept band pass filters is shown in the figure below.

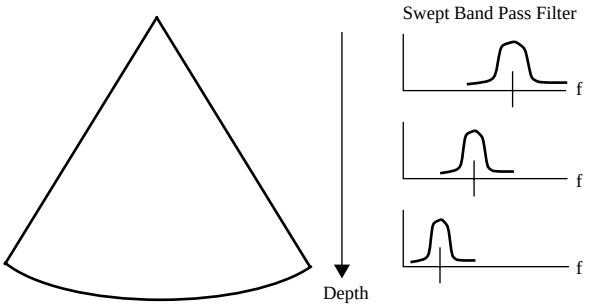

Fig. 4.4 Swept Filter

4.2.4 Detection

Detection (or rectification) is a process where the signal amplitude is derived from the RF signal, i.e. the sign is neglected. In System 5 this is done digitally on the RF and Tissue Processor board by a square root operation of the two-phase components, I and Q.

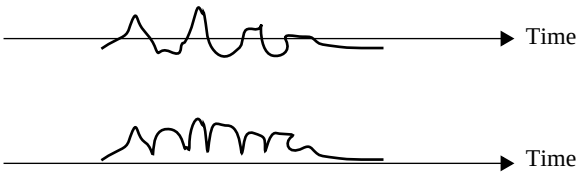

Fig. 4.5 Detection

4.2.5 Compression (pre-)

Detection of a signal is usually combined with compression where low level signals are amplified more than strong signals. This is done to reduce the dynamic range, so that the weak echoes can be visualized together with strong ones. A typical transfer function of a compression curve is shown below.

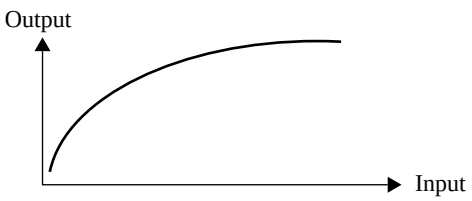

Fig. 4.6 Compression

4.2.6 Composite beam handling / Zone stitching

As one can see from the descriptions on focusing, the transmitted beam has one focal point only, usually placed in the center of the field of view. Better focusing would be achieved if one could combine the received data originating from different beams with different transmit focus points. This can be accomplished in System 5 with so-called Composite Transmit Focusing. Several beams with different focus and different transmit frequency are fired in the same direction (though not consecutively), and the received data is combined in such a way that the focused zones from each beam are “stitched” together. The technique is most commonly used with linear arrays to obtain excellent image quality (sacrificing frame rate). It is also usually combined with swept receive filters.

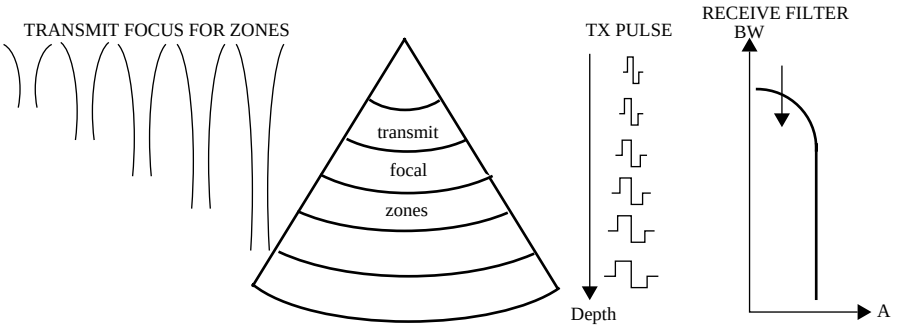

Fig. 4.7 Composite beam

4.2.7 Peak detection and Edge Enhancement

Peak detection is done in order to reduce “black holes” in the image. It is accomplished by comparing two or more consecutive samples along a beam, picking the larger for further data processing.

Edge enhancement is a filter technique where a rapid change in the amplitude of the received signal will be emphasized, thus easier visualizing moving targets and structures (like leaflets). The degree of enhancement will usually be higher in M-Mode.

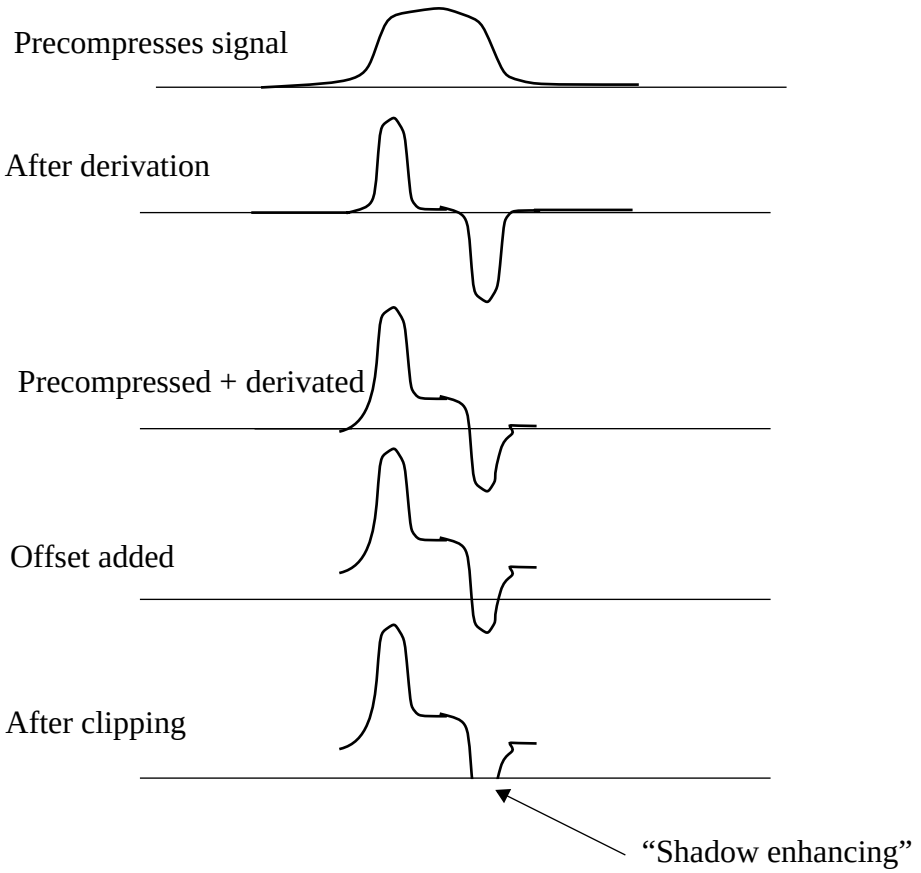

Fig. 4.8 Edge Enhancement

5 Spectrum Doppler Processing

5.1 General Description

When an ultrasound wave is transmitted into the body, the velocity of any moving scatter will be modulated onto the frequency of the transmitted signal. The backscattered signal will have a higher or lower frequency depending on if the target is moving away from or towards the transducer. The frequency shift of the backscattered signal can be derived using the following equation:

$$F_d = 2 F_0 v / c \qquad (5.1)$$

where F_0 is the transmitted ultrasound frequency, v is the scatter velocity and c is the acoustic velocity in tissue (apprx. 1540 m/s). The above equation is valid provid-

ed the angle between the ultrasonic beam and the direction of the blood flow is small, i.e. beam is close to parallel to flow. The ultrasound wave (F_0) is typically in the frequency range of 2 - 7.5 MHz, while the velocities of the moving blood cells are in the range of +/- 0 - 40 kHz. There are two ways of measuring the velocity of the blood cells utilizing the Doppler technique. One is using Pulsed Wave (PW) Doppler and the other is using Continuous Wave (CW) Doppler.

Below is a functional block diagram of the Doppler data flow.

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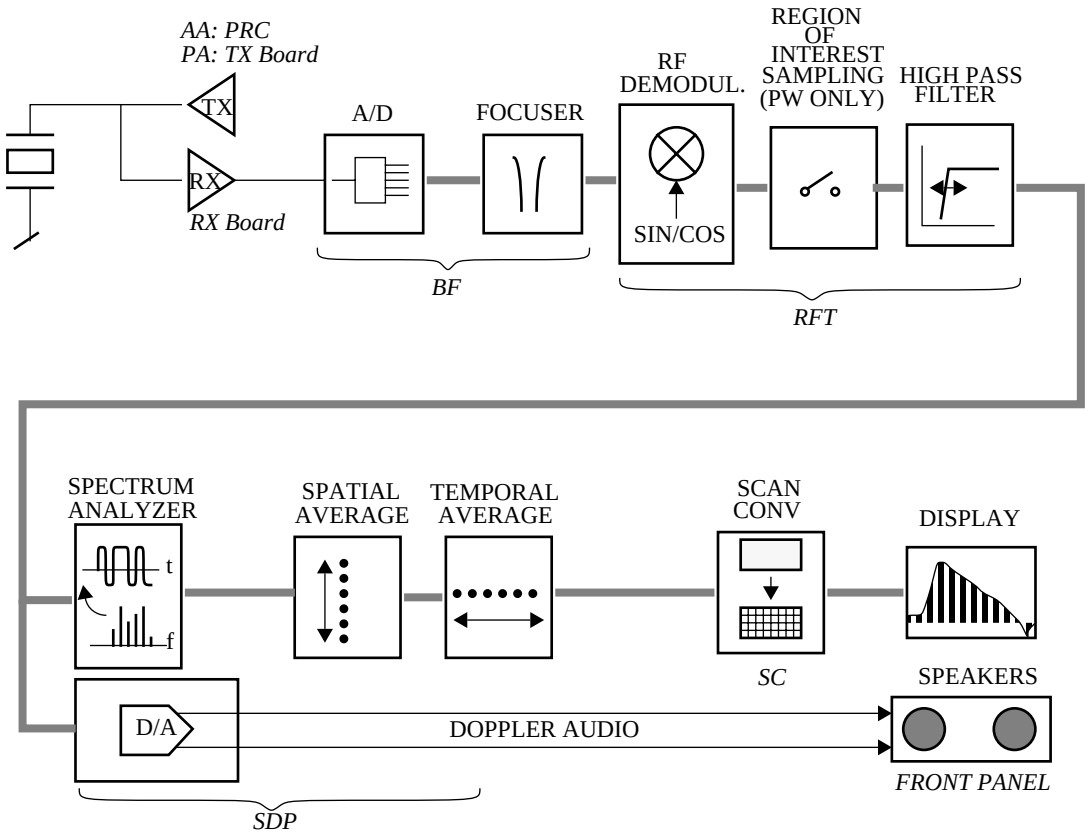

Fig. 5.1 Doppler Data Flow

5.2 Detailed descriptions of data processes

5.2.1 RF demodulation

An ultrasound burst with a certain length (a few us) is transmitted from the transducer elements into the body at a certain direction towards the area of interest. As this burst propagates through the tissue it is attenuated and reflected, and when hitting moving objects (blood cells, leaflets, heart walls etc.), the reflected signal is modulated by the velocities of the objects.

In order to extract the Doppler shift from the backscattered signal, the ultrasound component must be removed. This is done in a process called RF demodulation or mixing and is a complex modulation followed by a low pass filter.

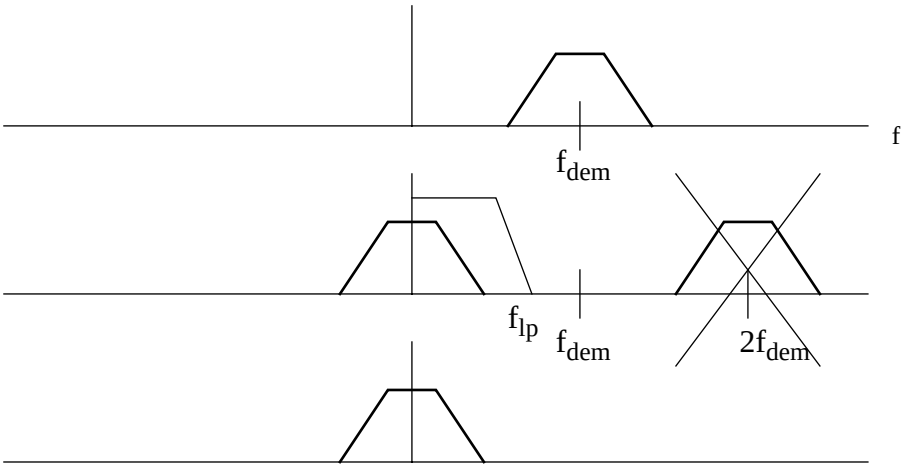

Fig. 5.2 RF Demodulation

A complex multiplication will move the signal up to 2 times the demodulation frequency and down to the base band.
The low pass filter will remove the signal wrapped around 2 times the demodulation frequency.

5.2.2 Sampling in Pulsed Wave (Narrow Band)

Since it takes time for the sound wave to travel from the transducer, down to the target and back up,

$$t = 2d/c,\ t=\text{time},\ d=\text{distance},\ c=1540\text{m/s} \quad (5.2)$$

there is a limitation on how often one can transmit (pulse repetition rate) to avoid having echoes from two transmit pulses at the same time, (Nyquist limit).

The receiver can sample the signal a certain selected time after transmit, called the depth. The size of the sampled blood flow is called the sample volume. Only velocities from this depth is later displayed.

Conventional PW Doppler is limited to measuring velocities below the half the Nyquist limit (or below the Nyquist limit if so-called spectral unwrapping is used (baseline moved up/down)). Velocities above the Nyquist limit will be aliased, i.e. be wrapped around as opposite velocities.

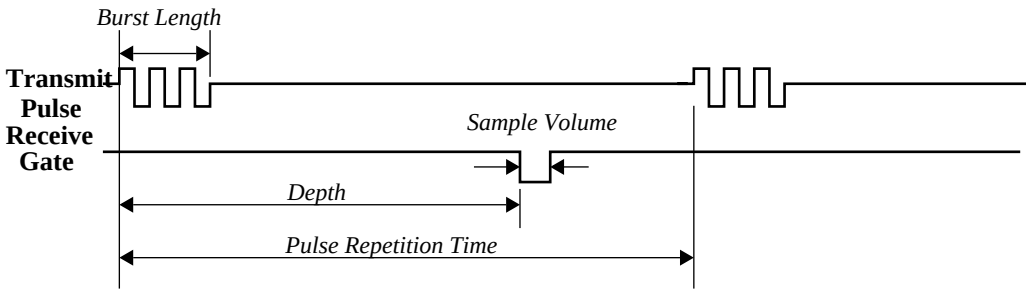

Fig. 5.3 Pulsed Wave Doppler

In high PRF PW Doppler the pulse repetition rate can be much higher than in conventional PW. However, in this mode there are multiple sample volumes located along the ultrasonic beam. This off course causes range ambiguity, since it is impossible to interpret from which sample volume the backscattered Doppler shifts originate.

The PW Doppler technique in System 5 is two-dimensional, where the sample volume is divided into maximum 64 discrete ranges. For each transmit pulse (along the horizontal axis) these 64 ranges can be stored along the vertical axis, thus building up a matrix. In order to incorporate the effect of the scatter displacement from one pulse to the other, the backscattered signals for DFT estimation are picked from different delays (ranges) from pulse to pulse. This is described in more detail in the Spectrum Analyzer paragraph *5.2.5*. This method of performing PW Doppler spectrum analysis makes it possible to measure velocities up to ~7 times the pulse repetition rate without aliasing.

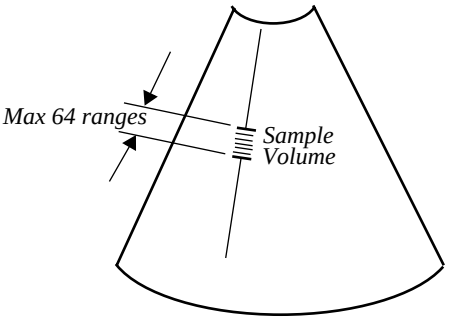

Fig. 5.4 PW Sample Volume

5.2.3 Continuous Wave

In CW mode, the transducer elements are divided into one section for transmit and one section for receive. An ultrasound signal is continuously transmitted into the body and the reflected signal demodulated in the receiver. This mode lacks range or depth resolution (one do not know the location of the different scatters), but the problem with a limited pulse repetition rate does not exist, thereby giving the ability to measure high velocities.

5.2.4 High pass filtering

Before spectrum analysis, the signal is high pass filtered to remove low frequency components. This is done in a variable digital filter on the RF and Tissue Processor board and is also called Low Velocity Reject from a user's point of view.

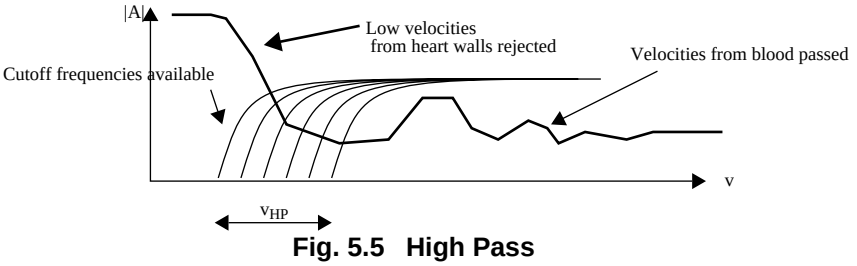

Fig. 5.5 High Pass

5.2.5 Spectrum Analyzer

A modified Discrete Fourier Transform is used to perform the digital spectrum analysis. As mentioned previously, the whole sample volume in PW is divided into maximum 64 discrete samples or ranges, thus there are 64 discrete ranges (making up one sample volume) per transmit pulse. Samples/ranges from maximum 512 pulses are stored in a matrix as shown in *Fig. 5.6*.

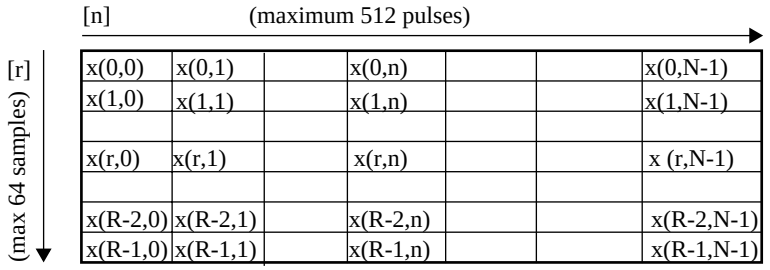

Fig. 5.6 PW Data Storage

By organizing the data in this fashion, the backscattered signal from a scatter will move up or down according to its velocity as time elapses for every new pulse, [n]. Thus, by performing DFT on different slopes where the data is picked from different ranges from pulse to pulse (see example in *Fig. 5.7* below), one can estimate the various frequency/velocity components present within the sample volume.

Assuming in the example below that scatter A is located at depth r_{17} at time t_o, then at time t_1 it has moved to r_{14} and so on. Since both time (pulse repetition time) and distance (derived from range delay) of travel is known, the velocity, v_A, can be estimated, $(r_{17} - r_{14})/(t_1 - t_2)$. Scatter B moves slower, v_B, since it needs the time $t_4 - t_1$ to travel the same distance as scatter A.

There are a total of maximum 256 frequency components (slopes) or velocities which are estimated in the complete spectrum analysis.

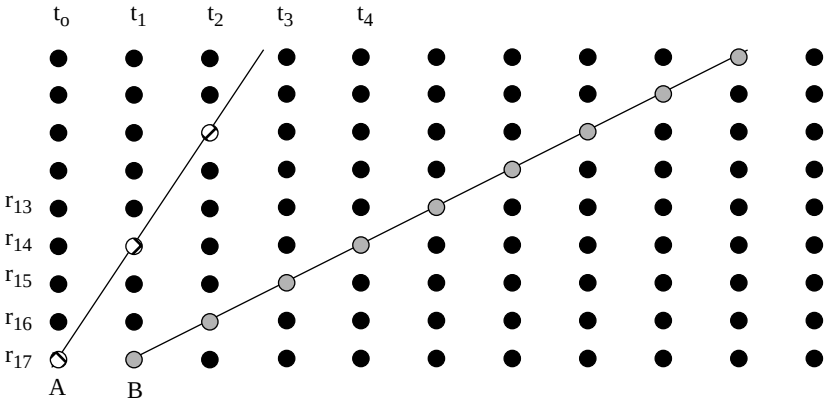

Fig. 5.7 Example

For CW mode the data acquisition is done as a function of time only, i.e. in one range as time elapses.

6 Color Flow Processing

6.1 General Description

2D Flow

In PW Doppler the velocity, intensity (power) and direction of the blood is interrogated within one sample volume utilizing DFT, which is rather time consuming. Thus, this method is unsuited for Color Flow velocity estimation.

Color Flow information is obtained using Multigated Doppler, where the signal from multiple samples along a line are analyzed. Unlike 2D Tissue imaging where it is only necessary to fire one pulse for each direction and then perform sampling along this line, 2D Flow imaging requires firing of several pulses in the same direction, ref. *Fig. 6.2*, and repeated demodulation and sampling of the signal from the same scatterers. This must be done in order to observe the movement of the scatters over time, otherwise it is impossible to tell if they have moved or not. The longer they are observed, the better is the frequency estimation. When sufficient time is spent to gather data in one direction, one can start collecting data from the next.

A functional block diagram (*Fig. 6.1*) shows the complete data flow for the color flow processing, from transmit to display. As for Doppler, the RF signal is amplified, A/D converted and demodulated, i.e. the ultrasound component (F_o) is removed from the backscattered signal. The samples from the region of interest (inside the color sector) are used for processing by the 2D Flow unit.

It is necessary to high pass filter the backscattered signal (so-called Fixed Target Cancelling), due to presence of strong low-frequency components from the slowly moving heart walls, valves and leaflets.

Color M-Mode

Data for Color M-Mode is acquired in the same way as for 2D Flow, with exception that the beam is pointing in one direction only, not scanning. Thus, the same functional data flow diagram (*Fig. 6.1*) and velocity estimation (*Fig. 6.2*) is valid (when all sector shapes are replaced with vertical vectors and rectangles).

The advantages of Color M-Mode over 2D Flow are better accuracy of the velocity estimation and better signal to noise ratio since more pulses can be fired in the desired direction (the probe does not move as in 2D Flow). In addition, this mode provides superior temporal resolution, but the spatial resolution is poor.

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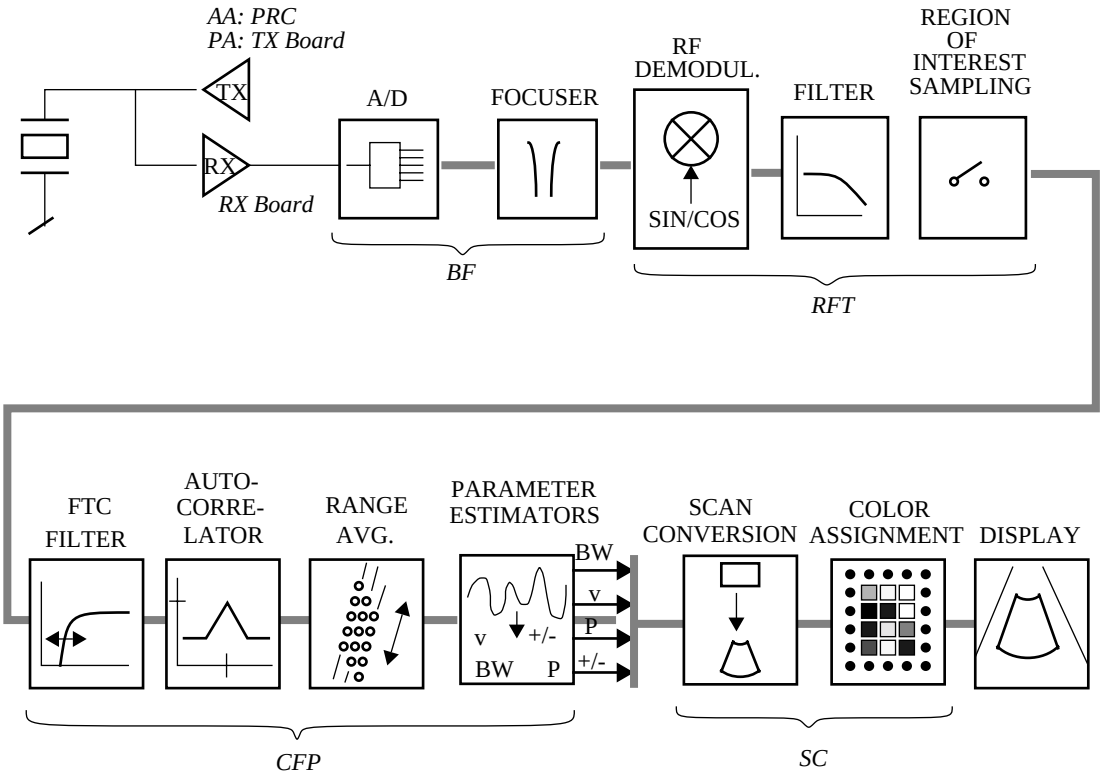
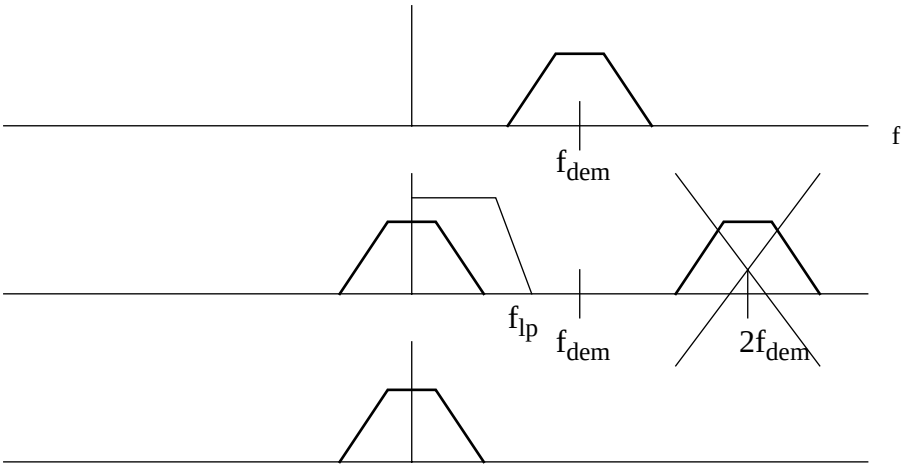


Fig. 6.1 2D Flow Data Flow

6.2 Detailed descriptions of data processes

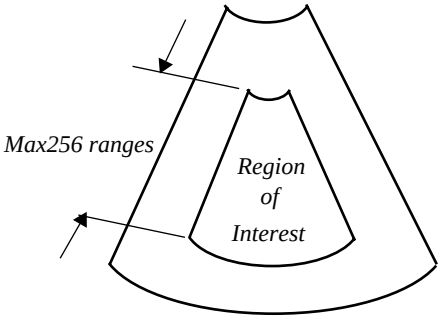
6.2.1 RF Demodulation

This is performed in the same way as for Doppler with a complex multiplication followed by a low pass filter.



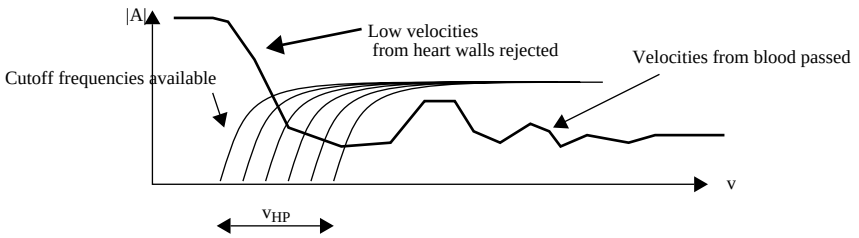
6.2.2 Sampling in region of interest

As mentioned before, repeated data sets from consecutive samples or ranges along a beam is required in order to later perform high pass filtering, velocity estimation and color encoding. Selection of which samples to further process, is actually done by the Front End Controller board enabling the addresses (for the data sets for ranges within the selected color sector) to the RF and Tissue Processor data buffer. Samples originating from outside the boundaries of the color sector, will be neglected.



6.2.3 Variable high pass filtering (Fixed Target Cancelling)

Samples from the same ranges at different time intervals are stored in a memory, so that they can be used for estimation of the velocities within each range. Velocities below a certain user selectable limit (Low Velocity Reject) are rejected in a variable digital high pass regression filter, which “on the fly” first generates a curve of the low -frequency components, then subtracts the curve from the signal to separate the high-frequency components.



6.2.4 Autocorrelation and Range Averaging

Given a range, r_n at a certain depth with the transducer element pointing all the way to one side (at line # 0). The sampled values in this range will vary with time (from t_o to t_N) according to the scatters within this area as shown in a). These samples are stored in a memory as shown in b), as well as samples from any other range at the same time intervals (prt). By comparing the data from this range with the neighbor ranges in a so-called autocorrelator, estimates reflecting movement of blood can be obtained. In order to axially smoothen the color vectors, range averaging of the autocorrelation values is performed.

6.2.5 Frequency Parameter Estimation and Color Encoding

Three different estimators use the autocorrelation values to estimate the velocity, power and bandwidth of the signal. The results are computed in signal processors. Two different color coding schemes are used to map the parameter estimates in a two-dimensional display (c):

Power/frequency map: The color intensity is modulated with signal power and center frequency determines color hue.

Bandwidth/frequency map: The center frequency is mapped in red-violet-blue for low bandwidth signals, gradually changing to green for higher bandwidths.

The above mappings are used as the basis for the displayed color in the particular pixel (picture element) corresponding to the position of that range (after scan conversion) (e).

Intelligent mapping used together with an advanced algorithm for autocorrelation features a color coding without aliasing or wrap-around for frequencies above the Nyquist limit.

As time elapses and the flow line position is changed, the above process is repeated (d) for each range in each flow scan line until the transducer element points all the way to the other side (e.g at line # 63 for AA probes) and one complete color frame has been generated.

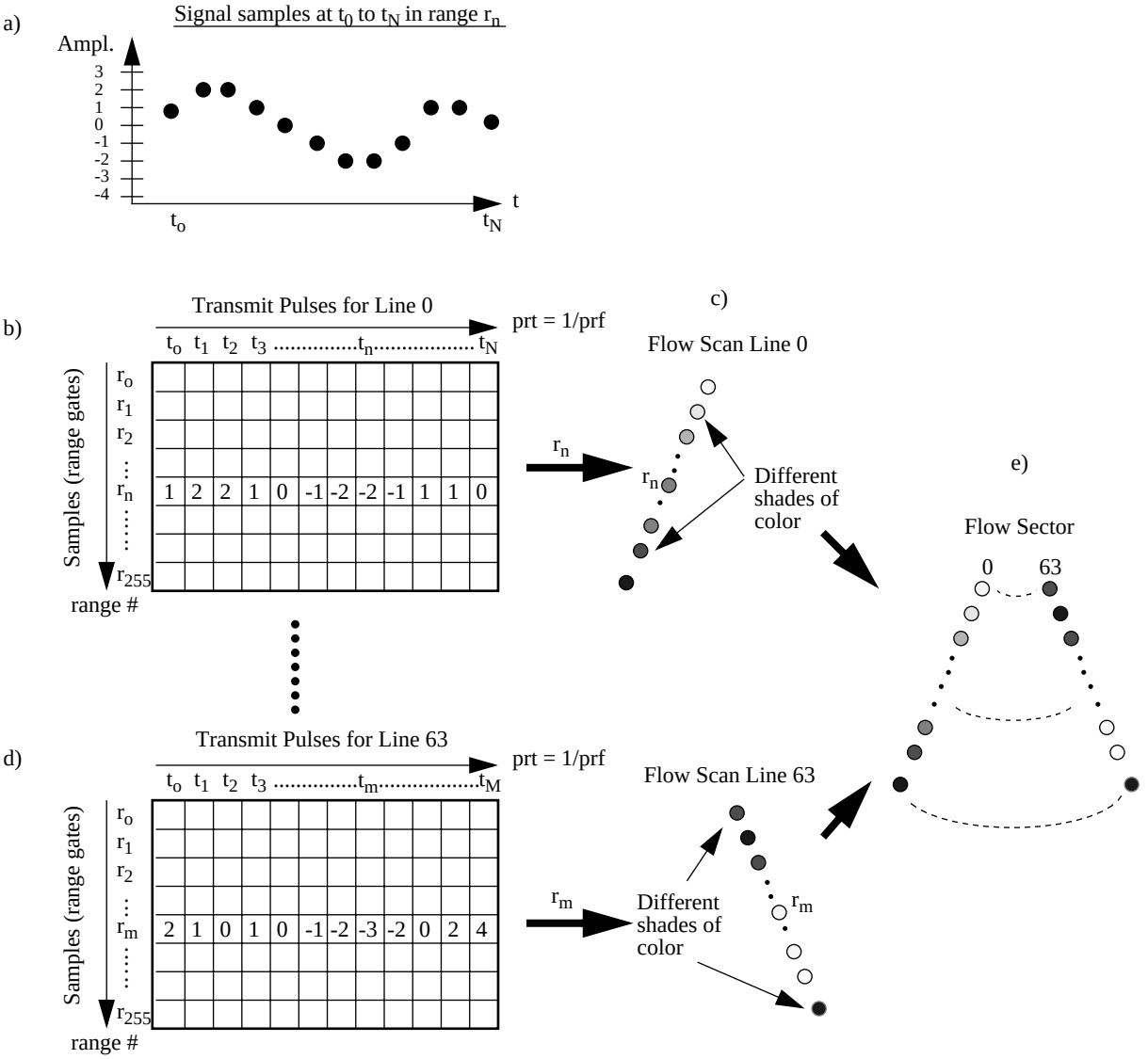


Fig. 6.2 2D Flow Velocity Estimation

7 Post Processing

7.1 Recursive Filtering

In order to reduce random noise in the image, recursive filtering (or temporal averaging) is performed. This is averaging of data located at the same pixel position from frame to frame. Signal from structures will be present from one point in time to the other, while noise usually will appear once, and will be averaged out over time.

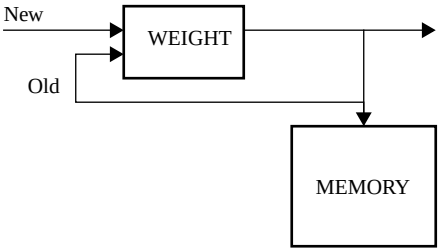


Fig. 7.1 Recursive Filtering

7.2 Scan Conversion

The main purpose of the scan conversion process is to convert the image data stored in a rectangular format in memory to a geometrical correct image on the monitor, i.e. the data has to be presented on the screen in the same format as it was acquired (e.g. in sector shape for AA or PA probes). This is done by converting the x and y addresses from the pixel domain to r and theta addresses in the angular format. These r and theta addresses are used as inputs to the memory. The pixels are given a grey scale (for tissue/Doppler) or a color (for flow) value which depends on the data stored in the memory.

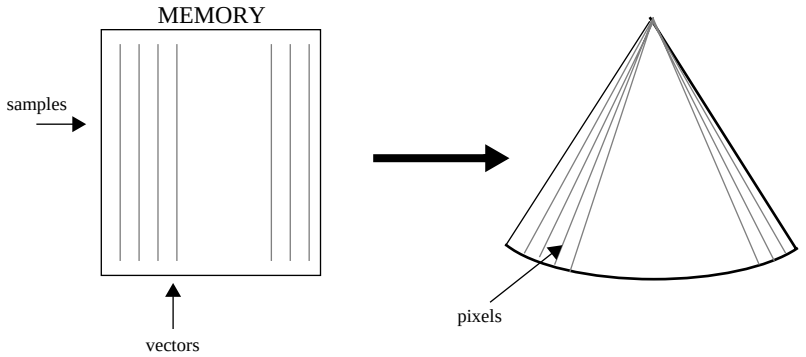


Fig. 7.2 Scan Conversion

7.3 Interpolation

It is not very likely that a sample in the r/theta format coincides with the accurate position of the pixel, thus, somehow they have to be aligned. Also, the value of the pixel will depend on the values of several surrounding samples, not only the closest. This is accounted for by bi-linear interpolation where 4 neighboring samples (two in r- and two in theta direction) are simultaneously read out of memory and weighted to calculate the pixel value.

It is quite obvious that there are far to many horizontal samples stored in memory for shallow depths, compared to the number there are room for in the near field of a sector shaped image. Thus, a lot of samples are “thrown away” during interpolation. In the far field there are not enough horizontal samples, and interpolation is used to generate pixel values based upon information from neighboring samples.

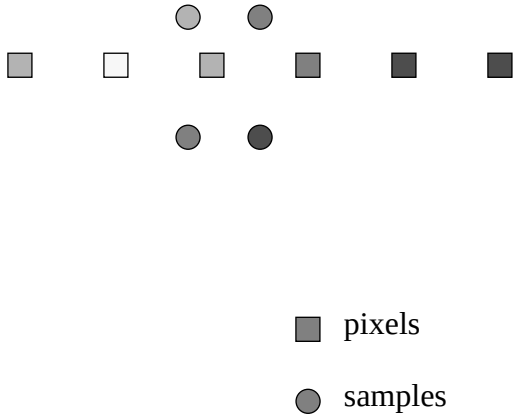


Fig. 7.3 Interpolation

7.4 Compression and Reject

All though there is a compression of the signal prior to scan conversion, there is also compression and reject after the scan converter. As mentioned before, compression will enhance low level echoes on behalf of strong signals, while reject will suppress noise.

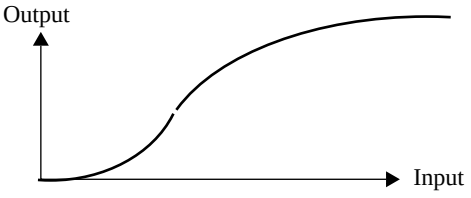


Fig. 7.4 Compression/reject

7.5 Arbitration

An arbitration algorithm takes care of the priority between grey scale and color code in 2D Flow imaging, where the two has to be blended in such a way that the color information is correctly superimposed on to the black and white tissue information. Since a pixel can only be of one data type, both tissue and flow data are weighted and the greater is selected as the output pixel.

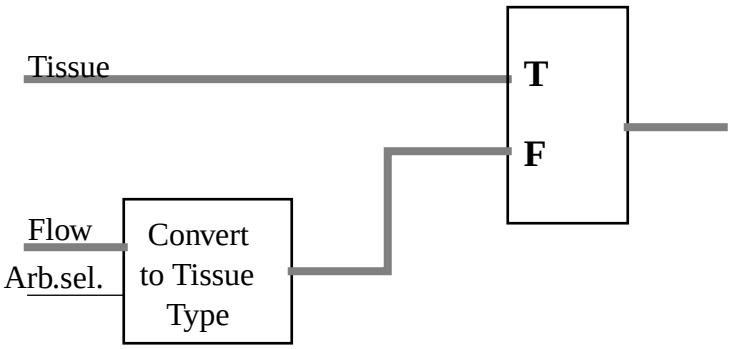


Fig. 7.5 Arbitration

System Description – rev. 07

8 Introduction

8.1 Overview

The purpose of this document is to give a system overview, with special emphasis on data flow from the probes to the monitor. A block diagram, *Front End and Mid., rev. 10* on *page B1-3*, is used as a reference for the description starting with:

- *9: General Information*. The system is divided conceptually into four functional blocks;
- *10: Front End*,
- *11: Mid Processors*,
- *12: Display and Control* and
- *13: Keyboard, I/O and Peripherals*.

8.2 Document History

Rev.	Date	Sign.	Description
01	25 Aug 1994	GRL	First version.
02	2 Jan 1995	LHS	Updated layout. Corrected some minor errors.
03	21 Aug 1996	GRL	Minor corrections, added descr. of HV supply
04	28 Feb 1999	LHS	Updated and corrected some errors.
05	9 Sep 1999	LHS	Some small changes to reflect that the Image Port 2 Board has been introduced.
06	18 Oct 1999	LHS	Corrected errors. Updated to include changes from sw. 1.7.1, RX64 has been introduced.
07	1. Oct. 2000	LHS	Corrected errors.

9 General Information

- System FiVe is a phased and linear array ultrasound imaging scanner with an option for mechanical annular array probes. The system is universal and can be used for a number of various applications; all a matter of software.
- The system can do 2D black and white imaging, 2D Color Flow, M-Mode black and white imaging, Color M-Mode and Doppler, in addition to a number of combinations of the above. It also has provisions for several analog inputs (e.g. ECG, phono).
- System FiVe is a digital beamforming system which can handle up to 192 element linear probes by use of multiplexing.
- System configuration is stored on a hard disk and all necessary software is loaded from the hard disk on power up.

- User interface via the keyboard initiates the system operation and set-up via two major bus structures interconnecting the different printed circuit boards residing in the card cage.
- Signal flow from the input connector panel to the monitor and peripherals is mainly done over a backplane, but the final path from the I/O section and up from the card cage is done via cables.

10 Front End

10.1 General information

The System FiVe Front End consists of the following boards:

- Relay Board (RLY),
- Transmitter Board (TX),
- Receiver Board (RX),
- Probe Controller Board (PRC),
- Beamformer Boards (BF) 4x
- Front End Controller Board (FEC).

It presents a digital representation (18 bit) of the backscattered/reflected signal from blood and tissue to the Mid Processor section.

10.2 Front End Bus

Most of the FE boards are controlled by the Front End Controller board via a Front End Bus (FE_BUS). The FE_BUS is a synchronous and bidirectional bus built up by 16-bit data, 6-bit device address select, 10-bit page address and 8 strobe signals controlling the data transactions. The Front End Controller board can also read the revision status of the Front End boards through a serial line to a E^2PROM located on each board.

10.3 Phased and Linear Array Front End

- The phased and linear array probes consist of several identical transducer elements (e.g. 64, 128, 192). Three probes can be connected to the system. The connectors are physically located on the RLY board, where one of them is selected and connected to the transmitter (TX) and receiver (RX) through a number of relays.
- Depending on probe type and system setup, a certain scan pattern is selected on the FEC board. This board loads scan parameters for both the transmitter and the beamformer (steering- and focusing delays) into local RAM on these boards. Thus, when the FEC board goes through a scan sequence, it loads the proper contents of the RAM into the TPG, then issues a transmit trigger pulse (TXTRIG_L) for the transmitter and a receive synchronization pulse (SYNC_L) for the beamformer. By firing the transmit pulses from the different elements at certain repeated time intervals and with different delays, the ultrasound beam can be steered in desired directions (re. principles of operation) obtaining the selected scan patterns (e.g. 2D, 2D Flow etc.).

- The ultrasound transmit bursts are generated on the TX board, initiated by the transmit trigger pulse (TXTRIG_L). The transmit trigger starts the Transmit Pulse Generators (TPG) on the TX board, each generating 16 transmit pulses with different delays. The transmit pulses are then routed to separate transmit “amplifiers” fed with voltage HV1 and HV2 witch are controlled by the Acoustic Power control software.
- The transmit pulses are routed over an Xducer Bus Board (XDBUS) located on the front side of the Front End boards, to the Relay board, where they are fed to the selected (one out of three) phased/linear array probe.
- The reflected signal from body structures and blood cells are routed from the probe, via the Relay board over the Xducer Bus to the RX (receiver) board, where preamplification (20dB) and Analog Time Gain Compensation (ATGC) (-10 - +30 dB) is performed. Gain is determined by an analog signal (ATGC) generated by the FEC board.
  On the very input of the RX board are transmit/receive (T/R) switches to prevent the transmitters from destroying the receivers. Prior to preamplification the signal from the different channels is also fed through relays. This is for having the possibility to route echoes from annular array probes into the receiver, in addition to injecting a test signal, TSIG.
- The output channels from the RX board are fed to four Beamformer boards. Each Beamformer board performs A/D conversion of 32 channels. Then the sample outputs from four A/D converters are fed to one Focusor ASIC. The samples in the four channels are individually delayed (to focus at a certain depth) and weighted (so-called apodization) before summed to one channel. The sample outputs from four Focusors are summed to one channel in a so-called Beamadder ASIC (level 2) (BAL2) while finally the outputs from two BAL2’s are added together with the output from the preceding Beamformer board (if existing) in a Beamadder ASIC (level 3) (BAL3). The output from Beamformer 1 (sum of 32 channels) is fed to Beamformer 2 where it is added to the sum of the 32 channels on Beamformer 2. This summation goes on through all four Beamformer boards until all 128 channels are summed making up one sample focused at a certain depth. The next sample is then focused a little deeper and so on, until one vector is made up. Before the next transmit trigger pulse is fired, new delay parameters are loaded from VRAM into the Focusors so that they can focus in a new direction and/or depth.
- In order to process two vectors simultaneously (Multi Line Acquisition), a second set of Focusors and Beamadders can optionally be mounted on the Beamformer boards.
- As mentioned before, the Front End Controller board controls all Front End boards. The board loads all parameters to the TX and Beamformer RAMs, it reads the probe identification, selects probe connector on Relay board and controls the high voltage multiplexer in linear probes. In addition the board generates the transmit trigger pulse for TX, a receive synchronization pulse (SYNC_L) used by Beamformers and RF & Tissue Processor, a differential ATGC voltage used by RX and control signals for the High Voltage Power Supply (HV POWER). The Front End Controller board also generates the global 40 MHz system clocks and reset pulse (SRES).
- The output of Beamadder level 3 at BF4 is fed to the RF and Tissue Processor Board (RFT).

- Front End can be configured with the RX board. RX64 supports 64 receive channels. Implementation equals the RX128 receiver. The RX64 board has multiplexers in addition to handle linear arrays containing more than 64 elements.

10.4 Annular Array Front End

The annular array probes consist of maximum 5 elements which can fire transmit pulses independently, forming an ultrasound beam. Depending on type of mode, the beam is steered in desired direction with the use of a linear motor controlling a mechanically movable transducer.

- A Motor Controller (XDCTRL) and a power amplifier for the APAT probes is located on the PRC board. A scan sequence is started by the system CPU telling the XDCTRL to start a sweep.
  Communication between the CPU and the XDCTRL is done over two serial lines, TXD1 and RXD1. A motor signal is applied to the motor coil in the probe, and a position signal is fed back to a position sensor, thus forming a regulator loop. When the element is in the desired position, the XDCTRL issues a tissue line request signal (TLREQ_L) indicating that now it is time to fire the transmitter. This signal is fed to the FEC board, which immediately (after synchronization) fires the transmit trigger (TXTRIG_L).
- This transmit trigger pulse is fed to the PRC board, and it initiates a transmit sequence in a Transmit Pulse Generator pre-loaded with delay-, frequency- and pulse width parameters. The same parameters are used throughout a scan (i.e. one frame). The TPG outputs 5 transmit pulses which are routed to 5 transmitters fed with high voltage (HV1 and HV2). For Stand Alone Doppler probes, channels 7 and 8 are used.
- The transmit pulses are routed to the Relay board via the Xducer Bus board. Here they are fed to the selected (one out of two) annular probe, or directly to the Stand Alone Doppler probe.
- The reflected signal is fed back to the RX board where relays on the input feed each of the 5 annular channels into 16 receiver channels. Same signal conditioning is done to the signal as for the phased/linear array probes.
- The 80 (or 64 or 32 depending on # of elements in AA probe) active channels (5 * 16, 4 * 16, 2 * 16) are fed to the Beamformer boards for receive focusing. Multi Line Acquisition is not possible with annular array probes.
- The output of Beamformer board 4 is fed to the RF and Tissue Processor Board (RFT).

10.5 Isolated inputs (incl. ECG and Phono)

ECG-, Phono-, Pressure- and Respiration sensors can be connected to the Patient I/O board. Dedicated preamplifiers and filters are designed for each of the sensor types. The analog signals are multiplexed, gain controlled and A/D converted (serial output) before fed through opto-couplers (for isolation) to the Internal I/O board. A DSP interface forwards the trace data to the Spectrum Doppler Board, which presents traces on the pipelink bus to the Image Port or the Image Port 2.

10.6 High Voltage Power Supply

The transmitters on the TX board and PRC boards are fed with high voltage from the HV supply. This module consists of three linear power supplies; one providing a symmetrical output voltage ranging from 0 to +/- 80 V (HV1), the other providing a voltage ranging from 0 to +/- 40 V (HV2) and the third outputting +/- 80 V for the multiplexers in the linear probes. HV1 and HV2 are programmable through a serial interface from the FEC board.

11 Mid Processors

The System FiVe Front End and visualization system are interconnected through digital signal processing modules, called the Mid Processors. These processors performs the adequate signal conditioning for the different data types; Tissue, Doppler and Flow. The current Mid Processors are the RF & Tissue Processor board (RFT), the Spectrum Doppler Processor board (SDP) and the 2D Flow Processor board (CFP or 2DF).

11.1 Pipelink bus

- The Mid Processors are interconnected through a data bus system called the Pipelink. This is a unidirectional bus transporting data from the pipelink dispatcher (RF & Tissue Processor) through the accessed processor to the destination, the Image Port. The Image Port will then map the data into the Image Memory.
- Data leaving the RF & Tissue Processor have a tag indicating what type of data that is transported; e.g. tissue, Doppler, 2D Flow. Each of the remaining mid processors decode this tag and when it matches their own address, the data is processed. Data that doesn't have a matching tag, is passed on to the next processor.
- In 2D, data is typically transferred in vector blocks from the RFT board. In spectrum Doppler and Color Flow, data from one range gate is transferred.

11.2 RF and Tissue Processor (RFT)

The RF & Tissue Processor board receives its data from the Beamformer 4 board in the Front End. Both type of data and what data samples (RF_MODE) to use are communicated to the RFT board from the Front End Controller board (over the Front End Bus).

RF Processing

Different types of RF processing can be performed depending on later usage of the data; e.g.:

- RF Demodulation
- Digital Time Gain Compensation
- Filtering
- Decimation.

Data Buffer

After RF filtering, the data is written into different sliding ring buffers, dedicated the different types of data. While data is written into the buffers sample by sample in vec-

tors, multiple samples from the same range (depth) can be read out. Both input addressing (start and length) and output addressing (through output events) is controlled by the Front End Controller board.

Tissue Processing

A number of different tissue processes are performed on this board: First the signal amplitude is obtained by detection. Then the data is compressed to attenuate the strong signals and amplify the low level echoes. After compression so-called zone stitching is performed. This is used to combine the (transmit) focal zones from different vectors into one vector by weighting the zone transitions, and does only apply to phased/linear array probes where multiple vectors can be collected in the same direction. For M-Mode, peak detection and edge enhancement is implemented. Finally an offset can be added to the signal and clipping is performed. The tissue data is then tagged, and sent on to the Image Port board.

Color Flow Processing

No Color Flow processing is performed here, except for the RF demodulation previously mentioned. The data used for Color Flow is tagged with the appropriate headers and tails and routed through an output multiplexer to the 2D Flow Processor board.

Doppler Processing

In addition to RF demodulation, a variable digital high pass filter is implemented on the RFT board.The purpose of this filter is to remove strong low frequency signals returning from wall motion, valves and leaflets. The filtering is performed by the local DSP. Data is then tagged and sent to the Spectrum Doppler Processor board.

Control

The RFT board has a local Digital Signal Processor (DSP) with an external EPROM.The DSP performs multiple control tasks:

- It handles communication with the System CPU over the VME bus.
- It updates filter coefficients and other parameters in the data path.
- When output events from the Front End Controller is received, it sets up the pipelink output control for data tagging and transfer.
- During transfer of time motion data, it sets up a so-called time-slot data transfer (which replaced the output event based transfer).

11.3 Spectrum Doppler Processor

The Spectrum Doppler Processor board (SDP) receives its data from the RFT board. In Pulsed Wave (PW) Doppler several sets of data from the same range (depth) originating from different transmit pulses are transferred from RFT data buffer. In Continuous Wave (CW) Doppler the data samples are transferred consecutively.

Spectrum Analysis

The data sets are written into a sliding ring buffer with different ranges along the vertical axis and different transmit pulses along the horizontal (time) axis, thus achieving a two-dimensional matrix. By reading the data out of the buffer in a certain way (re. Principles of Operation) and performing Discrete Fourier Transform on the data, velocities up to seven times the pulse repetition frequency (in PW) can be displayed. Parts of the spectral analysis is done by a digital signal processor (DSP1).

During Duplex modes (e.g. 2D and Doppler) the gaps in the spectrum (when doing 2D) is filled by stretching the “real” spectrum out to fill the missing time.

Audio

The Doppler audio channels (I and Q, or DOPLA and DOPLB) are generated based upon the digital data stored in the ring buffer. The data is transferred from the buffer into DSP2 (Digital Signal Processor no. 2) which controls the D/A conversion as well as the Missing Signal Estimation of audio in Duplex modes.

Trace Interface

A serial link from the Internal I/O board, feeds several A/D converted traces (like ECG, phono, pressure) into the Spectrum Doppler Processor board.

These traces as well as spectral data, are tagged and transported over the pipelink to the Image Port under control of DSP1.

Control

The DSP1 controls the data flow and updating of all parameters, including control of read/write address generation. It communicates with the System CPU over the VME bus and provides the pipelink output with spectrum and trace data.

11.4 2D Flow Processor

The 2D Flow Processor board receives its data from the RFT board. Several complex data sets for the same range originating from different transmit pulses are transferred over the pipelink bus, then data sets from the next range are transferred and so on. The purpose of the board is to convert the demodulated Doppler signal to color coded values that can be presented to the Scan Converter board.

The different functions and calculations on the board are performed in a total of 21 Digital Signal Processors. These are grouped in four identical groups each built up as follows:

- Four DSPs (FTC DSPs) performing fixed target cancelling and autocorrelation.
- One DSP (VEL(ocity) DSP) performing range averaging and frequency parameter estimation.

The purpose of having four groups is to have parallel processing giving increased through-put rate. The 5 DSPs in each group are supervised by a master DSP on several serial lines.

The data is received by an Input Dispatcher which checks the tags of the pipelink data. Data without 2D Flow tags are passed on directly to the output (bypassed), control information is transferred to the master DSP, and data is distributed to the four DSP groups which each can handle 128 range gates (totalling 512 range gates per vector). The Input Dispatcher also keeps track of beam and range numbers.

Fixed Target Cancelling

Data from the input dispatcher is stored in FIFOs before transferred into the FTC DSPs under DMA control. Here, fixed target cancelling is performed for each range. Each DSP processes data from 32 ranges. The input parameters and program executing the filter algorithm has previously been loaded into the processors from the master DSP.

Autocorrelation

After filtering, the autocorrelation functions for each range is estimated in the same DSPs as fixed target cancelling is performed. The outputs (related to signal power and velocity) of the 4 FTC processors in a group, are sequentially latched out to the VEL DSP via external RAM, also under DMA control.

Range Averaging

The autocorrelation numbers received from the FTC DSPs are first averaged in a recursive manner, i.e. data from a certain number of ranges along a vector are averaged by adding and division, then one element is added on top and one element is subtracted in the bottom and another add/divide is done. This is repeated for all ranges along each beam.

Frequency Parameter Estimation

The averaged autocorrelation numbers are used as inputs to three estimators computing the velocity, the bandwidth and finally the power (or intensity) of the signal in each range gate. The first two are found with the help of look-up tables stored in external RAM, the last is calculated. As for the FTC DSPs, the programs for both averaging and estimation has previously been loaded into the VEL DSPs from the master DSP.

Output Processing

The 3 estimates from each of the 4 VEL DSPs are transferred through FIFOs to the master DSP. Here they are first packed in 16 bit words (power-4bit + velocity-8bit + bandwidth-4bit = 16 bit), then the 16 bit words are organized in a beam (or vector) and fed out on the pipelink through an output FIFO.

Control

As mentioned before, the Master DSP controls both the FTC- and VEL DSPs serially. It also organizes the data from the VEL DSPs and writes the vector data out on the pipelink bus after having tagged it with head and tail information. In addition, it communicates with the System CPU board over the VME bus, and handles error situations and test facilities.

12 Display and Control

The Display and Control block takes the data from the pipelink bus, stores it in a memory, performs scan conversion to pixel domain and drives the system RGB monitor.

The boards within the Display and Control block are:

- the Image Port board,
- the Image Memory board,

or

- the Image Port 2 board, replacing both the Image Port board and the Image Memory board
- the Scan Converter board,
- the Graphics board
- the System CPU board.

12.1 Image Port

(Image Port 2 has the functionality of the Image Port board plus the Image Memory board on one card).

The purpose of the Image Port is to capture signal processed data from the Mid Processors or video data from the VCR, and route this data to the appropriate locations on the Image Memory.

Data from Mid Processors

Data from the Mid Processors are transferred over the pipelink in data packages called Frames, Packets and Tuplets, all depending on size of the package. At the Image Port the Packet is collapsed. A Frame contains enough data to construct one frame (e.g. one 2D frame), while one Tuplet contains enough data to construct one vector (e.g. one Color vector). The size of the vectors will depend on data type. The Image Port demultiplexes the different types of data, groups the same types and maps them into the proper ring buffers in the Image Memory located on the Memory board or included on the Image Port 2 board.

Data from VCR

Video and S-VHS (both in PAL and NTSC format) from the VCR (or another video source) is first digitized and then fed through a video multi-standard decoder providing decoded luminance (black and white) and chroma (color) data. Data is then transferred to a ring buffer in the image memory where it later can be fetched by Scan Converter for display on the system monitor.

12.2 Memory

The default size of the Image Memory is currently 64 MByte. The Image Port board is the data source and the Scan Converter and System CPU boards are the data destinations. The different data sets that can be stored, are the following:

- 2D Tissue data
- Doppler data
- M-Mode Tissue data
- 2D Flow data
- M-Mode Color data
- Trace data
- Video Luminance data
- Video Chroma data
- RF data

Up to eight of the above data sets can be stored live simultaneously in the Image Memory in eight different ring buffers.

12.3 Scan Converter

The Scan Converter board fetches the different types of data from the Image Memory using VME DMA transfers. Its main purpose is to convert the data stored in the image memory to a display format which gives a true view of what was actually scanned.

Time Domain Processor

Address and data is multiplexed, pipelined and fed through input FIFOs into a so-called Time Domain Processor (TDP). The FIFOs can hold up to two vectors each containing 1024 samples. The TDP performs recursive filtering of the data which is still on a sample/vector format, and stores the data in one of three memory banks depending on data type. The three banks are for simultaneous storage of tissue data, flow-frequency data and flow-bandwidth data.

Space Domain Processors

The different types of data are now stored in separate memory banks, and can be read out in three parallel paths for further simultaneous processing in the Space Domain Processors (SDP). It is when addressing these memories that the actual scan conversion takes place. Each of the banks have separate addresses since the output formats/shapes are different for e.g. a 2D Tissue sector and a 2D Flow sector. The addresses to the memories are derived from the CRT x and y counters and the selected format shapes.

- Sector for 2D tissue and 2D flow (phased array and annular array probes).
- Rectangle for tissue and parallelogram for color (linear array probes).
- Rectangle for tissue, M-Mode tissue, M-Mode color, spectrum, traces, video.
- Parallelogram for both 2D tissue and 2D flow.

Samples are read out four by four in three parallel paths. Four samples are first mapped through compression PROMs before they are used for interpolation of the value of the closest pixel. There are different interpolation filters for tissue, flow-frequency and flow-bandwidth. The interpolation scheme for the flow-frequency component is done in such a way that frequency aliasing is avoided. The output of the interpolator is fed to a pixel encoder.

Pixel Encoder

The different data types have different encoders or look-up tables to get from data codes to RGB. After conversion to RGB, all data types are input to a multiplexer, where only one type can be output at the time (pixel by pixel).

Video information (back from the VCR) which is demodulated by the Image Port and stored in the Image Memory, can also be fed through the Scan Converter board. Video is stored as digital luminance and chrominance, and is fed through an encoder and converted to digital RGB.

Tissue data is fed through RAM based look-up tables for the purpose of compress and reject functions. The outputs of the RAMs are three 8-bit R, G and B paths fed to the output multiplexer.

Color Flow data (frequency and bandwidth) is fed to an arbiter where it is compared to the tissue signal. Depending on the weight of the flow signal, either tissue RGB or flow data (which also has been fed through a RGB look-up table) is selected as the output pixel through the multiplexer.

Before pixel data is presented out on the Pixel Bus, it is multiplexed with the pixel address.

12.4 Graphics Buffer

The Graphics board gets its data from the Scan Converter board over the Pixel bus which is a high speed bus providing 24 bit “true color” (8 bit each for R, G and B) at a burst bandwidth of 20 Mpixels /second. The bus is both writable and readable.

The board can drive two independent monitors, one high-resolution main screen and one video monitor (or VCR); the screen formats can range from 640*480 to 1024*1024 pixels. Data from the pixel port is demultiplexed and fed to four banks of video RAMs providing a 24 bit underlay for imaging.

From the VME interface, two separate overlays are provided. One overlay is for the windowing system, and the other is for video.

The Graphics board supports a window system server.

Both PAL, NTSC and S-VHS outputs are provided for VCRs and printers.

The board records tape status from the VCR to ease searching for specific recordings.

12.5 System Control

The System CPU board supports the VME controller function and provides the software resources for computation and real time control. It has provisions for different interfaces, like SCSI to hard disk, floppy disc and optical disc, RS232 to VCR and XDCTRL, ethernet, and parallel interface to laser printer.

13 Keyboard, I/O and Peripherals

Miscellaneous functions are located in the last system block. The Internal I/O board and External I/O board are the interfaces between the card cage and the rest of the system, including the Front Panel and the Peripherals.

13.1 Internal I/O and Peripheral Control

The Internal I/O board performs buffering and distribution of video and control data from various sources inside the card cage to multiple destinations. The board also contains a VME Interface and can thus generate its own control signals and read the status of peripherals.

- R, G, B and Sync are fed from the Graphics board, directly up to the system monitor. Another set of RGB can be fed to a color printer.
- Composite video, black and white video and S-VHS video are buffered and distributed to VCR and printers.
- The analog Doppler signals are fed from the Spectrum Doppler board to the VCR audio inputs and through a switch where audio from VCR playback also is input, up to the audio amplifier and then to the speakers.
- A parallel port is generated on the Internal I/O board, where data to e.g. a laser printer can be output.
- Serial RS-232 interface signals from the System CPU and the Graphics board are fed to the destinations; Front Panel Interface, VCR, XDCTRL (on Probe Controller board).
- A SCSI-2 bus is fed from the System CPU, buffered and routed to multiple internal discs.
- Remote control signals for printers are generated on the I/O board.
- The Footswitch is connected to the I/O board.
- The board controls the Patient I/O board, and provides serial trace data to the SDP board.

- An AC Power Interface controls power on/off and fan speed.

13.2 External I/O to Rear Connector Panel

Several signal are fed from the Internal I/O board to an External I/O board located in the rear of the system, right next to the Rear Panel. This board contains data buffers and a galvanic isolation section. Different types of signals are fed to connectors accessible on the Rear Panel.

- R, G, B and Sync are provided for external RGB monitors or printers.
- Composite video, black and white video and S-VHS video are buffered and fed to output connectors for external monitors and printers. Video and S-VHS can also be fed into the system.
- Two serial RS-232 ports are provided for external communication with e.g. the System CPU.
- An Ethernet signal from the System CPU is fed to a 15 pin D-connector (AUI), or on some of the earlier systems, a BNC connector.
- An ECG trigger pulse for use in stress echo machines, is output to a connector.
- Four analog signals can be input to an A/D converter.

13.3 Keyboard

The Front Panel Main board (FP_MAIN) is the core in the System FiVe keyboard. It is constructed around a uP6809 processor and contains several types of inputs/output registers which are used in encoding/decoding of the different devices connected to the FP_MAIN board. It has serial communication with the rest of the system through a RS-232 link to the Graphics board.

- The rotary switches are located both on the Front Panel Main board and on a separate Rotary Switch and Display board, connected to the main board via a cable. Decoding of rotary movement is done through a set of parallel registers.
- Each of the 8 TGC slide potentiometers generates analog voltages which all are A/D-converted and read by the local uP.
- The function and mode push-buttons (switches) are decoded in a matrix and read through parallel registers.
- The two displays are programmed directly from the local uP bus.
- Movement of the trackball is read through a versatile interface register.
- A standard QWERTY keyboard is used for type writing purposes. The matrix formed by the switches are decoded and read by the uP.

The two analog Doppler signals are fed from the Internal I/O board and up to a Front Panel Audio Amplifier board, where volume control and current amplification is performed. A connector for headphones is also provided on this board. From the audio amplifiers the Doppler signals are routed to loudspeakers via a cable.

Power Distribution - rev. 05

14 Introduction

14.1 Abstract

This is a short description of the power distribution in SYSTEM FIVE.

14.2 Document History

Rev.	Date	Sign.	Description
01	25 Aug. 1994	GRL	First version of document
02	20 Sep 1995	LHS	Updated layout Included page references
03	1 Oct. 1996	LHS	Corrected typo, added nominal load in DC Power Supply table.
03.1	5 Mar 1998	LHS	Added two new crossreferences under *14.3*.
04	19 Oct. 1999	LHS	Updated pr. sw. 1.7.1 release.
05	20 Jun. 2000	LHS	Updated pr. BT-00 release. .

14.3 References

- Block Diagram of *System FiVe Overall Power Distribution – rev. 05* on *page B3-7*.
- *AC Controller - rev.02* (description) on page A8-2.
- *DC Power Module - rev.03* (description) on page A8-6.

15 Description

There are three types of power supplies in SYSTEM FIVE; an AC power supply, a DC power supply, and a High Voltage power supply.

15.1 AC Power Supply

The mains power cable is fed to a combined on/off switch and circuit breaker located in the back of the system, in the AC power assembly. Rating of the circuit breaker depends on the nominal mains voltage in each country. Correct voltage setting is configured using jumpers on a terminal block. Then the mains is fed through an isolation transformer to the AC Controller board. This board contains a.o. a local +5V/ +12V DC power supply which purpose is to provide stand-by power for the power-switch in the front of the system and for e.g. a VCR’s tape counter.

When pressing the stand-by power-switch, the AC controller generates an interrupt via the INT I/O board to the CPU board, which in turn starts a power-off routine. Upon completion of this, the CPU returns a grant signal to the AC Controller which shuts off the relay for the power to the rack, monitor and peripherals (excluding the VCR on some systems). Each outlet to internal peripherals is filtered.

The AC Controller also contains a voltage regulator for controlling the speed of the fans. It senses the air temperature above the card rack, and adjusts the speed accordingly. If a high temperature reading occurs, maximum speed is selected.

15.2 DC Power Supply

Filtered 230VAC is fed to the DC power supply, which is a GE Vingmed Ultrasound specified supply designed and manufactured by Philips. The power supply has a modular design and provides the following voltages:

Voltage [V]	Nominal load [A]
+5(d)	120.0
+10	3.0
+12	4.0
-12	1.0
+15	4.0
-15	3.0
+5(a)	15.0
-5(a)	25.0

+5V(d) [digital] and ground is fed from the power supply to the main rack motherboard through thick rails. The other voltages are routed via a DC Extension board which plugs into the motherboard. The front panel and disks are powered via the internal I/O board. The voltages to these devices are fused with recoverable PTC fuses.

15.3 High Voltage Power Supply

The input to this supply is also filtered 230VAC. A mains cable plugs into the front of the supply, which again plugs directly into the motherboard.

The HV supply consists of three dual modules, all linear supplies providing symmetrical outputs; one generating 0 to +/- 80V (HV1, maximum 10W), another generating 0 to +/- 40V (HV2, maximum 10W) and a third generating +/- 80V (HV_MUX, maximum 8W).

The high voltages HV1 and HV2 are fed to the transmitter hybrids on the TX board (for PA/LA) and to the PRC board (for AA). The HV_MUX voltages are fed to the multiplexers located in the connector housing of the 192 element linear probes.

The two HV1 and HV2 supplies are controlled serially by the Front End Controller board, which also surveils the voltage and current drawn. This is done for output power safety purposes.

Bus Distribution – rev. 05

16 Introduction

16.1 Abstract

This is a description of the buses in SYSTEM FIVE:

- *"Front End Bus" on page A1-59*
- *"MLA Buses" on page A1-61*
- *"Pipelink Bus" on page A1-62*
- *"VME Bus (VME 64)" on page A1-65*
- *"from IMMEM to CPU/GRAPH (a.o. for test)." on page A1-66*

16.2 Document History

Rev.	Date	Sign.	Description
01	29 Aug. 1994	GRL	First version of document.
02	20 Sep 1995	LHS	Updated layout.
02.1	5 Mar 1998	LHS	Included 16.3 References, updated layout.
03	9 Sep 1999	LHS	Updated to reflect that the Image Port 2 board has been introduced.
04	18. Oct. 1999	LHS	Updated per 1.7.1 / 1.8 release.
05	1. Oct. 2000	LHS	Corrected error/updated per 1.9.x release.

16.3 References

Display, Control and I/O – rev. 09 (block diagram), *page B1-4*.

Front End – rev. 04 (block diagram), *page B1-5*.

17 Front End Bus

17.1 Bus Master:

Front End Controller Board (FEC), see *A2-47*.

17.2 Slaves:

- Transmitter Board (TX128), see page *A2-20*.
- Probe Controller Board (PRC), see page *A2-35*.
- Beam Former Boards (BF1-4), see page *A2-40*.
- RF- and Tissue Processor Board (RFT), see page *A3-3*.

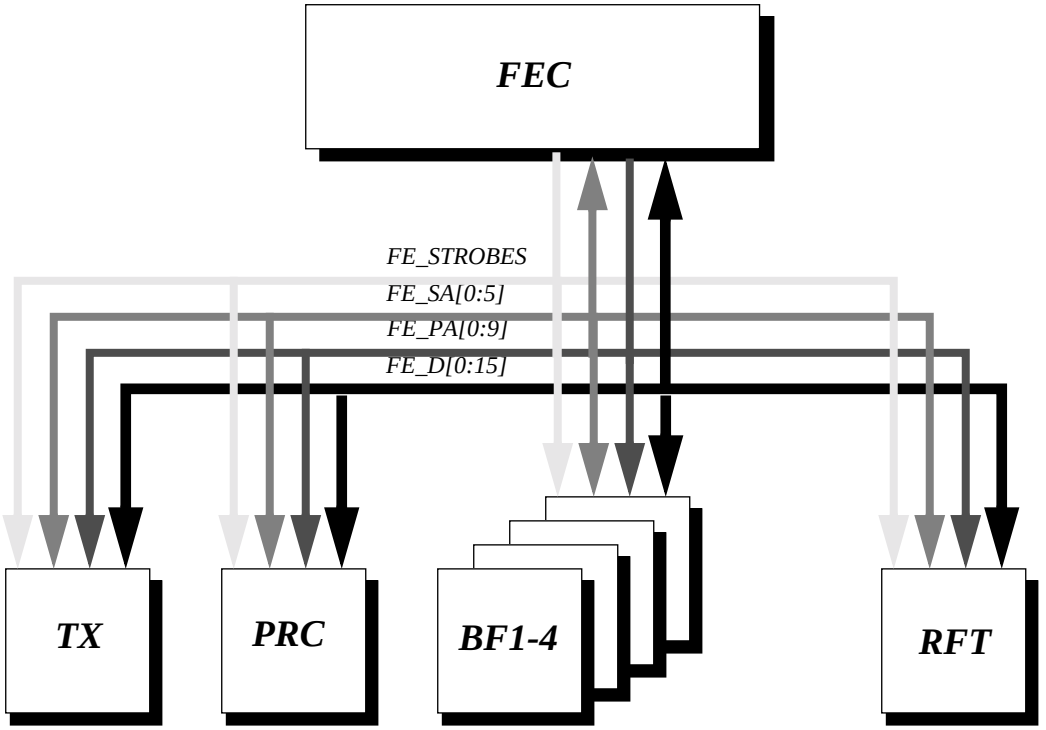


Fig. 17.1 The Front End Bus.

17.3 Description

The Front End Bus is a synchronous and bidirectional bus for control and setup.

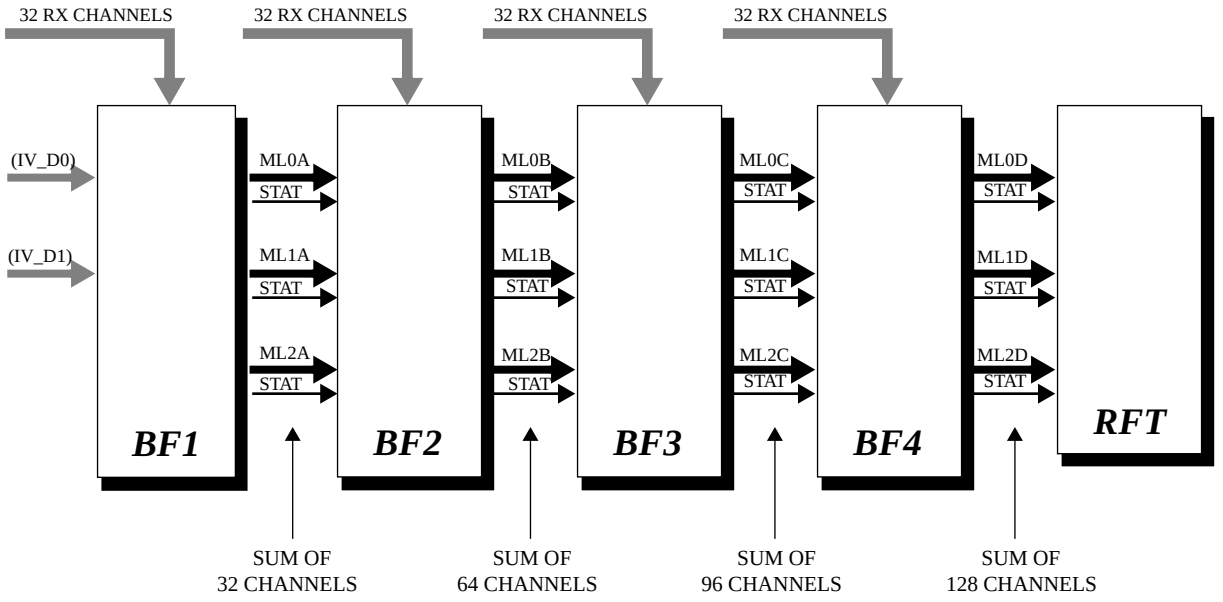
- Data:
  16 bit (FE_D[0:15])
- Address:
  6 bit device address (FE_SA[0:5]) and
  10 bit page address (FE_PA[0:9])
- Control:
  FE_C20 – FE bus address/control valid strobe (20 MHz ‘clock’).
  FE_SAS_L – Synchronous address strobe.
  FE_SWR_L – Synchronous write select.
  FE_PGTR_L – Page transfer select (for TX board and BF caches).
  FE_RFSH_L – Refresh strobe (for TX board and BF caches).
  FE_SUDS_L – Synchronous upper (FE_D[8:15]) data strobe.
  FE_SLDS_L – Synchronous lower (FE_D[0:7]) data strobe.
  FE_TACK_L – Transaction acknowledge (driven by the slaves).

The bus is used to read from and write to the various registers residing on the front end bus. Each transaction usually takes eight 40 MHz cycles, i.e. 200 ns.

18 MLA Buses

Data buses routing data through the Beamformer boards to the RFT board.

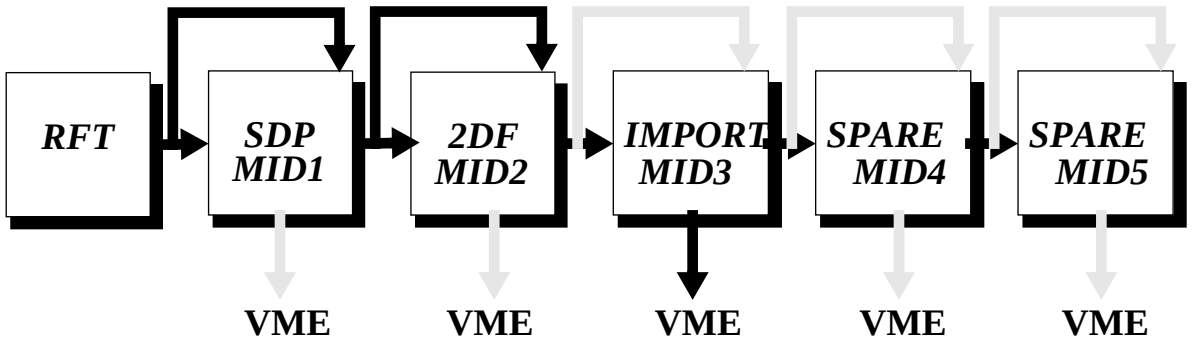
- Data:
  19 bit, MLn_D[0:18], n=0,1,2 (Currently only n=0,1 supported by the BF boards.)
  Data rate: 20 MHz
- Control:
  3 status signals (both going out of and in to each BF board):
  MLn_RDY: MLA data ready
  MLn_VAL: MLA data valid
  MLn_ERR: MLA error



19 Pipelink Bus

- Bus dispatcher: RFT
- Slaves: MID1-MID5 (SDP, 2DF, IMPORT (or Image Port 2))
- Unidirectional (from RFT to IMPORT (or Image Port 2), via mid processors).
- Data transfer rate: 20 MHz.

The bus is used for transfer of Tissue-, Doppler- and Flow data in a sequential way to the Image Port (IMPORT) board (or the Image Port 2 board), which maps the data into the proper memory buffer in the Image Memory. If the Image Port (IMPORT) board is used, the Image Memory is located on the Image Memory board (IMMEM) and if the Image Port 2 board is used, the memory is included on the board.



The Image Port board (or Image Port 2 board) must always be located next to the last of the mid processor boards. E.g. if a system does not have a 2DF board, the IMPORT (or Image Port 2 board) must be moved to the slot next to SDP, and an BG/IACK VME JUMPER board, GE Vingmed Part Number FA200075, must be inserted in the P1 connector in the IMPORT/IP2 slot (see *"VME Bus (VME 64)" on page A1-65*).

19.1 Pipelink Bus Format:

- 18 bit wide, PLINK[0:17] with
  - 16 bit information and
  - 2 bit (msbs) control indicating type of data in the information word: Control word 1, control word 2 or data.

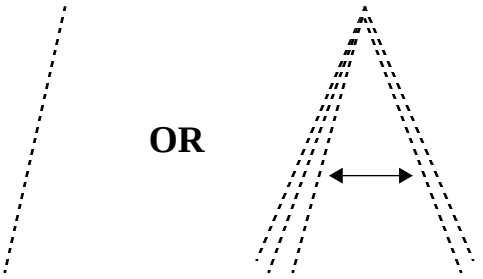
19.2 Pipelink Control (CTL):

- 00: Control word 1:
  - The information field identifies signal process and controls synchronization and dataflow.
- 01: Control word 2:
  - The information field identifies logical vector number.
- 10: Data -- 16 bit data:
  - The information field contains 16 bit data words, i.e. tissue-, Doppler- or flow data.
- 11:not used.

19.3 Pipelink Dataflow:

19.3.1 Tissue:

Data processed and transferred from RFT to IMPORT/IP2 in blocks of vectors or complete frames.

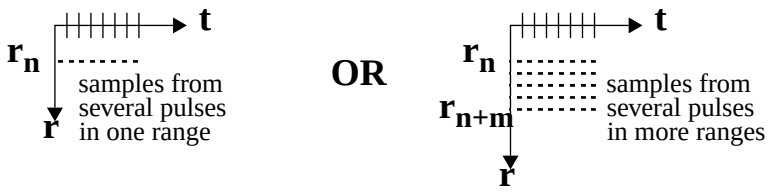


19.3.2 Doppler:

Raw data transferred from RFT to SDP in blocks containing data from one or all range gates of data.

Data from SDP to IMPORT is transferred spectrum line by spectrum line.

RFT TO SDP



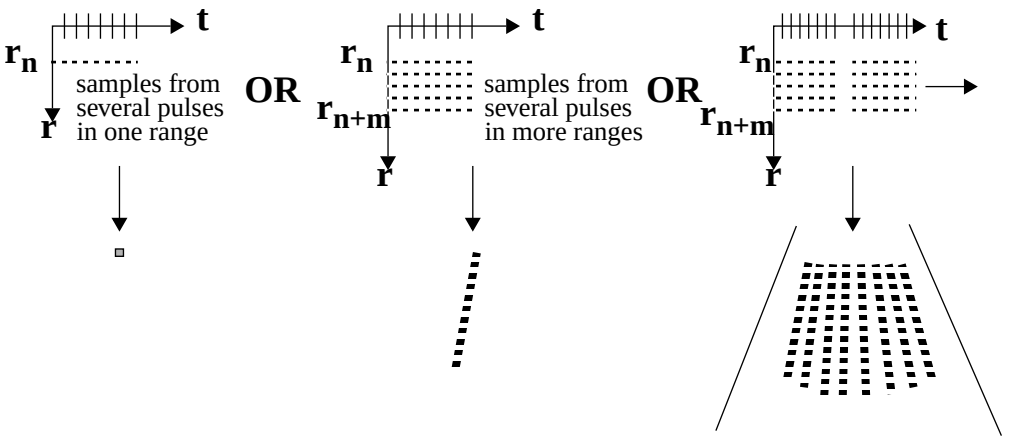
SDP TO IMPORT/IP2

19.3.3 Flow:

Raw data transferred from RFT to 2DF in blocks containing either data to generate one flow estimate from one range, data to generate one flow vector or data to generate one complete flow frame.

Data from 2DF to IMPORT/IP2 is transferred flow vector by flow vector.

RFT TO 2DF



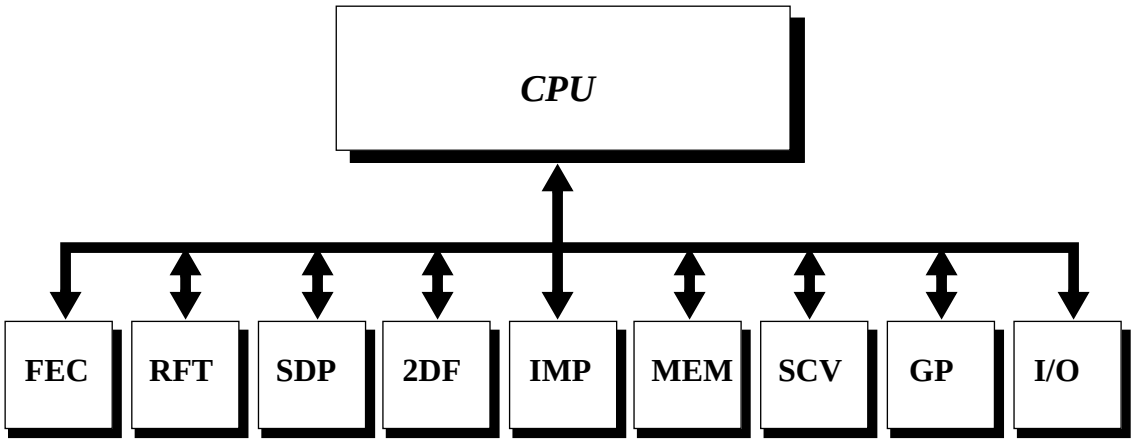
20 VME Bus (VME 64)

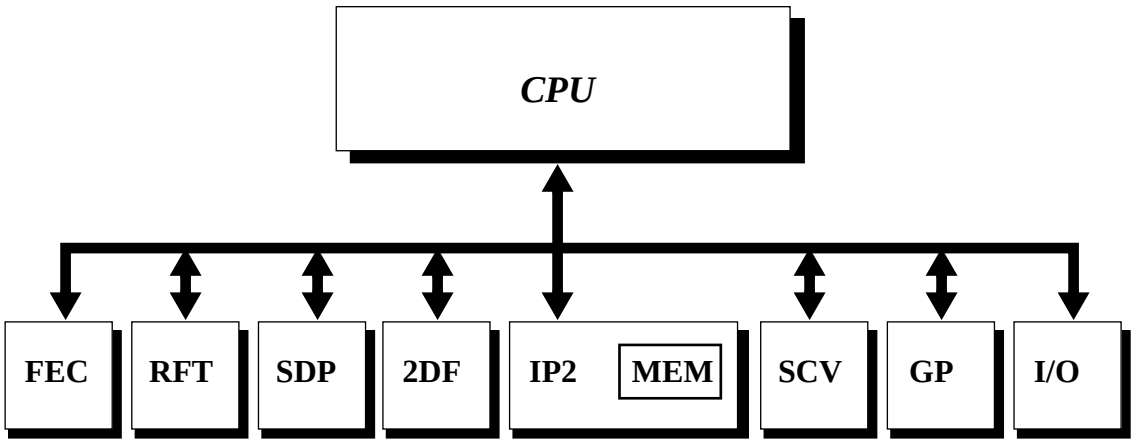
- Bus master: CPU
- Slaves: FEC, RFT, SDP, 2DF, IP2 (or IMPORT and IMMEM), SCONV, GRAPH, INT I/O
- Data: 32 bit D[0:31]
- Address: 32 bit A[0:31]

There are two alternative Image Port /Memory board variants in the field.

The upper illustration is with separate Image Port and Memory boards

The lower illustrations is with combined Image Port and memory, called Image Port 2 (IP2)





NOTE: In all unused VME board slots (spare boards) a VME BG/IACK JUMPER board must be installed on the P1 connector (upper). This board jumpers the Bus Grant and Interrupt Acknowledge lines pass the unused slot.

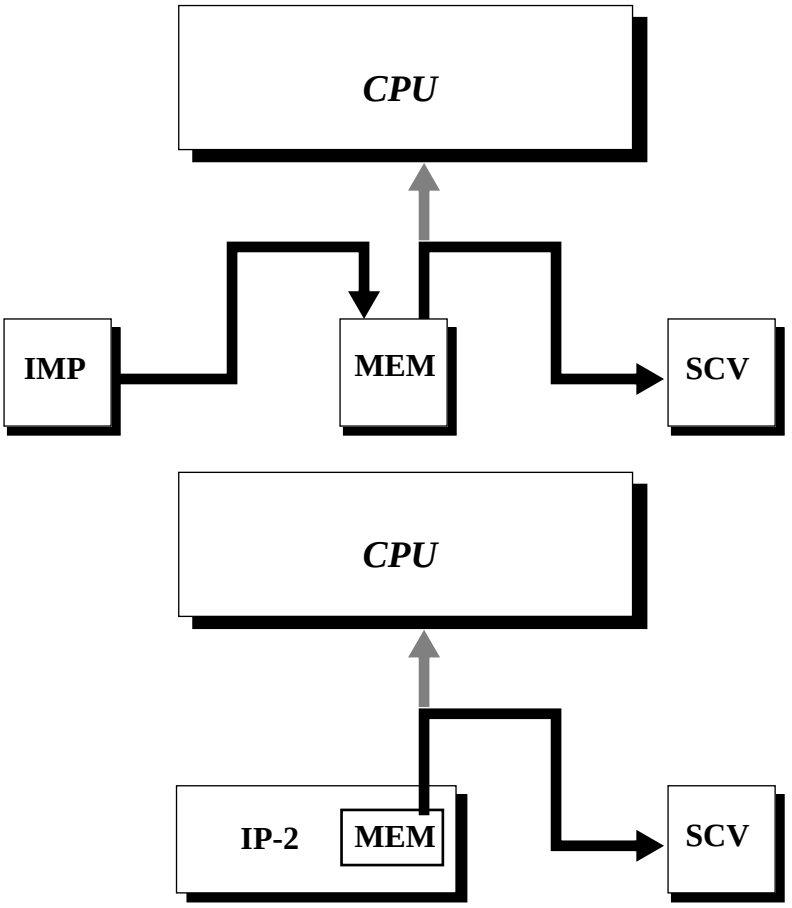
The bus is both used for control/setup and data flow.

20.1 Control/Setup

All boards residing on the bus.

20.2 Data Flow

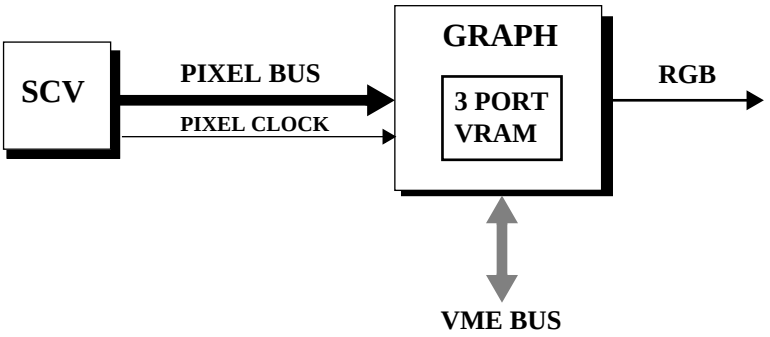
- From IMPORT to IMMEM (Image Port 2 (IP-2) holds these functions on one board),
- from IMMEM (or IP2) to SCONV,
- from IMMEM to CPU/GRAPH (a.o. for test).



21 Pixel Bus

High-speed, synchronous, multiplexed (address and data) bus dedicated for imaging purposes.

- Dataflow: SCONV to GRAPH.
- Data:
  - 24 bit (PD[0:23])
  - 8 bit R, 8 bit G and 8 bit B.
- Address:
  - 12 bit line address and 12 bit pixel position address (on line).
- Data rate:
  - 20 MPixels/sec.
- Burst oriented:
  - Can transfer one scan line in one burst.


SCV
PIXEL BUS
PIXEL CLOCK
GRAPH
3 PORT
VRAM
RGB
VME BUS

Clock Distribution – rev. 04

22 Introduction

22.1 Abstract

This is a description of the clock distribution in SYSTEM FIVE.

22.2 Document History

Rev.	Date	Sign.	Description
01	24 Aug. 1994	GRL	First version of document
02	2 Jan. 1995	LHS	Updated layout and corrected some minor errors.
03	19 Oct. 1999	LHS	Updated text.
04	20 Jun. 2000	LHS	Updated text.

22.3 References

Block Diagram for SYSTEM FIVE Clock Distribution on *page B3-3*.

23 Description

In order to provide synchronous data transfers throughout the system, a global 40 MHz clock is distributed to all boards. The clock signals are generated on the Front End Controller board. A 160 MHz clock from an ECL oscillator is divided down to four quadrature 40 MHz clocks; a differential (H and L) I clock and a differential (H and L) Q clock. These clocks are buffered and distributed on ECL level to the other boards through three different paths, 1, 2 and 3.

All boards in the Front End receives clock 1, while clocks 2 and 3 are distributed in an interleaved fashion to the boards in the mid- and display section.

The clocks are terminated to -2V through 47 W resistors at the physical end of the clock traces on the motherboard. The -2V voltage is generated by a regulator on the FEC board. Typical high and low levels for ECL logic are -0.9V and -1.8V respectively.

Each board receives one pair of the I and Q clocks (except RLY, RX board, CPU and IMMEM). However, the SCONV board has its own local clock oscillator used to generate the 20 MHz clock for data transfers to the GRAPH board on the Pixel bus.

A global reset signal is also distributed to all boards in the same way as the clocks. The reset signal is derived from the SYSRESET_L signal on the VME bus.

Board Formats – rev. 02

24 Introduction

24.1 Abstract

This is a description of the board formats in SYSTEM FIVE.

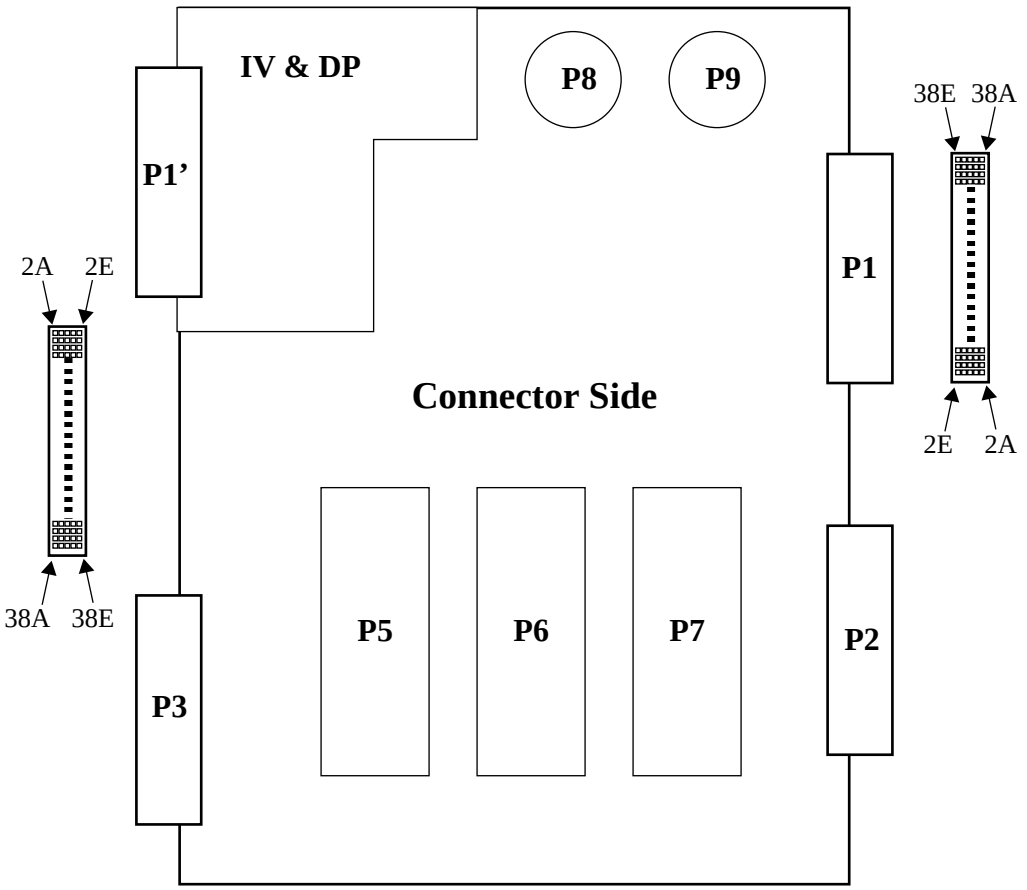
24.2 Document History

Rev.	Date	Sign.	Description
01	29 Aug. 1994	GRL	First version of document
02	19 Oct. 1999	LHS	Updated content.

25 RLY

Board with 185 or 93 pin connectors / 2.5 mm pin spacing. P1' is located on the IV & DP Connector board mounted as a piggyback on the upper left corner of the RLY board. P1' and P3 are for motherboard connections, and P1 and P2 are for XDBUS connections. P5-P7 are for PA/LA probes and P8 and P9 are for APAT probes.

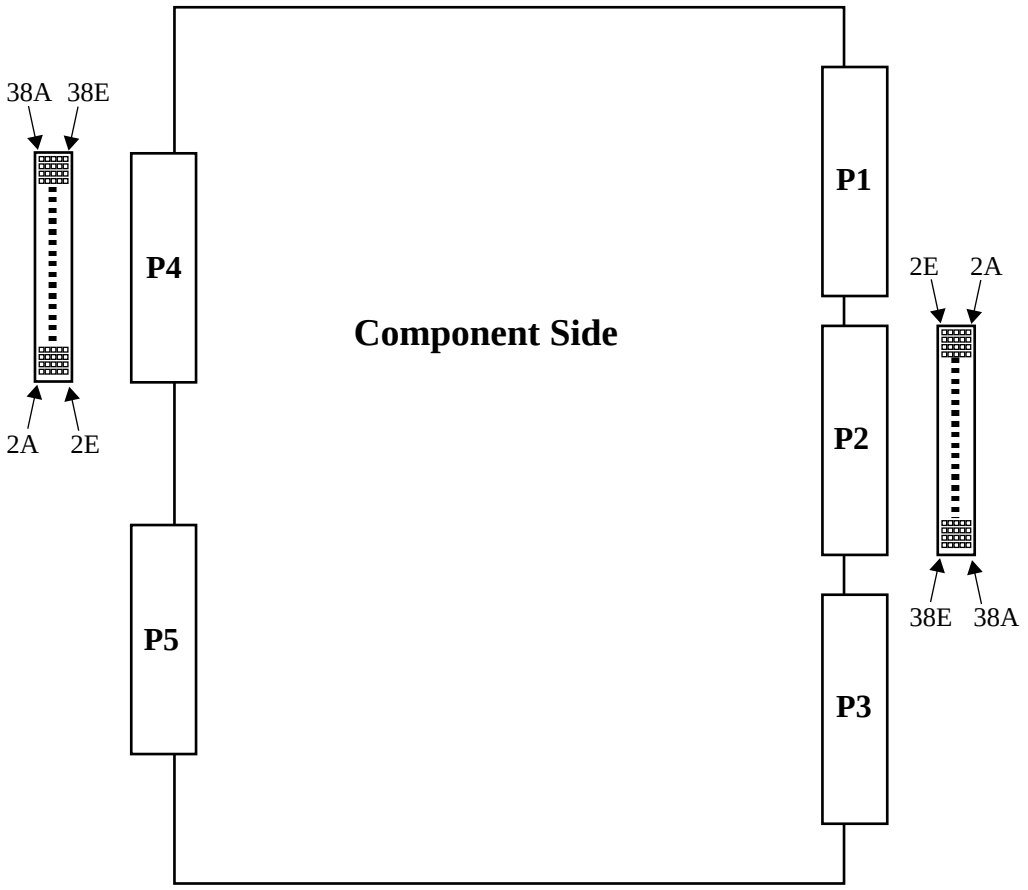
Board size (W x H): 280 x 350 mm.



26 TX128, RX128, RX64 and PRC

Boards with 185 or 93 pin connectors / 2.5 mm pin spacing. P1, P2 and P3 are for motherboard connections, and P4 and P5 are for XDBUS connections.

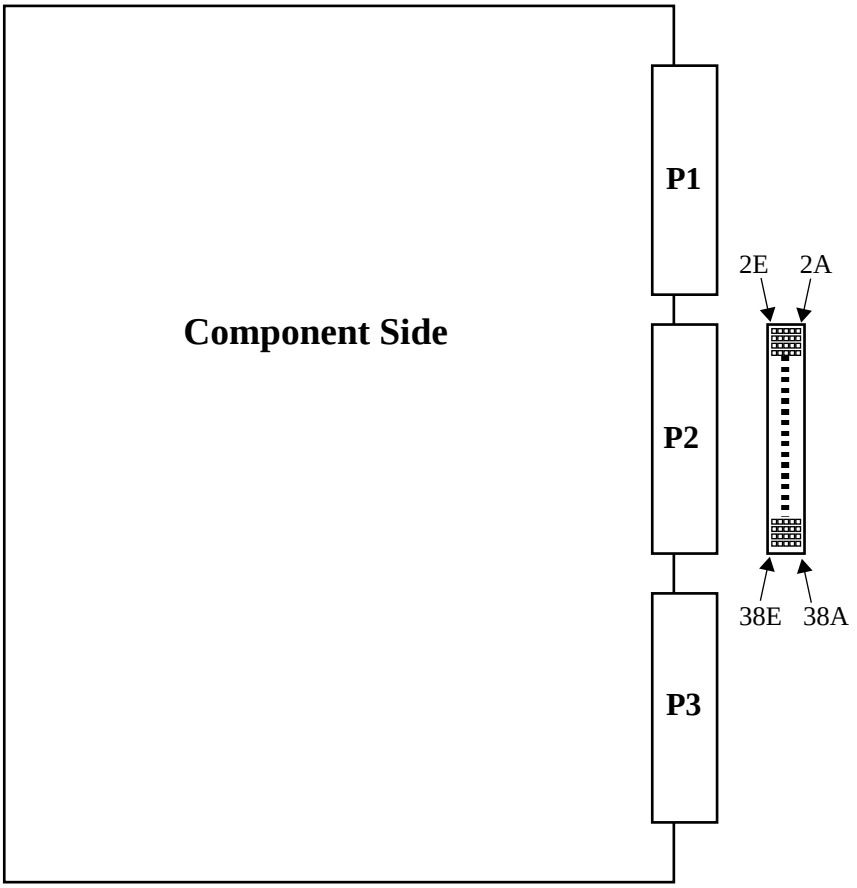
Board size (W x H): 280 x 366.8 mm.



27 BF1-4, FEC and RFT

Boards with 185 pin connectors / 2.5 mm pin spacing. P1, P2 and P3 are for motherboard connections.

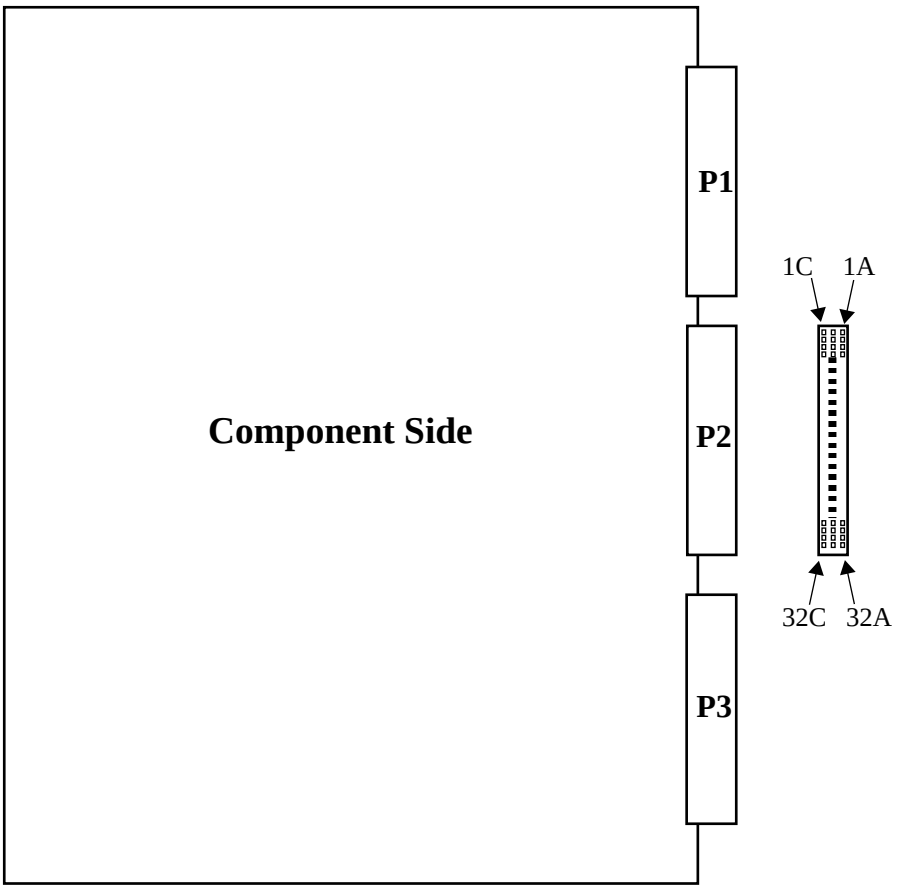
Board size (W x H): 280 x 366.8 mm.



28 SDP, 2DF, IMPORT, IP2, SCONV and GRAPHIC

Boards with 96 pin Euro-connectors, 2.54 mm spacing. P1, P2 and P3 are all for motherboard connections.

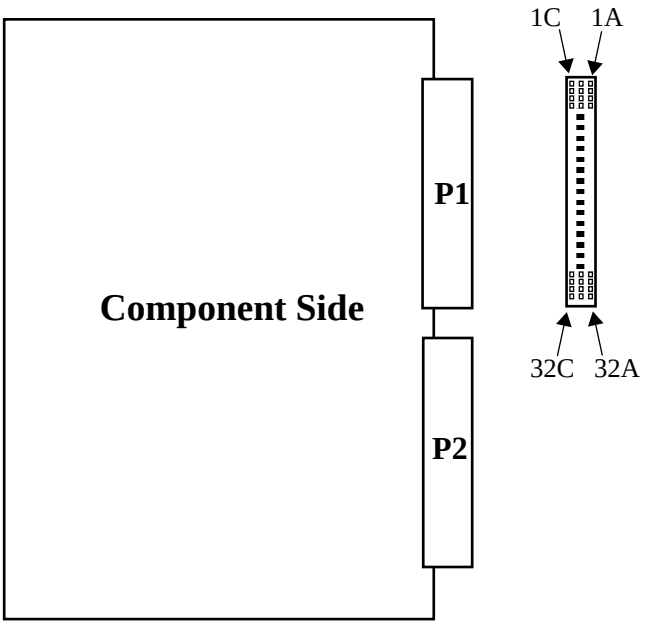
Board size (W x H): 280 x 366.8 mm.



29 CPU and IMMEM

Standard double Europe size boards with 96 pin Euro-connectors, 2.54 mm spacing. P1 and P2 are both for motherboard connections.

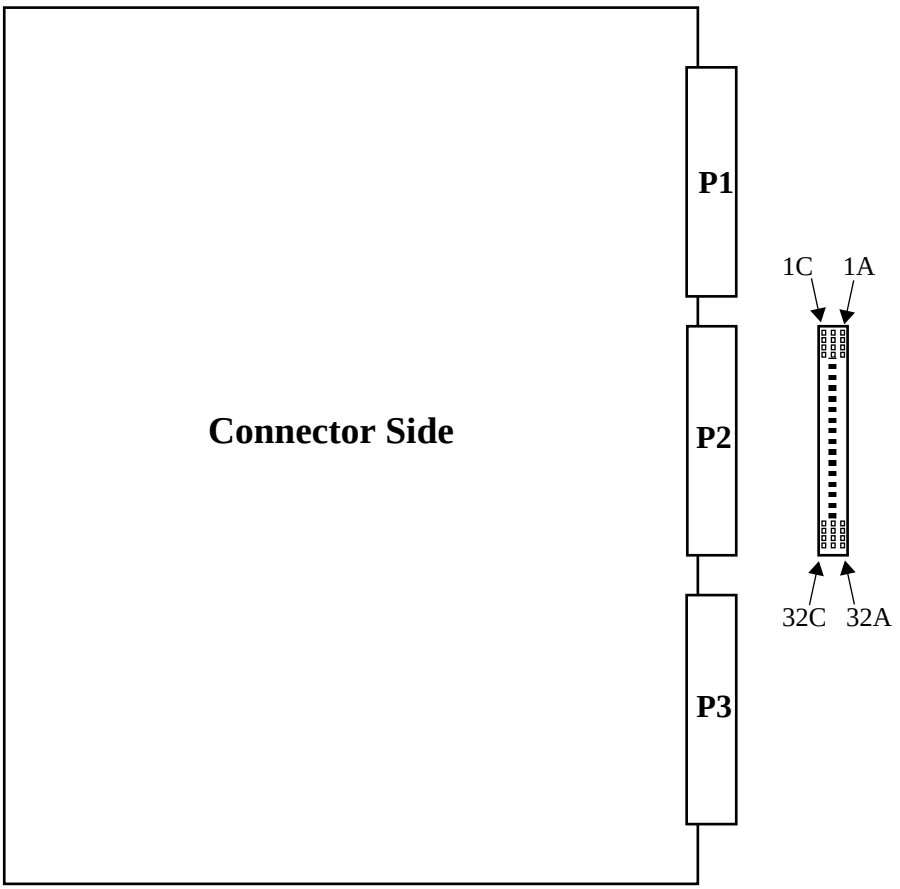
Board size (W x H): 160 x 233 mm.



30 INT I/O

Board with 96 pin Euro-connectors, 2.54 mm spacing. P1 and P2 are both for motherboard connections.

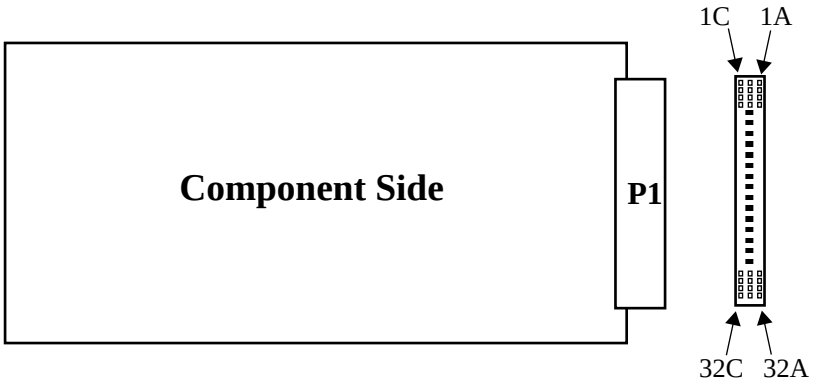
Board size (W x H): 188 x 366.8 mm.



31 HV POWER

Board with 96 pin Euro-connector, 2.54 mm spacing. P1 is for motherboard connections.

Board size (W x H): 232.2 x 110.4 mm.



The Front End Modules

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the Front End of the instrument.

Modules and sub-systems described in this part of the manual

The modules and subsystems in this part of the manual:

Module / subsystem	Page
Probe Description - rev. 06	**A2-3**
Probe Cable – rev. 01	**A2-11**
IV & DP Connector Board – rev. 04	**A2-12**
Relay Board - RLY rev. 03	**A2-15**
Transmitter Board - TX128 – rev. 04	**A2-20**
Receiver Board - RX 128 - rev.02	**A2-25**
Receiver Board - RX 64 rev.02	**A2-29**
Probe Controller Board - PRC – rev. 04	**A2-35**
Beam Former Board - BF - rev.03	**A2-40**
Front End Controller - FEC – rev. 04	**A2-47**
Patient I/O rev.01	**A2-53**
Transducer Bus Board - XDBUS – rev. 04	**A2-59**

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A2_01_Front_End_i.mnh:03.
Printed: December 5, 2000.

Your Notes:

Probe Description - rev. 06

1 Introduction

1.1 Abstract

This document gives a general description of the probes used in System FiVe. Both flat phased array, flat linear array, curved linear array and annular array probes are covered. Emphasis is put on the electronically steered probes.

1.2 Document History

Revision	Date	By	Description
01	16 Sep 1994	GRL	First revision of document
02	26 Apr 1994	GRL	Impr. mux description
03	30 May 1996	GRL	Interface board descr. corrected
04	10 Oct 1996	SB/lhs	General update
05	19 Jan 1997	LHS	Minor update
06	1. Oct 2000	LHS	• Updated company name. • Corrected some small errors.

Table 1: Document History

Macintosh HD:User:James:@I-arb:Service:S5_ServiceMan:S5_serv_files:A2_02_03.fm.
Printed: December 5, 2000.

1.3 Abbreviations/Nomenclature/Definitions

FPA	Flat Phased array
FLA	Flat Linear array
CLA	Curved linear array
AA	Annular array
Mux	Multiplexer
SDA	Serial Data
SCL	Serial Clock
EEPROM	Electrically Erasable Programmable Read-Only-Memory
SPST	Single Pole Single Throw (Switch)

1.4 References

- *Probes* , see chapter *E*
- *Spare Parts – 02*, see chapter *O*

2 Electronically Steered Probes

2.1 Overview

The probes are divided into the following modules

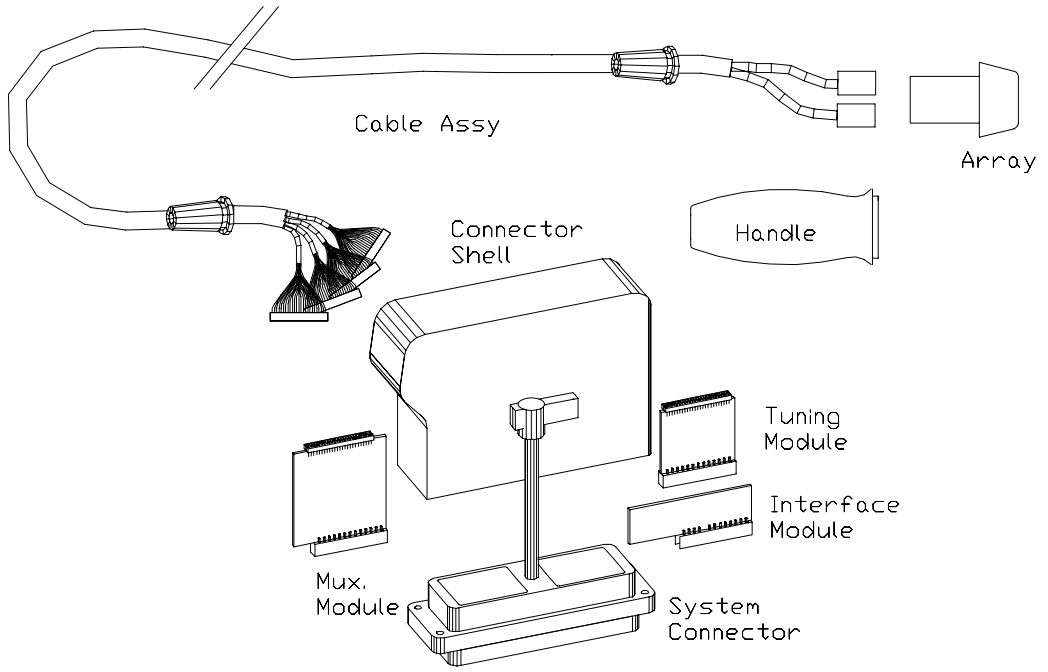
- Transducer array
- Cable

- System connector
- Mechanics

The system connector comprises the following sub-modules:

- Tuning boards
- Multiplexer boards when applicable
- ID board, Interface board

On the figure below, the various modules included in a probe is shown.



2.2 Connector Interfaces

In the following section, the various interfaces between modules are described.

Probe Assembly - System

The connector used is ITT-Cannon DL5-260 or equivalent.

System Connector - Tuning/ID/Interface/Multiplexer Boards

The electronic boards plug directly into the pin rows on the Cannon connector. The board connectors used here are 26 pin, double row, 0.1 inch female grid connectors.

Tuning/ID/Interface/Multiplexer Boards - Cable Assembly

The cable plugs into the electronic boards through 0.05 inch double row connectors.

Interface for active probe indication LED

In the probe, there is a requirement for an indicator in the transducer assembly. The connectors used on the interface board and cable assembly, is based on Hi-Rose A4B 2 terminal crimp connectors, with female contacts on the cable assembly. These connectors are suitable to be used directly on a standard 3 mm LED.

2.3 Module Descriptions

In this chapter, a general description of the various modules is given.

2.3.1 Transducer Array

The transducer array is built as a separate module, with connectors as described in section *2.2*.

2.3.2 Cable Assembly

The selected coax is a 40 AWG, 50 or 75 ohm. This is a dimension with tolerable losses. It is a standard cable with high production volume, and is commonly used and produced by various cable manufacturers.

2.3.3 System Connector

The system connector to be used is an ITT-Cannon DL5-260P or equivalent. The connector is used together with a matching EMI-shell to ensure good shielding of the interface between system and probe.

The electronic boards are directly connected to the system connector with connectors as described in chapter *2.2*.

2.3.4 Mechanics

The mechanics of the probe include all the remaining hardware which is not part of the other main modules. The main items are probe nose piece and handle, and system connector housing.

2.3.5 System Connector Boards

The boards are contained in the ITT-Cannon 260 pin connector. Connectors are used between the boards and the multi-coax cable to the probe, so it is possible to mount the boards without any soldering.

The interconnection between the interface board and the multiplexer boards is by soldered wires between the boards. The wires are accessible from the outer board edges, and are easily removable.

The boards are designed to be mounted on the Cannon connector with 0.2" C/C spacing

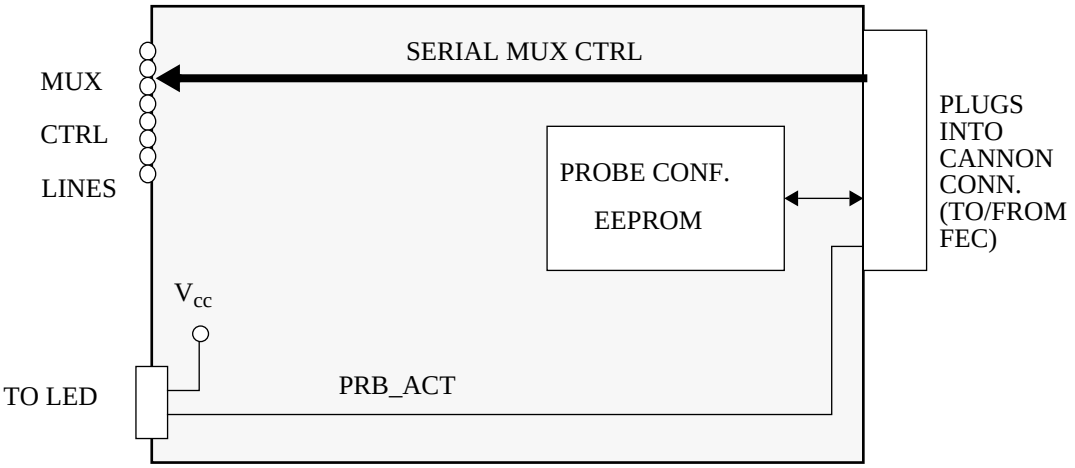
Probe Interface Description

The Interface board is used in probes with more than 128 elements and connects necessary power supply, data, clock and latch enable signals to the multiplexer boards. The Id board do not contain these functions, only the ones listed below.

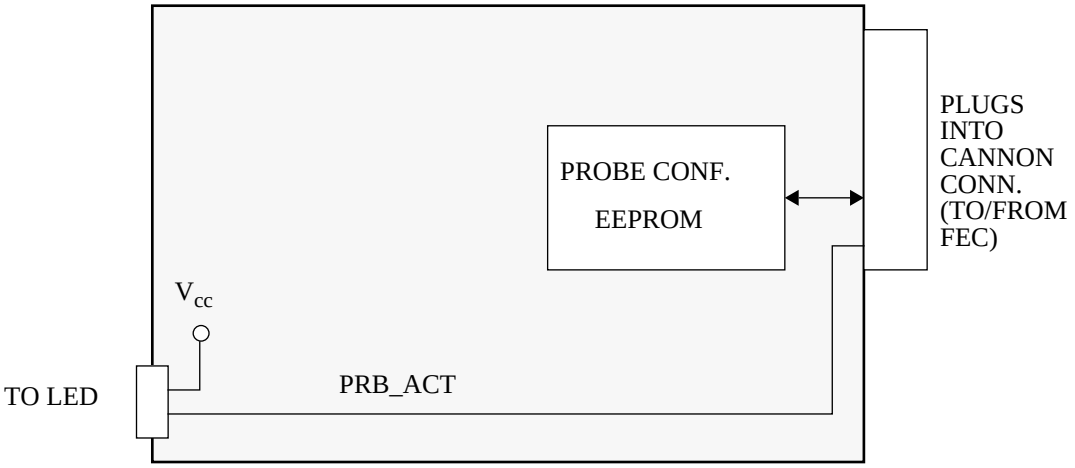
There is also an interconnection to the Active Probe indicator LED in the probe head.

The power supply lines contain some filter components to reduce the component count on the multiplexer boards. All logic lines are terminated in 100k resistors to bleed static charges.

The boards contain an EEPROM circuit with enough capacity to keep the data for the probe identification. The control signals are generated on the Front End Controller. The address for the EEPROM circuit is hardwired to 000_b.



INTERFACE BOARD (LA)

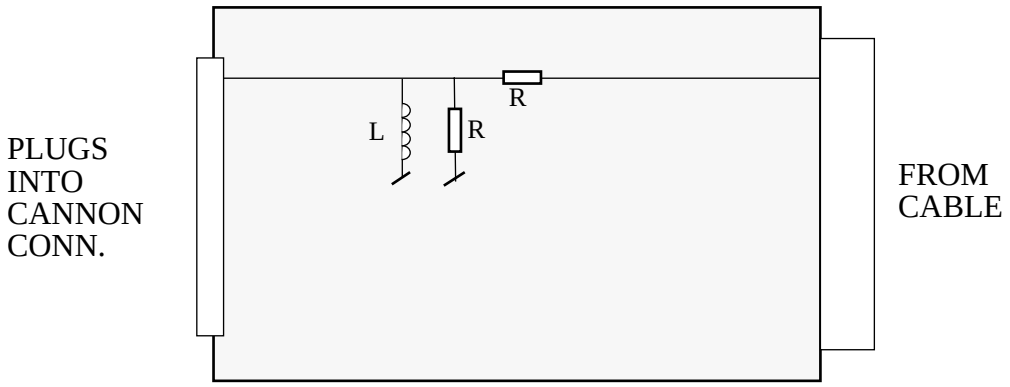


ID BOARD (PA)

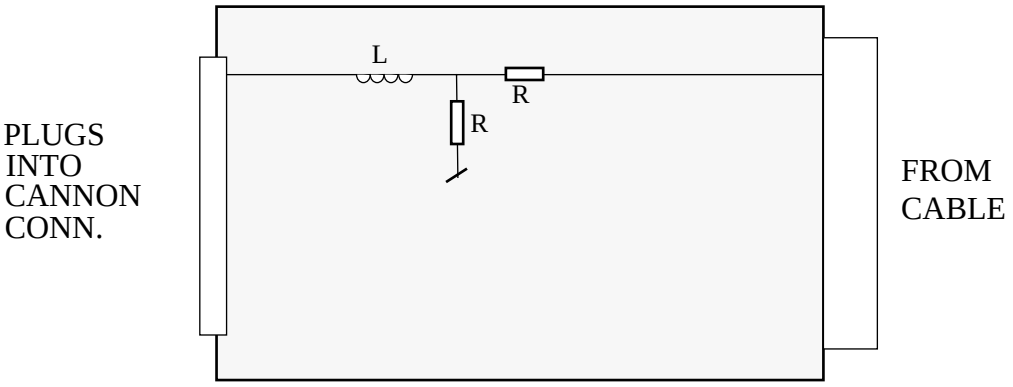
Tuning Board Description

The tuning boards contain the tuning components for impedance matching between the coaxial cables from probe elements to transmitters. Different boards have been designed for serial and parallel tuning. Serial and parallel resistors are added to compensate for mux losses, and to attenuate out-of band resonances for the probe. Component values are selected for each probe type.

Each board contains matching components for 16 channels.



TUNING BOARD, PARALLEL TUNING (ONE CHANNEL SHOWN)

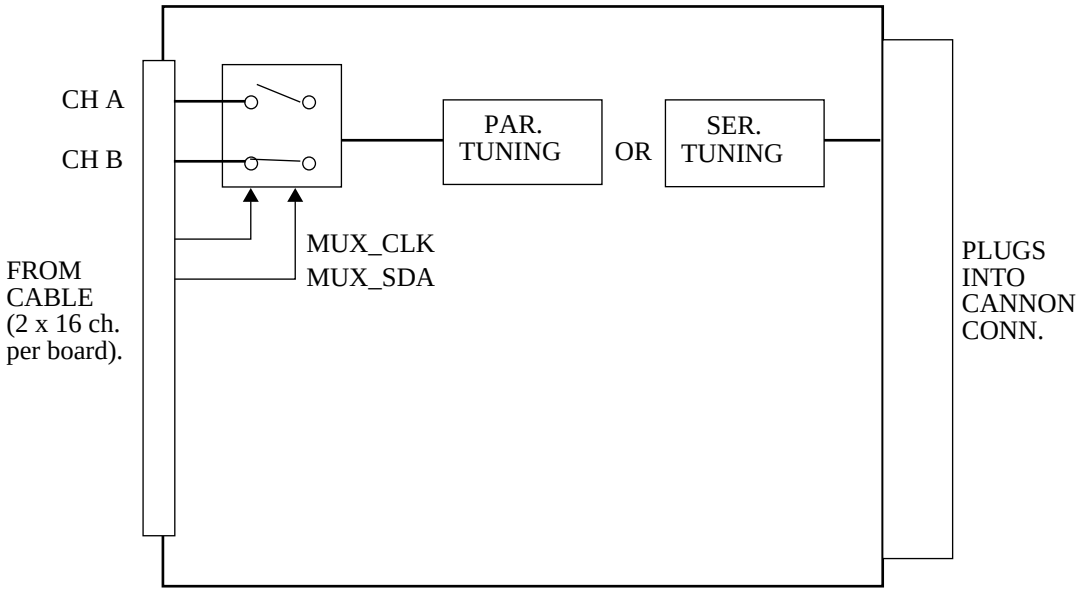


TUNING BOARD, SERIAL TUNING (ONE CHANNEL SHOWN)

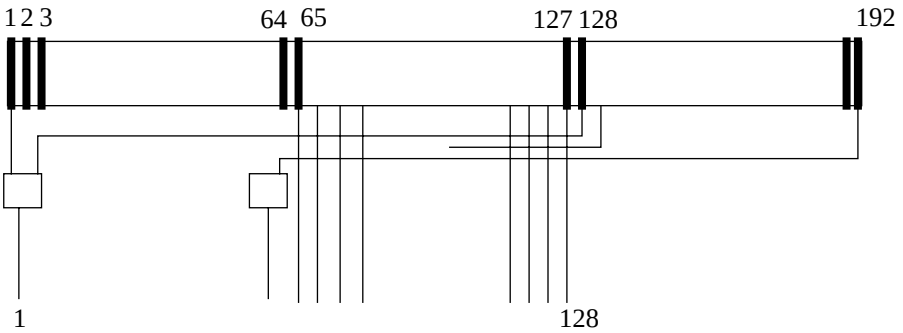
Multiplexer Board Description

Each multiplexer board multiplexes 32 elements to 16 channels. Of the circuits available, the Supertex HV21716WG is selected. It has acceptable loss and cross-talk characteristics. The circuit contains 8 SPST switches, and is serially programmed. Several switches may be programmed in series. 128 switches are required to multiplex 192 elements to 128 channels, and to achieve sufficient fast programming time, it is necessary to program the switches with 8 parallel data lines.

The boards also contain the tuning components for the elements, and to reduce the number of components, only the active elements are tuned. It implies that the unused elements are not terminated. Different boards for serial and parallel tuning have been designed due to space limitations.



MULTIPLEXER & TUNINGBOARD
TWO TO ONE CHANNELMULTIPLEXING SHOWN



3 Mechanically Steered Probes

3.1 Trans-thorax Probes

The probes are divided into the following parts:

- Transducer array (4-5 elements formed as concentric rings).
- Motor coil
- Position sensing coil
- Lemo connector
- Mechanics (probe chassis, handle, dome, color coding ring).

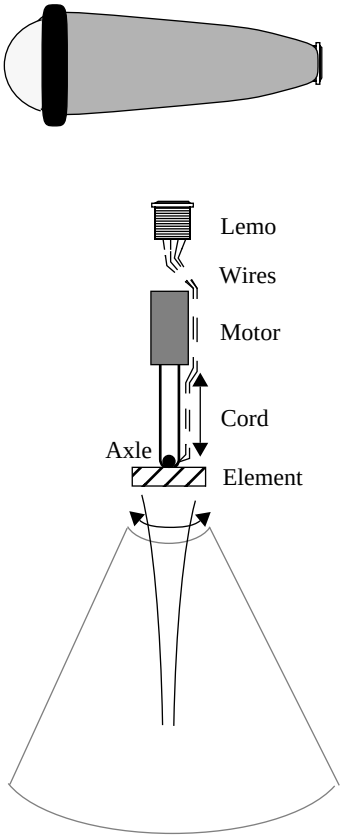


Fig. 3.1 Element Movement

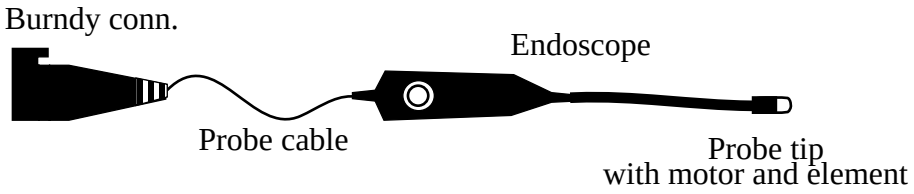
The transducer is mounted on an axle, which connects to the motor via a cord. The elements are electrically connected to the Lemo connector through flexible wires.

Each probe contains a code resistor which is read by the system.

3.2 Transesophageal probes (TE)

These probes are principally working in the same way as the trans-thorax probes, but in addition contains the following parts.

- Endoscope
- Probe cable



The Burndy connector contains coaxial pins for the element signals, and single pins for the other signals. It plugs directly into the system RLY board. The endoscope is used to move the probe tip in the desired position inside the esophagus. This is done by use of the two wheels on the endoscope house.

Vingmed Sound currently have three types of TE probes; single-plane, multi-plane and an electronic TE probe (Oldelft). In the multi-plane probe, the second scan plane is controlled electronically between 0 and 180°.

Probe Cable

4 Introduction

4.1 Abstract

This document gives a brief description on the Probe Cable used for some probes.

4.2 Document History

Rev	Date	Sign	Description
01	8 Apr. 1998	LHS	Initial document release

Table 2: Revision control.

4.3 Definitions/Abbreviations/Nomenclature

APAT: Annular Phased Array Transducer

4.4 References

Annular Phased Array Transducer (APAT) on page E1-2.

5 Descriptions

- A Probe Cable with connectors in both ends are used for some probes. One end is plugged into the System FiVe, the other end is plugged to the probe.
- The cable is marked with Part Number and Serial Number. Look for these numbers near the black connector. (See arrow.)

- From the factory, the cable is delivered with a protection sleeve. (See the lower picture.)

IV & DP Connector Board

6 Introduction

6.1 Abstract

This document is a description of the IV & DP Connector Board used in System FiVe. The board contains connectors for the stand-alone Doppler probe, in addition to the remote AC power Standby switch. It also contains a 2 MHz notch filter to remove the carrier frequency in CW when using the 2 MHz Pedof probe.

6.2 Document History

Rev	Date	Sign	Description
01	23 June 1994	GRL	First version of document
02	6 Feb 1997	GRL	Added 2 MHz CW filter for 2 MHz Pedof probe.
03	18 Nov 1997	GRL	Changed R6 from 100 to 220 ohm to reduce gain to avoid saturation (gain down 7 dB).
04	1 Oct 2000	LHS/jb	Updated contents. Maintenance Aid moved to Ch.K

6.3 Definitions/Abbreviations/Nomenclature

DP- Doppler

STBY-Stand-by

RLY - Relay board

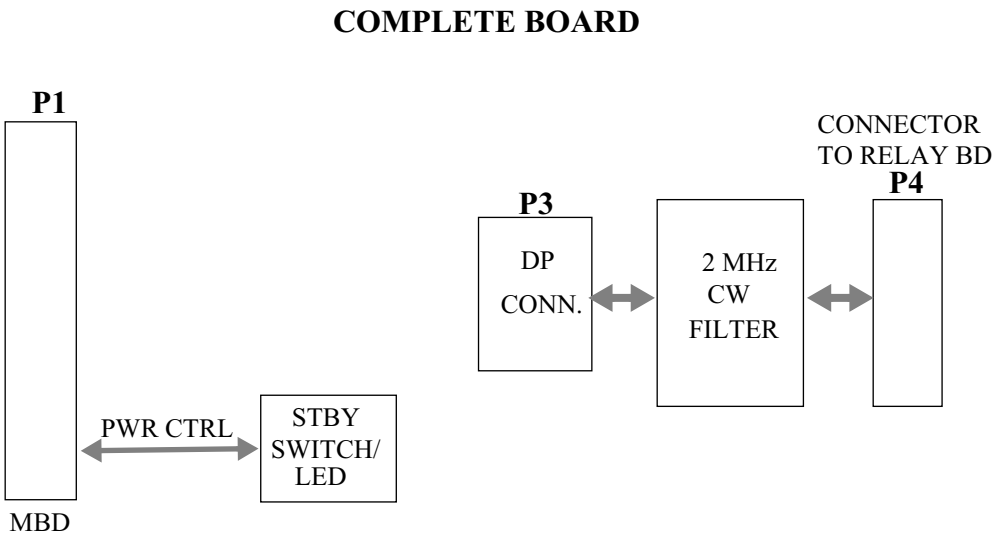
PRC - Probe Control board

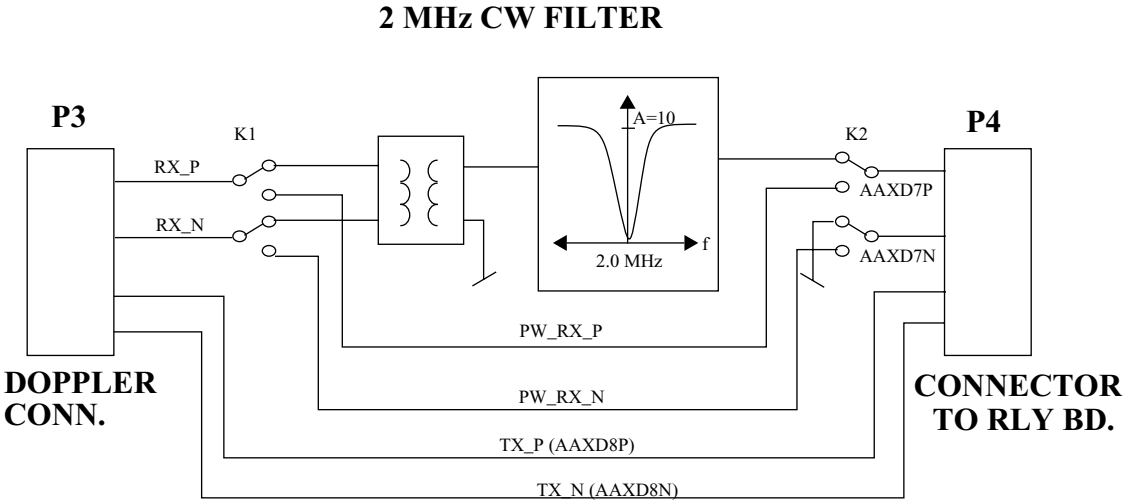
7 Physical Dimensions

The board itself is mounted as a piggyback board on top of the RLY board, fitting a connector on this board. Size is 135 mm (W) by 130 mm (H).

8 General Description and Block Diagram

8.1 Block Diagrams





NOTE: A 20 k resistor is permanently installed from pin 5 (XDDPCD) to GND on this version of the board (with 2 MHz CW filter). This resistor which is in parallel with the probe code resistor, alters the probe code ID, thus providing a way for the system to identify the presence of the CW filter.

8.2 Standby Power Switch

Four signals are routed between the AC controller board and the Power Switch over the backplane to the P1 connector. They are all referenced to “digital ground”.

STBTGL_L is low-pass filtered to avoid glitches from toggling power on and off.

8.3 2 MHz CW Filter

This filter is a narrowband notch filter which purpose is to attenuate the 2 MHz carrier frequency from the 2 MHz Pedof probe in CW Doppler. This is done to prevent the receiver from being saturated by this frequency component.

The differential Rx and Tx (also called AAXD7 and AAXD8) signals to/from the receiver/transmitter are routed from the RLY board stiftlist, P4, onto this board.

In PW Doppler the relays K1 and K2 are energized, thus the Rx signal (AAXD7) is bypassing the filter circuitry. The TX signal (AAXD8) is routed directly from P4 to P3.

In CW Doppler, the Tx signal (AAXD8) is also routed directly from P4 to P3. The relays are de-energized, thus feeding the Rx signal from the probe via P3, through relay K1 into the filter. A 4:1 transformer is provided for impedance matching. The first stage in the filter is an amplifier (Q3) with a tuned circuit (L21, C7, CV1) in the collector. The circuit has a Q of apprx. 5 with its maximum adjusted to peak at 2 MHz. This is done to remove undesired out-of-band noise.

The gain of the amplifier is determined by the ratio of the R7//$|Z_{X1}|$ divided by R6. The impedance of the Xtal, X1, is low (typically 70 ohm) at resonance (2 MHz) and high (several kohms) at frequencies outside +/- 500 Hz from 2 MHz.

Thus, for frequencies outside +/- 500 Hz from 2 MHz, the gain is approximately 13 dB (1000/220), while at resonance the gain is -3 dB (~70/100), giving a 16 dB attenuation of the 2 MHz carrier frequency provided that this carrier exactly matches the frequency of the Xtal. There are provisions for installing two Xtals in parallel, to widen the bandwidth and/or increase the attenuation.

The emitter follower stage consisting of Q1 and Q2 provides current to the receiver on the RX128 board.

Switching between PW and CW is done by a control signal PW_CW_L generated on the FEC board.

Relay Board - RLY

9 Introduction

9.1 Abstract

This document describes the Relay Board (RLY board) used in the SYSTEM FIVE Front End. The Relay Board contains three phased array probe connectors and provides a switchable connection between the probes and the 128 channel phased array Front End. It also supports two annular probes containing up to six transducer elements, and one stand-alone Doppler probe containing two transducer elements.

9.2 Document History

Revision	Date	By	Description
01	23 Aug. 1994	GRL	First version of document
02	15 Dec. 1994	LHS	Updated
03	1 Oct. 2000	LHS/JB	Updated Xref

9.3 Definitions/Abbreviations/Nomenclature

PA	Phased array
AA	Annular array
TE	Transesophageal probe
MPTE	Multiplane transesophageal probe
SP2	Scan Plane 2 (MPTE)

9.4 References

Relay Board Block Diagram – rev. 04, *page B2-3*

Board Formats – rev. 02, *page A1-69*

Relay Module — Component Side, page M-2

Relay Board Assembly Replacement Procedure – rev. 03, page L1-21

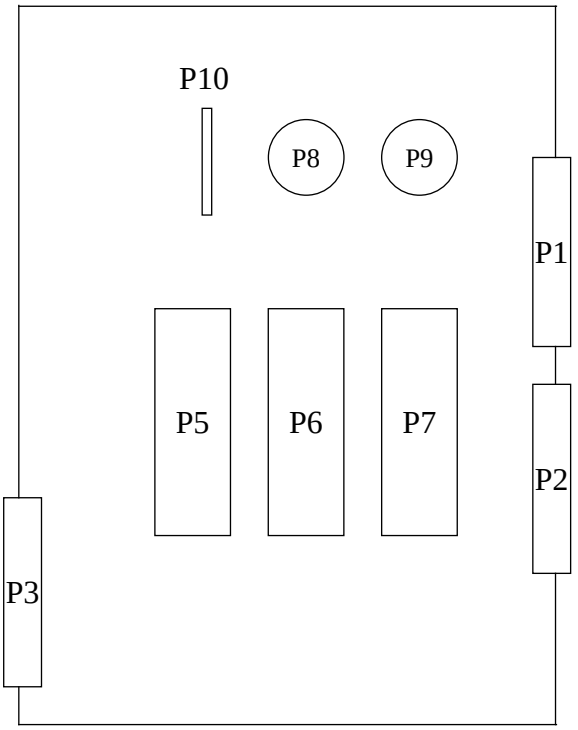
10 Physical Dimensions

The RLY board is attached to the left side panel of the SYSTEM FIVE rack and connects to the motherboard at the back and two transducer bus (XDBUS) boards at the front. The connectors for phased array and annular array probes are attached directly to the Relay Board, while the Doppler probe signals are routed through a 10 pin SIL connector to Doppler connector board (IV&DP). The IV&DP board is attached to the

Relay Board as a daughter-board, but has its own connections to the motherboard for the standby power signals.

11 Connectors and descriptions

11.1 Connector locations



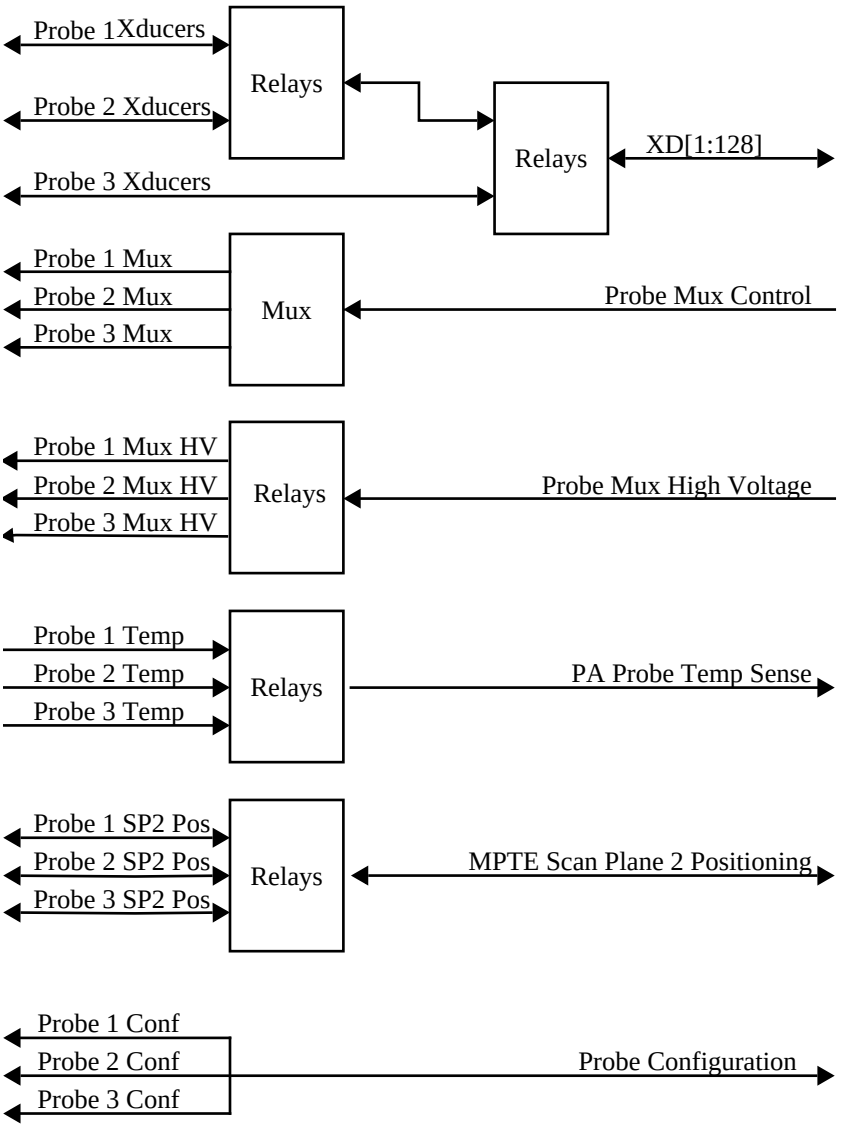
11.2 Phased- and Linear Array Connectors

The transducer channels are routed between the PA probes and the analogue Front End through two sets of 64 dual relays (K1 to K128). One set (K1 to K32 and K65 to K96) is used to switch between probe 1 and 2, while the other set (K33 to K64 and K97 to K128) is used to switch between probe 3 and probe 1 or 2. Latching relays are used in order to reduce the current consumption, and they are activated by discharging the energy stored in capacitors C61 to C76 through (non-latching) relays K153 to K156. Capacitors C61, C62, C65, C66, C69, C70, C73 and C74 are charged to +5 V, and discharging them sets the latching relays, while Capacitors C63, C64, C67, C68, C71, C72, C75 and C76 are charged to -5 V, and discharging them resets the latching relays.

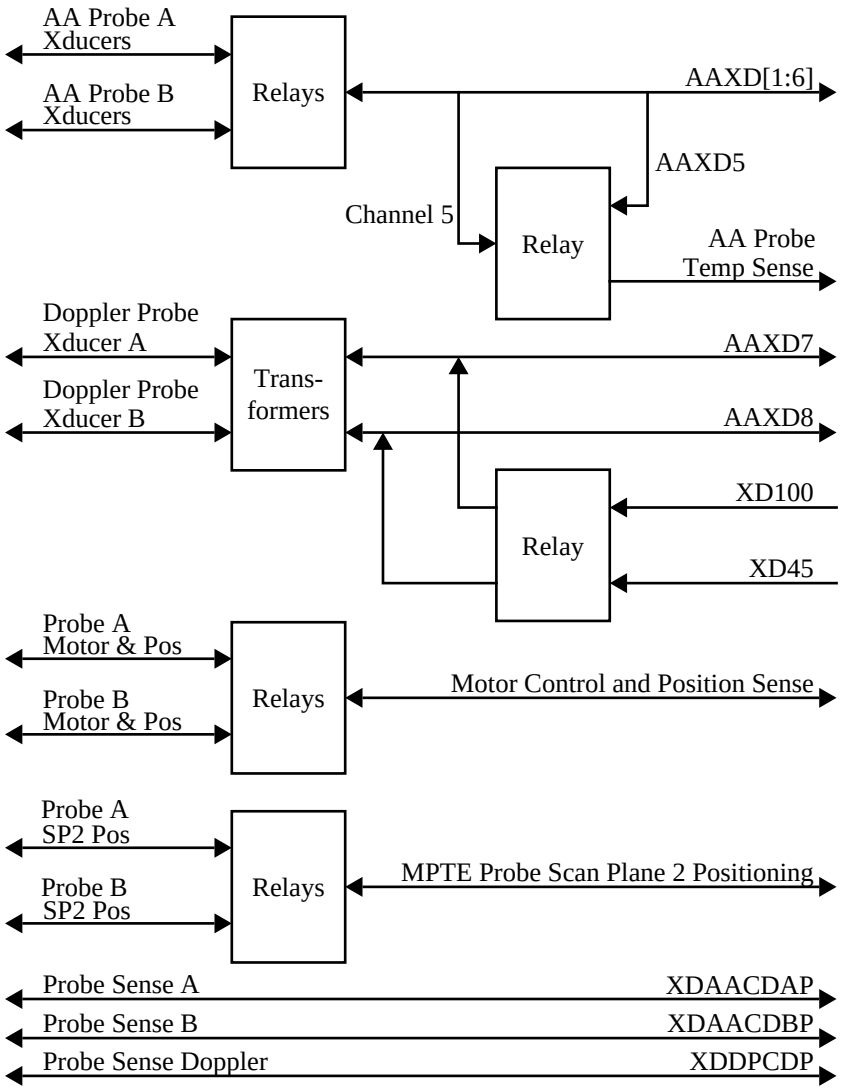
The relay board also routes the probe multiplexer control signals and HV power supplies to the currently active PA probe. The HV power supplies are routed through relays K157 to K159, and are disconnected if the selected probe is not present. Relays K160 to K165 are used to route the temperature sense signal and MPTE scan plane 2 positioning signals between the currently active PA probe and the probe controller board (PRC).

The configuration PROMs in the PA probes are read by the Front End controller board (FEC) through the relay board. The three PA connectors share a common bi-

directional serial bus, and each PA connector has its unique address through two hardwired address pins on the relay board (PA connector 1: address 00, PA connector 2: address 01, PA connector 3: address 10).



11.3 Annular Array and Doppler Probe Connections



The transducer channels for the currently active AA probe are routed to the analogue front end through relays K133 to K138 (probe A) and relays K143 to K148 (probe B). AA probe transducer channel 5 can be routed either to the analogue front end bus (for standard probes) or to the temperature sense input on the probe controller board (for TE probes) through relay K149.

The doppler probe transducer channels are routed to the analog front end bus through balancing transformers T1 and T2. For systems without the probe controller board the transducer channels are also routed to two transmitters on the TX board through relay K150.

Relays K129 to K132 (probe A) and K139 to K142 (probe B) are used to route the motor control and position sense signals between the currently active AA probe and the probe controller board. Probe sense signals for the AA probes and the doppler probe are routed straight through to the probe controller board.

11.4 Control Interface

PAL U4 is used to decode the relay board control signals and controls the different relays through relay drivers U1, U2 and U5. CMOS drivers U6 to U12 provide level shifting to 15V CMOS levels for the probe multiplexer control signals.

Transmitter Board - TX128 – rev. 04

12 Overview

12.1 Abstract

This document describes the transmitter board (TX128 board and TX128-2 board) of GE Vingmed Ultrasound's System FiVe Phased Array Front End. The transmitter board contains 128 individually controlled switched mode transmit channels and provides transmit pulses to the transducer array.

12.2 Document History

Revi-sion	Date	By	Description
01	24. Oct.1994	ALO	Initial release
02	27. Dec.1994	LHS	Updated layout
03	6. Feb. 1998	LHS	Added References
04	20. Oct. 1999	LHS/ JB	Corrected error. Updated (TX128-2) Maintenance Aids moved to Ch.K

12.3 Definitions/Abbreviations/Nomenclature

Please refer to the *Abbreviations, Definitions, Glossary, Terminology, Nomenclature* list starting on *page P-1*.

12.4 References

- *TX-128 Block Diagram – Rev. 02, page B2-4.*
- *Board Revision History* starting on *page H4-1*

13 Inputs

The main inputs to the board are the FE bus which controls the board and high voltage (HV) for the transmitter voltage.

SIGNAL	DESCRIPTION	TYPE	LEVEL
FE_D0-15	Front End Data bus	Digital	TTL
FE_PA0-9	Front End Page Address bus	Digital	TTL
FE_SA0-5	Front End Device Select Address bus	Digital	TTL
TX_TRIG_L	Transmit trigger	Digital	TTL
HV1P	TX High Voltage supply	Analog	0- +80V
HV1N	TX High Voltage supply	Analog	0- -80V
HV2P	TX High Voltage supply	Analog	0- +40V

SIGNAL	DESCRIPTION	TYPE	LEVEL
HV2N	TX High Voltage supply	Analog	0- -40V
VDRIVER	TX Driver Supply	Analog	+ 10V

14 General Description

14.1 Overview

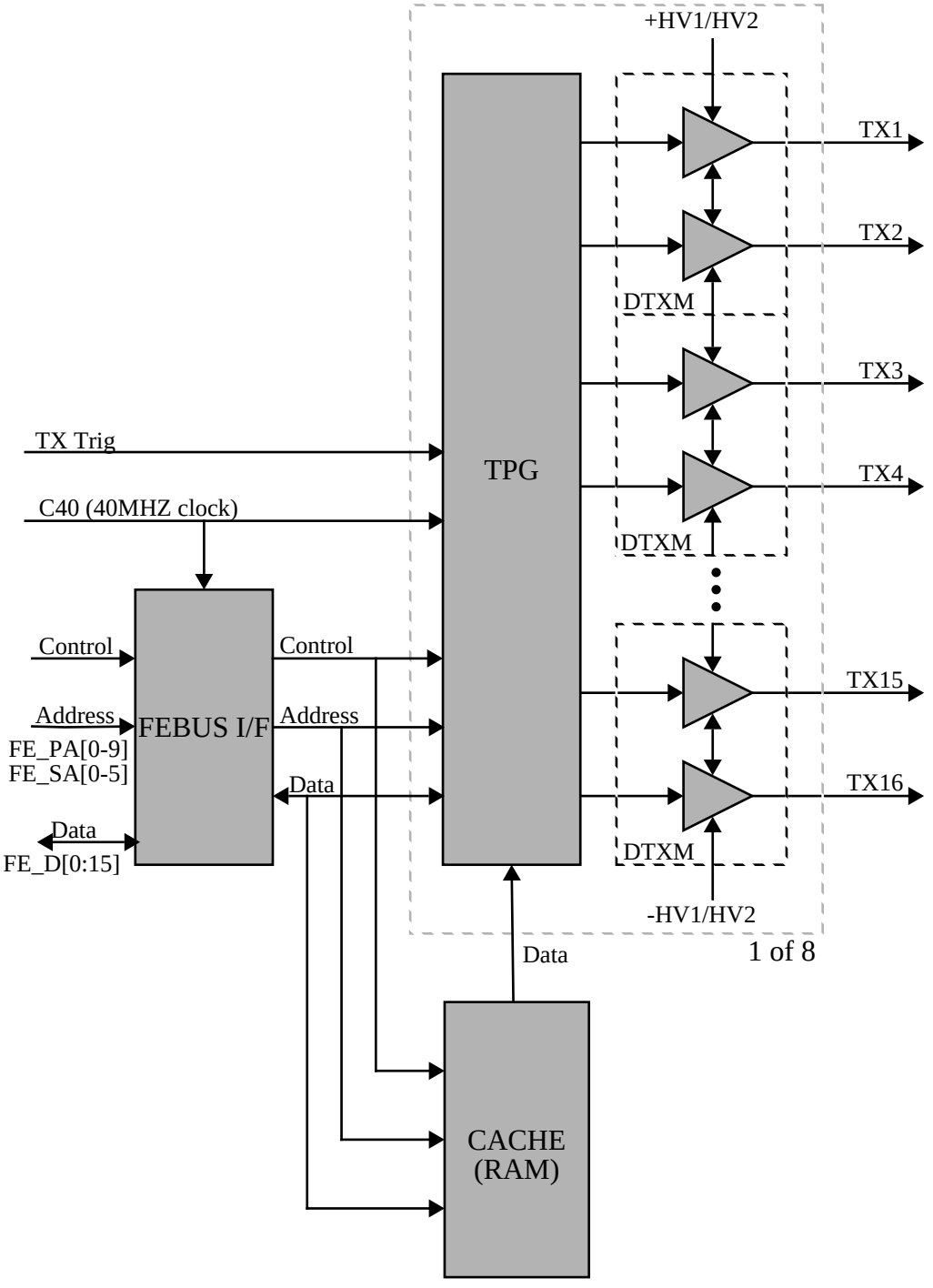


Fig. 14.1 TX 128 board block diagram

Refer to *Fig. 14.1* for a block diagram of the TX128 board.

The TX 128 board contains 64 dual transmitter modules (DTXM, U1 to U64), eight 16 channel transmit pulse generator (TPG) ASICs (U65 to U72) used to control the TX modules, a VRAM cache (U73 to U82), and logic circuitry to interface the TPGs to the front end bus.

14.2 Dual Transmitter Module

The DTXM is a 28 pin SIL hybrid module containing two identical switched mode transmit channels, each consisting of two separate half bridge output stages and a common clamp. Two output stages supplied by different high voltages (HV1 and HV2) are used for each channel in order to enable very fast switching between different power levels in mixed tissue/doppler modes. The output of each channel is clamped to ground during reception to avoid transducer cable ringing at the end of a transmit pulse.

The DTXMs are located at positions U1 to U64.

The outputs of the DTXMs are AC coupled (through capacitors C1 to C128) to prevent high voltage DC from damaging the probe if a transmitter output stage fails. Back-to-back diodes D1 to D128 are used to isolate the transmitters from the probes during reception.

14.3 Transmit Pulse Generator ASIC

The Transmit Pulse Generator (TPG) ASIC is designed to control 16 transmit channels by generating pulses of programmable width, delay and frequency. Each channel has a pair of complementary outputs to drive the upper and lower half of a half bridge output stage. The TPG contains four 11 bit registers for each channel, addressed as shown in table 1. The address bus consists of two parts, a 2 bit function code (FC[1.:0]) and a 4 bit channel address (ADR[3:.0]).

The TPG ASICs are located at positions U65 to U72.

14.4 RAM Cache (VRAM)

The TPG delay registers need to be updated for each vector in a 2D scan in order to set up a new transmit beam direction and focus zone. These parameters must be loaded into the TPGs before firing a new transmit pulse.

The system processor will calculate the transmit delays and load the data into the TPGs through the Front End Controller (FEC) board. In order to avoid Front End Bus activity during data acquisition, all parameters for a complete scan are loaded into dual port VRAMs on the transmitter board. Each vector is stored in one page in the VRAMs and this page is transferred to the TPGs before triggering the next transmit pulse.

The VRAM cache is organized as shown in *Fig. 14.1*. Four transmit pulse generators share a 12 bit wide cache consisting of three 256k x 4 VRAMs (U73 to U75 and U78

to U80). The TPGs and their cache are accessed through bidirectional transceivers (U76, U77, U81 and U82) in order to reduce the capacitive load seen at their outputs.

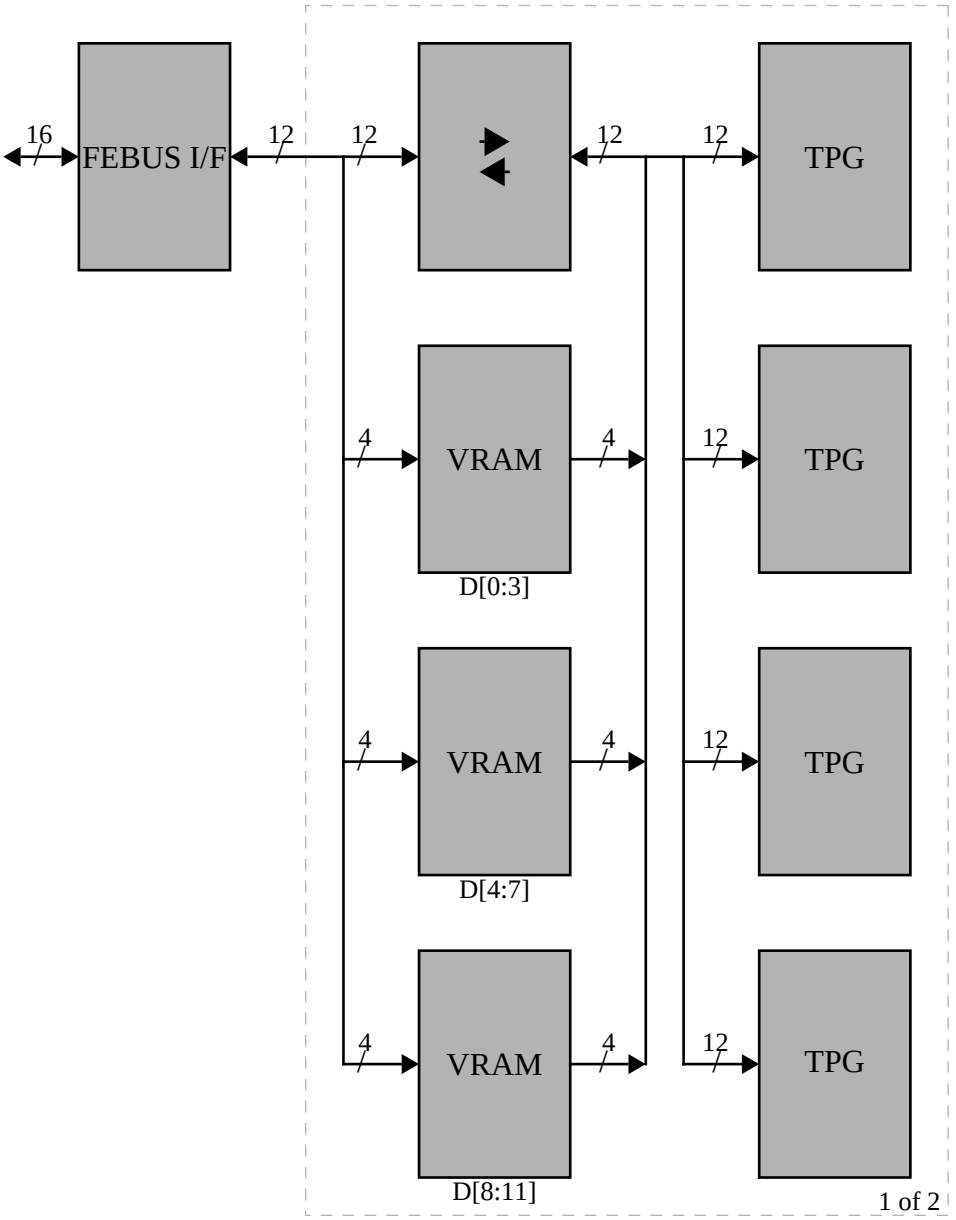
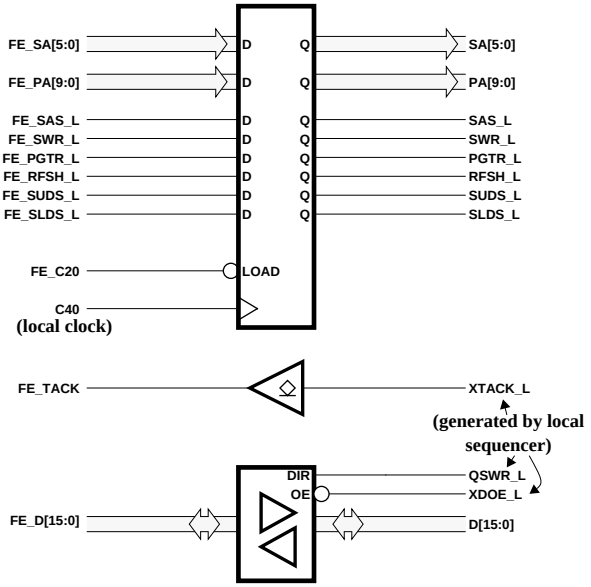


Fig. 14.2 VRAM cache data flow

14.5 FE Bus Interface

The FE Bus interface provides address decoding and buffering between the TPG ASICs and the Front End Bus. Two MACH PLDs (U91 and U92) are used to decode the address bus to access the eight TPG ASICs and their VRAM cache.



15 Outputs

The outputs from the TX128 board are the 128 transmitters channels XD1-128. They are fed from the P4 and P5 connectors over the Front Plane to the Relay board and then to the selected PA connector.

Receiver Board - RX 128

16 Introduction

16.1 Abstract

This document describes the receiver board (RX128 board). The RX128 board contains 128 identical receive channels and provides transmit/receive (T/R) switching, preamplification and time controlled gain (TGC) amplification to signals received from the transducer array. It also supports annular array transducers containing up to eight elements.

16.2 Document History

Revision	Date	By	Description
01	12 Apr. 94	ALO	Initial release.
02	27 Dec. 94	LHS	Updated layout, corrected some minor errors.
03	01Nov.00	JB	Moved maintenance Aid to Ch.K

16.3 Definitions/Abbreviations/Nomenclature

AA	Annular Array
BITE	Built In Test Equipment
PA	Phased Array
T/R	Transmit/Receive (Switch)
TGC	Time Gain Compensation

17 Inputs

Signal	Description	Source	Level
XD 1-128	Phased/Linear Array Transducer channel	Relay Board	Max 200mvrms
AAXD 1-8	Annular Array Transducer channel	Relay Board	Max 200mVrms
Test SIG.	Analog test signal	FEC Board	2Vrms
ATGCVP	TGC control voltage	FEC Board	-10 to+10 V (non inverting)
ATGCVN	TGC control voltage	FEC Board	-10 to +10 V (inverting)
AASEL	Select AA inputs	FEC Board	TTL

18 General Description

18.1 Overview

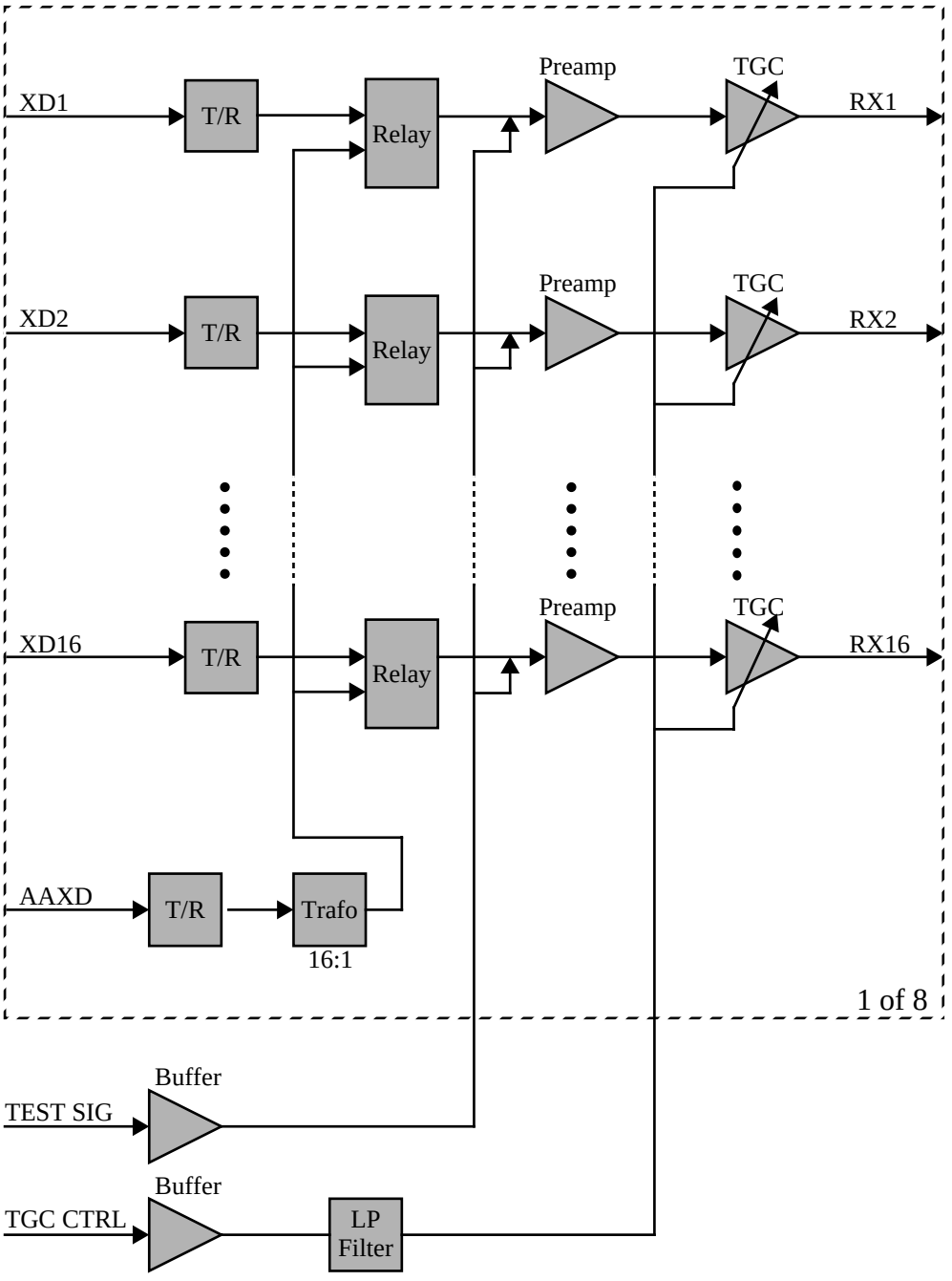


Fig. 18.1 Block diagram

Refer to *Fig. 18.1* for a block diagram of the receiver board.

The RX128 board contains 128 identical receive channels and a common control interface. Each receive channel consists of a T/R switch for transmit signal isolation, a low noise preamplifier, and a voltage controlled TGC amplifier. A set of relays is

used to switch between phased array (PA) mode, where each transducer element is connected to one receive

channel, and annular array (AA) mode, where each transducer element is connected to sixteen receive channels.

18.2 T/R Switches

The T/R switches limit the voltage swing at the receiver inputs during transmission. High voltage diode bridges (D1 to D256) are forward biased as long as the input voltage is between the supply voltages. When the input voltage exceeds the supply voltages, the diodes are reverse biased, isolating the receiver inputs from the transducer.

Voltage regulators U217 to U220 generate the +/- 12 V supply voltages for the T/R switches from the +/- 15 V supplies on the motherboard.

18.3 Preamplifiers

Ultra low noise wide band operational amplifiers (Comlinear CLC425, U1 to U128) are configured as non-inverting amplifiers with a gain of eleven (21 dB). Series resistors between the preamplifier outputs and the inputs of the TGC amplifiers (R1024 to R1152) increase the load seen at the operational amplifier outputs, and provide 6 dB attenuation in combination with the 100 W input impedance of the TGC amplifiers.

A test signal can be injected at the preamplifier inputs for off-line BITE (Built-in Test Equipment) tests. This enables measurements of the gain/phase characteristics of the analogue front end and can also give an indication of transducer faults, since a change in transducer impedance will influence the test signal gain and phase.

18.4 TGC Amplifiers

Dual voltage controlled amplifiers (Analog Devices AD602, U129 to U192) are used to provide time variable gain to the receive signal. Their gain can be varied between -10 and +30 dB by applying a differential control voltage between -625 and +625 mV.

18.5 Annular Array Channels

A set of 64 dual contact bistable relays (K1 to K64) is used to switch between PA mode (128 channels, one receive channel connected to each transducer element) and AA mode (8 channels, sixteen receive channels connected to each transducer element). RF transformers with an impedance ratio of 16:1 (T1 to T8) on the annular array inputs ensure that their input impedance is the same as that of the phased array inputs. A set of T/R switches (D385 to D400) limit the voltage swing at the receiver input during transmission.

18.6 Control and Test Signal Interface

The TGC voltage enters the circuit board as a differential ±20 V signal. Inverting operational amplifiers U221 and U222 scale and filter the TGC voltage. It is then buffered in operational amplifiers U209 to U216, before it is scaled and filtered again and distributed to the gain control inputs of the TGC amplifiers. The filter sections combine to give a third order Bessel low pass filter with a group delay of 2.5 ms.

A common test signal can be injected at the receive channel inputs for test purposes. The test signal is bandwidth limited to 20 MHz in a buffered second order LC filter (L813, C814 and U223) before it is distributed to operational amplifier buffers U193 to U208. Each amplifier drives eight preamplifier inputs through attenuators R257 to R640.

Digital control signal AASEL is used to switch between PA and AA mode (active high selects AA mode) and controls monostable relay K65 through driver transistor Q1. This relay controls the bistable input relays (K1 to K64) by connecting their coils to either a positive voltage (capacitors C815, C816, C819, C820) or a negative voltage (capacitors C817, C818, C821 and C822). The capacitors are charged to either AVCC (+5 V) or AVEE (-5V) through resistors R1597 to R1600. When switching between modes, the capacitors are discharged to ground through the relay coils and the relay contacts are latched into position according to the selected mode.

19 Outputs

The outputs from the RX board are the 128 receiver channels RX1-128.

They are fed to the Beamformer board.

Signal	Description	Destination	Level
RX 1-128	Receive channel n of 128	BF 1 - 4	+ - 3V

Receiver Board - RX 64

20 Introduction

20.1 Abstract

This document describes the 64 channel receiver board (RX64 board) used in low-cost versions of the System Five. This board is based on the RX128 receiver board, with half the number of receive channels and 2:1 multiplexers used for dynamically mapping 128 transducer bus (XDBUS) channels into 64 receive channels for linear array (LA) probes. It also supports annular array transducers containing up to eight elements.

20.2 Document History

Revi-sion	Date	By	Description
01	96.06.21	WL	Initial release. CD rev. 01.
02	97.02.12	WL	CD rev. 02. Minor changes. AA transformer impedance ratio changed to 2:1. New test signal buffer topology.
03	01.11.00	JB	Moved Maintenance Aid to Ch.A

20.3 Definitions/Abbreviations/Nomenclature

AA	Annular Array
BITE	Built In Test Equipment
CW	Continuous Wave (Doppler)
FPGA	Field Programmable Gate Array
LA	Linear Array
PA	Phased Array
T/R	Transmit/Receive (Switch)
TGC	Time Gain Compensation
XDBUS	Transducer Bus

21 General Description

21.1 Overview

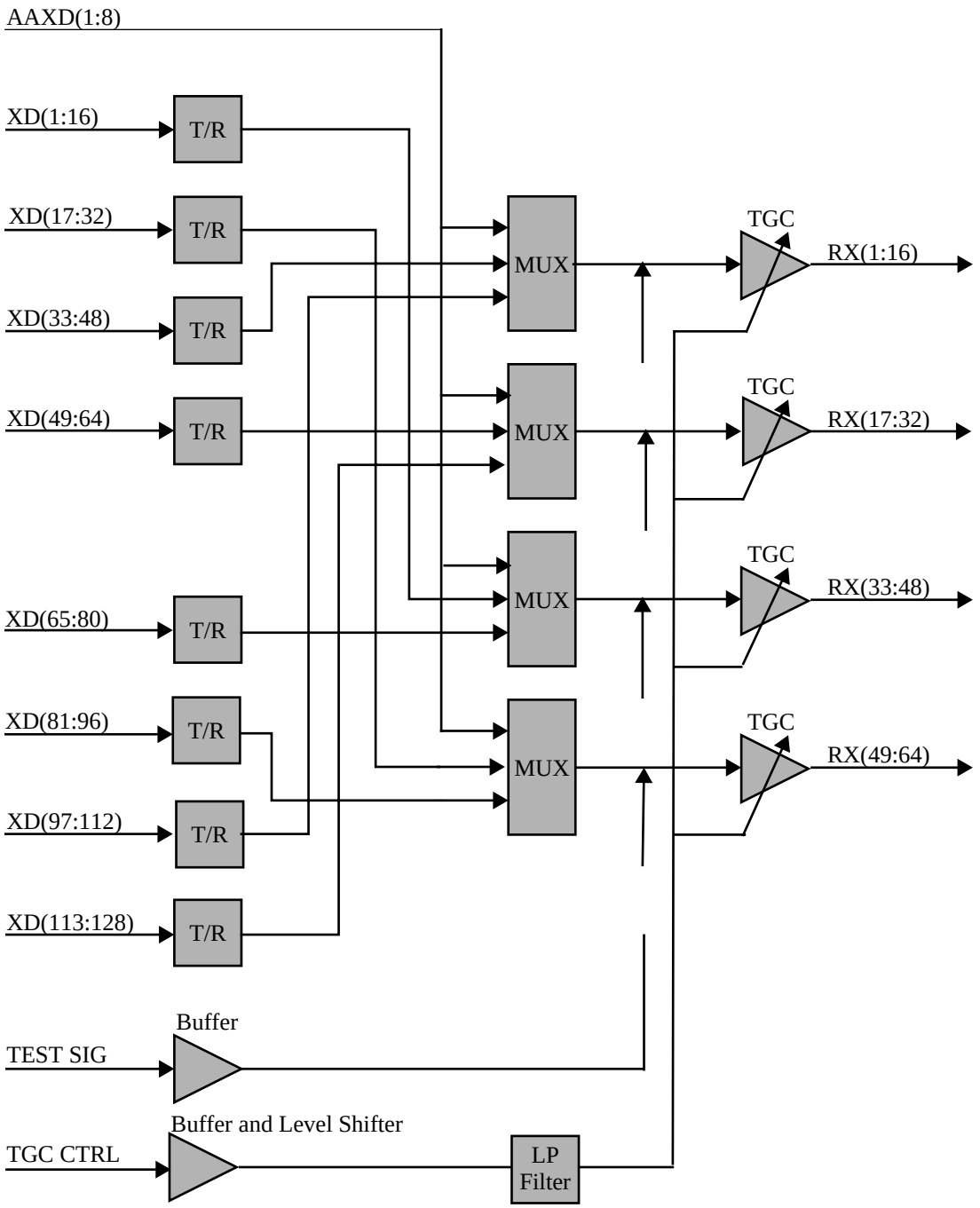


Fig. 21.1 Block diagram

Refer to *Fig. 18.1* for a block diagram of the receiver board.

The RX64 board contains 64 identical receive channels and a common control interface. Each receive channel consists of an input multiplexer preceded by a T/R switch for each multiplexer input and a low-noise voltage controlled TGC amplifier.

21.2 T/R Switches

The T/R switches limit the voltage swing at the multiplexer inputs during transmission. High voltage diode bridges (D1 to D256 for the PA/LA inputs, D385 to D400 for the AA inputs) are forward biased as long as the input voltage is between the supply voltages. When the input voltage exceeds the supply voltages, the diodes are reverse biased, isolating the receiver inputs from the transducer.

RF transformers with an impedance ratio of 2:1 (T1 to T8) on the annular array inputs ensure that their input impedance is the approximately the same as that of the phased array inputs (One AA input is connected to eight receive channels, so that without a transformer, the AA input impedance would be only 1/8 of the PA/LA input impedance).

Voltage regulators U105 to U108 generate the +/-12 V supply voltages for the T/R switches from the +/- 15 V supplies on the motherboard. The +12V regulators are also used to provide the positive supplies for the input multiplexers.

21.3 Input Multiplexers

Quad low on-resistance switches (Siliconix DG641, U1 to U64) are used to connect the output of the T/R switches to the preamplifier inputs depending on the currently active probe.

The following modes are supported:

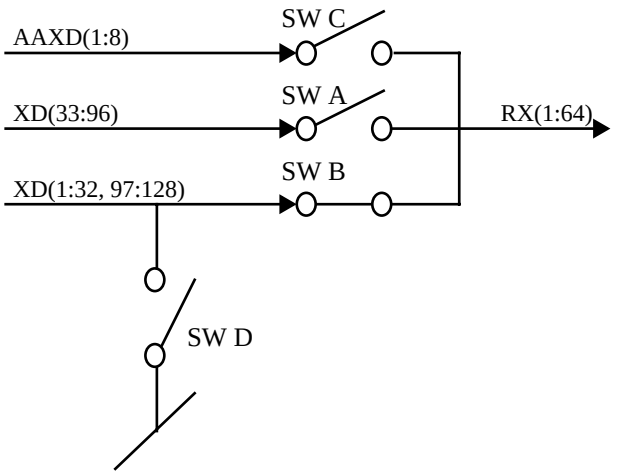
Mode 1: For linear array (LA) probes, 64 consecutive probe elements are connected to the receive channels, with the selected elements sliding along the array from pulse to pulse. The channel mapping is dynamically updated.

Mode 2: For phased array (PA) probes, the 64 centre elements of the probe (transducer channels 33 to 96) are connected to the receive channels. The channel mapping is fixed.

Mode 3: For annular array (AA) and standalone doppler probes, one probe element is connected to eight receive channels. The channel mapping is fixed.

Mode 4: In test mode, transducer channels 1 to 32 and 97 to 128 are connected to the receive channels. The channel mapping is fixed.

Each multiplexer consists of four switches (A, B, C and D) configured as shown in *Fig. 21.2*. Switch D connects unused inputs to ground in order to reduce CW crosstalk for PA probes.



Mode	SW A	SW B	SW C	SW D	Description
1A	On	Off	Off	Off	For Linear Array probes
1B	Off	On	Off	Off	
2	On	Off	Off	On	For Phased Array probes
3	Off	Off	On	Off	For Annular Array probes
4	Off	On	Off	Off	Test mode

Fig. 21.2 Multiplexer switch configuration

21.4 TGC Amplifiers

Dual ultra-low noise variable gain amplifiers (Analog Devices AD604, U1 to U32) provide time variable gain to the multiplexed transducer signals. The amplifiers consist of two cascaded sections: a fixed gain preamplifier with a gain of 14 dB is followed by a voltage controlled amplifier with a gain that can be varied between -14 and +34 dB by applying a control voltage between 0.1 and 2.9 V. A control voltage below about 50 mV shuts down the voltage controlled amplifier.

A test signal can be injected at the input of the preamplifiers for off-line BITE (Built-in Test Equipment) tests. This enables measurements of the gain/phase characteristics of the analog front end and can also give an indication of transducer faults, since a change in transducer impedance will influence the test signal gain and phase.

21.5 TGC Control and Test Signal Interface

The TGC control voltage enters the circuit board as a differential ±20 V signal and is converted to a single-ended ±10 V signal in -6 dB differential line receiver U110 (Analog Devices SSM-2143), before it is scaled and filtered in one half of dual opera-

tional amplifier U112. The output of voltage reference U111 is inverted in the other half of U112 and added to the TGC control voltage at the output of the line receiver in order to generate a control voltage range of about 0 to 2.9 V. The TGC control voltage is then buffered by one half of dual operational amplifiers U117 to U120, before it is filtered again (R777 to R780 and C691 to C694) and distributed to the gain control inputs of the TGC amplifiers. The filter sections combine to give a third order Bessel low pass response with a group delay of about 2 ms. The output of reference U111 is also buffered by the other half of dual operational amplifiers U117 to U120 and distributed to the reference inputs of the voltage controlled amplifiers.

A common test signal can be injected at the preamplifier inputs for test purposes. Operational amplifiers U122 and U123 buffer the test signal input, with their output enable pins driven by digital control signal TESTM through hex inverter U113. The test signal gain can be set to either 0 dB (TESTM = LOW) or -21 dB (TESTM = HIGH, used for dithering). The test signal is then distributed to operational amplifier buffers U97 to U104. Each amplifier drives eight preamplifier inputs through attenuators R449 to R640.

21.6 Multiplexer Control Interface

Two identically programmed Altera EPF8282A FPGAs (U115 and U116) are used to control the input multiplexers. They can be programmed by loading their configuration data either from an on-board Altera EPC1064 configuration EPROM (U121) or from the FEbus through tri-state buffer U114.

Each FPGA contains four eight bit serial-in-parallel-out shift registers and a 32 bit wide hold register. In linear array mode, the multiplexer data are loaded into the shift registers on the falling edge of shift clock RMX_SCL, and the contents of the shift registers are then clocked into the hold register on the rising edge of strobe signal RMX_LE. In all the other modes, the contents of the hold register is fixed. Refer to the table below for details. See also section *21.3*. Note that a switch is turned on when its control input is high.

Mode	AASEL	PASEL	Out A	Out B	Out C	Out D	Description
1	L	L	SDA	NOT (SDA)	L	L	LA mode
2	L	H	H	L	L	H	PA mode
3	H	L	L	L	H	L	AA mode
4	H	H	L	H	L	L	Test mode

The table below shows the mapping between the shift register data and the 64 receive channels in linear array mode. Note that data for the highest channel numbers are loaded first.

	D_N	D_{N+1}	D_{N+2}	D_{N+3}	D_{N+4}	D_{N+5}	D_{N+6}	D_{N+7}
MUX_SDA1	RX1	RX2	RX3	RX4	RX5	RX6	RX7	RX8
MUX_SDA2	RX9	RX10	RX11	R12	RX13	RX14	RX15	RX16

	D_N	D_{N+1}	D_{N+2}	D_{N+3}	D_{N+4}	D_{N+5}	D_{N+6}	D_{N+7}
MUX_SDA3	RX17	RX18	RX19	RX20	RX21	RX22	RX23	RX24
MUX_SDA4	RX25	RX26	RX27	RX28	RX29	RX30	RX31	RX32
MUX_SDA5	RX33	RX34	RX35	RX36	RX37	RX38	RX39	RX40
MUX_SDA6	RX41	RX42	RX43	RX44	RX45	RX46	RX47	RX48
MUX_SDA7	RX49	RX50	RX51	RX52	RX53	RX54	RX55	RX56
MUX_SDA8	RX57	RX58	RX59	RX60	RX61	RX62	RX63	RX64

Probe Controller Board - PRC – rev. 04

22 Overview

22.1 Abstract

This document is a description of the Probe Controller board (PRC) in System FiVe. The Probe Controller Board performs multiple tasks; one version of the board is mainly concerned with reading and controlling probe parameters related to the Annular Array probes, Stand Alone Doppler probes and TEE probes. The board resides on the Front End Bus, and is fully controlled by the Front End Controller Board, with the exception of the onboard XDCTRL board which is controlled directly by the CPU board.

22.2 Document History

Rev.	Date	Sign.	Description
01	4 May 1994	GRL	First version (for artw.B and onwards).
02	22 Nov. 1994	GRL	Added document history and definitions.
03	20 Oct. 1999	LHS	Updated content.
04	1. Oct. 2000	LHS/ JB	Corrected errors. Removed IVUS-descriptions (never included in System FiVe). Moved Maintenance Aid to Ch.K.

22.3 Definitions/Abbreviations/Nomenclature

Please refer to the *Abbreviations, Definitions, Glossary, Terminology, Nomenclature* list starting on *page P-1*.

22.4 References

- *Probe Controller Block Diagram – rev. 02, page B2-6*
- *Board Revision History* starting on *page H4-1*

23 Inputs

The main inputs to the board are 3 probe sense lines for AA and DP probes (XDAACDA, XDAACDB, XDDPCD), 2 temp sense lines for TEE probes (AA_TEMPIN, PA_TEMPIN) and position signals for AA probes (AAPOSP, AAPOSN).

Table 3: “Main” Inputs

SIGNAL	DESCRIPTION	SOURCE	LEVEL
XDAACDA	Probe Code, AA probe A	AA probe	0-12V_{DC}
XDAACDB	Probe Code, AA probe B	AA probe	0-12V_{DC}
XDDPCD	Probe Code, Doppler Probe	DP probe	0-12V_{DC}

Table 3: "Main" Inputs

SIGNAL	DESCRIPTION	SOURCE	LEVEL
AATEMPIN	AA Temperature Sense (AD590)	AA TEE probe	5.15-5.68V_{DC}
PATEMPIN	PA Temperature Sense (NTC)	PA TEE probe	0.70-1.17V_{DC}
AAPOSP	Position+ for AA probes	AA probe	+/- 13 V_{PP}
AAPOSN	Position- for AA probes	AA probe	0V
RF_INP	RF data input	Motor pod	0 - 1 V_{rms}

24 Descriptions

24.1 Annular Array and Doppler Transmitter

In order to support Annular Array and Stand Alone Doppler probes, 8 transmitters for a maximum of 6 annular channels and 2 Doppler channels, are implemented. (Note that the TXboard can also be used as Doppler transmitters). The receivers are located on the RXboard as for the Phased- and Linear Array probes. When an Annular Array probe is running, the XDCTRL board (see *section 24.4*) outputs Tissue and Flow Line Request signals which are fed to the FEC board. These signals are used to generate transmit trigger pulses (TX_TR_L or TTR_L) which are fed to a Transmit Pulse Generator (TPG) ASIC on the PRC board. This is a device which can output up to 16 different differential transmit pulses at TTL level. The FEC board programs the TPG with the proper pulse width, frequency and delay (between channels). 8 of the TPG output channels are used on the PRC board, and they are fed to 4 so-called dual transmitter modules (DTXM) (U61-U64) supplied with two high voltages, HV1 and HV2, which are selected depending on type of mode (PW or CW). A +10V VDRIVER voltage feeds the MOSFET drivers on the DTXMs. During reception the MOSFET outputs are clamped to ground to reduce ringing. All outputs are low pass filtered to reduce EMI emission.

24.2 Annular Array and Stand Alone Doppler Probe Sense

The Annular Array probes and Stand Alone Doppler probes are recognized in the same way as they are in the CFM-7XX and CFM-8XX products. A 2.5V voltage reference (VR1) will always be in parallel with one of the resistors selected by the multiplexer, U6 (by PS_CUR[0:1]). Thus, depending on the size of the resistor, one of four constant currents can be fed through the probe code resistor. The currents are ranging from 3.3uA to 1mA in order to cover the range of probe code resistors from 0 to 3.3 Mohm. Three different probe resistors can be selected through the multiplexer, U4 (by PS_PRB[0:1]). In addition, a fourth onboard resistor can be selected for automatic test purposes.

A voltage will develop across the probe code resistor. This voltage is buffered, low pass filtered (150Hz) and scaled (A=0.4) in U11, before fed (as AAPRBCD) to a multiplexing A/D converter (U93). The digitized values (D[0:7]) are read by the FEC board, which then forwards the probe type information to the CPU board.

24.3 Temperature Sensors

24.3.1 Annular Array TEE Probes

A temperature sensor is implemented for monitoring the temperature in the TEE probes. A reference voltage, 10.00V, is scaled down and fed to the temperature transducer (AD590), inside the TEE probe tip. This device outputs a current proportional to the temperature (1uA/Kelvin) or

$$I(T) = 273.2 + T, \quad [I\{uA\}, T\{^oC\}] \tag{24.1}$$

A voltage proportional to the current, develops on the inverting input of the instrumentation amplifier, AD620 (U12). A reference voltage corresponding to ~15°C, is connected to the non-inverting input. The voltage difference is then amplified (U12), low pass filtered (U7) and fed to the A/D converter (U93) for digitizing and transfer to the FEC board.

The temperature is displayed on the monitor. The system monitors the temperature and when exceeding a certain limit, (typ. 41.1 °C) necessary actions will be taken in SW to prevent further scanning.

A motor current shutoff mechanism is implemented: The amplified and low pass filtered voltage (AA_TEMP) is fed to two comparators (U10), so that when exceeding certain thresholds (below15 °C on the low end and above 41.3 °C on the high end), a TEMPOK signal goes low, turning a MOTOFF signal high, in turn disconnecting the motor and position lines in two relays (K2, K3).

As a self test of the circuitry, 3 test resistors can be selected (K6, K23, K24) by TMP_SEL[0:2] to simulate three different known temperatures.

24.3.2 Phased Array TEE Probes

A similar circuit as described above, is also provided for the Phased Array TEE probes. A PA_TEMPIN voltage is proportional to the temperature at a thermistor located inside the

probe tip. This voltage is compared to a “0-volt output level” set at ~15°C. From the output of U13 the signal path is similar to above. Since the thermistor is nonlinear, correction for this is done in a look-up table in software.

24.4 Annular Array Probe Motor Control

The Motor and Position Control of the Annular Array probes is implemented with the same circuitry as in the CFM-7XX/-8XX systems. The XDCTRL board is a plug-in add-on module utilizing exactly the same pcb as the CFMs do. The power amplifier is integrated into the artwork of the Probe Controller board. The XDCTRL board communicates serially (U18, U94) with the CPU on two control lines, TXD1 and RXD1.

A reference sweep (DAC) is generated on the XDCTRL board. This signal is compared to the position (POSP, POSN) coming back from the position coil in the probe. The error signal is applied to the motor coil after linear control (not shown on the block diagram) and power amplification, moving the element in the desired direction. The motor driver (U27/U96) is integrated into a closed loop amplifier (U14). It takes the control voltage, PA, from the XDCTRL board through a relay (K16) and provides sufficient current drive for the motor coil in the probe. The output of the current am-

plifier is fed through three different relays: In K10 a test load can be selected, K9 is controlled by a watchdog signal gated with a current limit signal (XDCLIM_L) and K2 is controlled by the TEE temperature dependant MOT_OFF signal.

The probe motor current will develop a voltage across a 0.2 ohm current sense resistor. This voltage is amplified, rectified, low pass filtered and compared (U76) to a threshold (1.6V) setting a current overload limit. In case of an overload condition, an XDCLIM_L signal will turn off the motor drive (K9). As a safety precaution, during no mode operation or if the probe element is jammed, a BWDOG_L signal goes inactive (high), shutting off the motor signals (K9) to the probe after 3 seconds.

The XDCTRL board provides several status signals (latch on block diagram) which reflect the sweep direction and type. These signals are used by the FEC to synchronize transmit pulse triggering on the PRC board and data reception on the BF and RFT boards.

24.5 Front End Bus Interface

The interface with the Front End Controller board over the Front End Bus conforms with the System 5 FE-bus standard. The bus consists of a 16 bit bidirectional data bus, a 10 bit page address bus, PA[0:9], and a 6 bit select address bus, SA[0:5]. In addition there are control signals like address strobes, reset, data acknowledge etc.

An address decoder, “PRCFINT0” (U20), is provided for generating the onboard device selects, (12-14 chip select lines, a number of register (U83-U87) output signals and one read-back register (U88)).

24.6 Clock Distribution

The PRC board receives two differential 40MHz clocks on ECL level, C40I1H/ C40I1L (U40) and C40Q1H/C40Q1L (U19) from the FEC board. C40I1 is fed through an ECL to TTL clock converter chip (U30), providing several 40 MHz clocks on TTL level. C40I1 and SRES1_L are used to generate a 20MHz clock (C20) in a flip-flop (U59). This clock is converted to TTL and distributed to the IV sections. C40I1 and C40Q1 are exclusive or’ed (U19, U29) to generate 160MHz, then divided by 5 in a counter (U89) to obtain 32MHz (for the IV option).

25 Control

As mentioned in section *section 22*, the PRC board is controlled by the FEC board over the FE-bus. The XDCTRL board is controlled by the CPU board on two RS-232 lines.

The module revision of the PRC board is programmed in a serial EEPROM (U48) which can be read by the FEC board.

26 Outputs

The main outputs from the board are the Annular Array and Stand Alone Doppler transmit channels (AA_XD[1:8]), motor drives for AA probes (AAMOTP/N) and probe

and temperature sense data sent over the FE data bus (FE_D[0:15]) to the FEC board.

Table 4: “Main” Outputs

SIGNAL	DESRIPTION	DESTINATION	LEVEL
AAXD1-6	AA Transmit Channels 1-6	AA probe	+/- 130V_{pp} max
AAXD7-81	DP Transmit Channels 1-2	DP probe	+/- 130V_{pp} max
AAMOTP	Motor + for AA probes	AA probe	+/- 0.5V
AAMOTN	Motor - for AA probes	AA probe	+/- 13V_{pp}

Beam Former Board - BF

27 Overview

27.1 Abstract

This document describes the Beam Former Board's Digital Phased Array Front End. (20 MHz / 12 bit ADC version).

The Beam Former board converts the analog RF-input signal from 32 transducer elements to digital form and performs receiver focusing and steering by digital delay.

All digital signal processing to filter and delay each channel is performed in two ASICs (named FOCUSOR and BEAM ADDER).

The output of this board is either connected to a new BF board (to increase the number of channels) or to the RFT board for digital RF processing.

By feeding the same ADC data to several ASIC sets, Multiple Line Acquisition (MLA) is accommodated.

The BF board is also used to A/D convert and focus the RF signal from Annular Array probes. Each AA-element is connected (on the receiver board) to several RF-input channels of the BF board to increase the total Signal/Noise ratio. Beam steering is performed by mechanically moving the transducer under control of the Probe Controller board (PRC board).

27.2 Document History

Revision	Date	By	Description
01	21.Mar.1994	A.Lohne	Initial release.
02	21.Mar.1995	LHS	Added A/D converter section
03	1.Oct.2000	LHS/JB	Updated. BF Board Testing moved to Ch.K.

Table 5: Document History.

27.3 Nomenclature

ASIC: Application Specific Integrated Circuit
FOC: FOCUSOR ASIC. Custom made Beamforming circuit
BA: BEAMADDER ASIC. Custom made Beamforming circuit
ADC: Analog to Digital Converter
MLA: Multiple Line Acquisition
PA: Phased Array
AA: Annular Array
RX: Receive
TX: Transmit
FEC: Front End Controller
PRC: Probe Controller

28 Inputs

The main inputs to the board are the FE-bus which controls the board and the RX analog signal from the RX board. 32 RX channels are input to each of the BF boards.

Table 6: Inputs

SIGNAL	DESCRIPTION	SOURCE	LEVEL
RX1-32	Receiver signals	RX-128	Analog
FE_D0-15	Front End Data bus	FEC	TTL
FE_PA0-9	Front End Page address bus	FEC	TTL
FE_SA0-5	Front End Device Select Address bus	FEC	TTL
SYNC_L	Receive Synchronization	FEC	TTL

29 Beam Former Board Functional Specification

29.1 Overview

The Beam Former Board (BF Board) contains the A/D converters and the ASICs named FOCUSOR (FOC) and BEAM ADDER (BA). The BF Board accepts 32 analog channels as input and converts each to a 12 bit word at a sampling rate of 20 MHz.

A 128 channel System will require 4 BF Boards. All board will be identical - their slot will determine which channels each board is handling.

The digitized samples at the ADC output are input to the FOCs (4 ADCs pr. FOC) whose outputs go to a BA (4 FOCs pr. BA). The output of this BA (BA Level 2) is the sum of 16 channels and it is summed together with the output from the other BA Level 2 and the output from any previous BF board in the BA Level 3 (see *Fig. 29.1*).

These ASICs will sum all the 32 channels together with appropriate delay to give optimal receive focusing and beam steering as a function of time. All focusing and steering parameters for a scan are stored in VRAMs on the BF Board. The output of

BF Board is a 19 bits word updated at 20 MHz. This output can be added to any succeeding board if more channels are desirable as shown in.*Fig. 29.1*

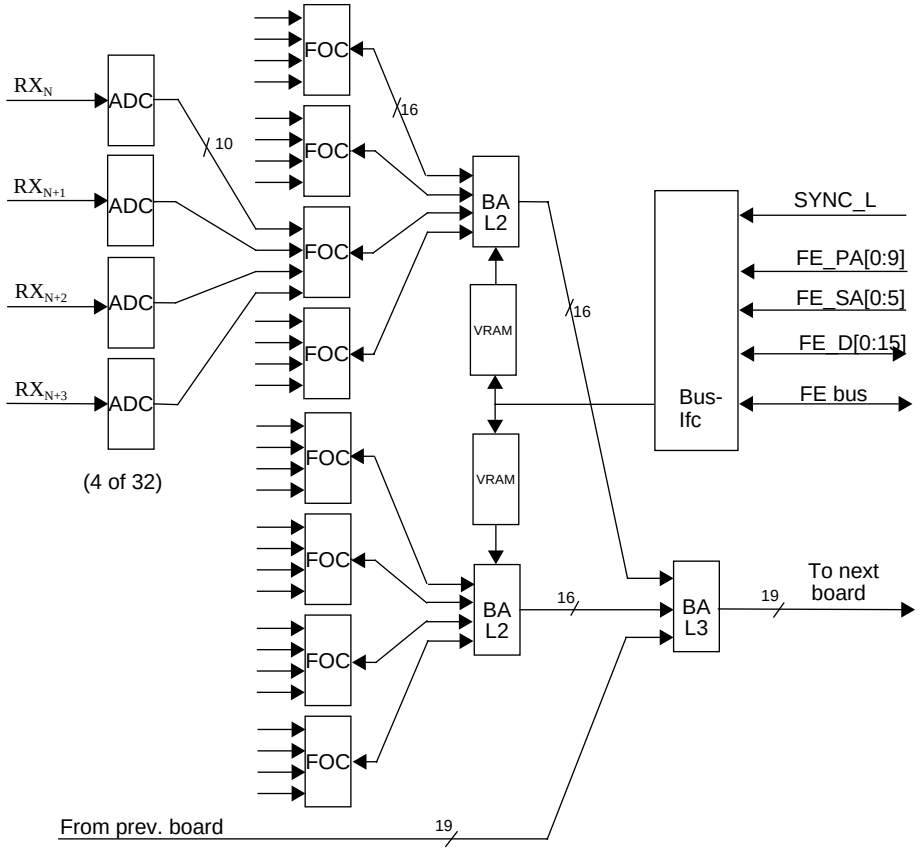


Fig. 29.1 BF Board Block diagram

Multiple Line Acquisition (MLA) is supported by adding a complete ASIC set for each additional line. The input data for the additional FOCs will be the same as for the first line, but the FOCs are set up with different parameters.

29.2 A/D Converter section.

This version is using a 12 bit/20 MHz ADC from AT&T (CSPA1220). It contains an internal T/H and a voltage reference.

The input signal (coming from the Receiver board) is isolated and converted to a differential signal centered around the mid range voltage of the ADC (2.25 Volt) by a 1:0.5:0.5 RF-transformer, and low pass filtered (-3 dB at 10 MHz) by a LC filter.

The digital output from CSPA1220 is buffered and connected to one FOC input port for each MLA.

A block diagram of an ADC section is shown in *Fig. 29.2*

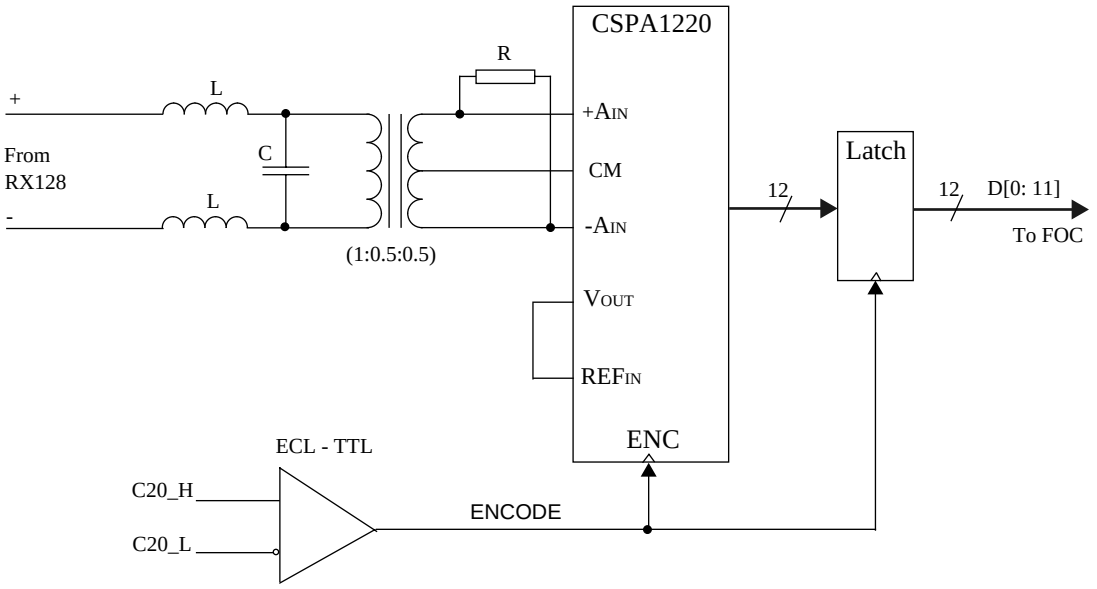


Fig. 29.2 ADC Section Block Diagram

29.3 Beamforming Section.

The digital beamformer uses two ASICs (Application Specific Integrated Circuits) to filter and delay each individual channel and sum all channels. The ASICs are called FOCUSOR (FOC) and BEAM ADDER (BA). Their master clock is 40 MHz and they are synchronized with a SYNC* signal (coming from Front End Controller) which is synchronized with the transmit trigger.

29.3.1 FOCUSOR ASIC

The FOCUSOR accepts digitized signals (up to 12 bit) from four elements of an electronically steered transducer. It can be programmed to support a data format of either 2's complement or offset binary. The four ports are passed through several stages of digital processing prior to being combined to a single 16 bit data-flow at 20 MHz on the output. Additionally, the chip delivers three status signals (CHIP_VALID, DATA_READY and DATA_ERROR) that tell the subsequent stage (the BA) when to accept data.

The signal processing algorithms are controlled by a set of parameters that must be downloaded into the FOCUSOR from the controlling system: The system processor loads the data (through the FEC board) for a complete scan into Video RAMs located on the Beam Former board before the scan is started. During the scan - in the time slot between the end of one beam and the firing of next - the parameters for the next beam are read from the VRAMs into the FOCs. In order to reduce this download

time the serial data from the VRAM is buffered on the BA and transferred in parallel to the FOCUSOR.

Four FOCUSORs require one 256k*4bit VRAM for parameter storage. 8 FOCUSORs and 2 VRAMs are needed to support 32 RF channels for each MLA.

29.3.2 BEAM ADDER ASIC

The BEAM ADDER can be configured for two slightly different functions: BA Level 2 (BAL2) and BA Level 3 (BAL3).

BAL2 accepts the 16 bit data word from four FOCUSORs, and sums and scales these inputs to one 22 bit output word: DATA_OUT[0:21]. 16 bit (DATA_OUT[2:17]) are used for input to BAL3. Additionally, the chip delivers three status signals (CHIP_VALID, DATA_READY and DATA_ERROR) that tells the subsequent stage (the BAL3) when to accept data. BAL2 will also be used for parameter storage during the FOC parameter loading. We will need 2 BAL2s for each MLA.

BAL3 accepts the data from two BAs Level 2 (each 16 bit) and one 22 bit data word from any preceding board, and sums and scales these inputs to one 22 bit word. In a 128 channel Front End a data word length of 19 bit is sufficient, so to reduce the number of signals between the BF boards only the 19 LSBs are used. This 19 bit word is the output of the Beam Former board and will be the input for any succeeding BF board or for the Scan Line Processor in the RFT board. Additionally, the chip delivers three status signals (see above) that tell the subsequent stage (next BF board or the RFT board) when to accept data. 1 BAL3 is needed for each MLA.

The BF board therefore uses 3 BEAM ADDERs to support 32 RF channels for each MLA.

29.4 Video RAM and Parameter loading.

The Beam Former parameters need to be updated for each beam in a 2D scan (new steering delay) and one scan may consist of two or more different Scan Modes requiring different setup of the FOCUSOR. These parameters must be loaded into the FOCUSOR before the firing of a new beam. For a full 128 channel, 2 simultaneous lines (MLA) front end there will be 2 Mbytes of parameter data for a complete scan.

The System processor calculates all these parameters and (through the Front End Controller) loads the data into the Beam Former board. To avoid Front End Bus activity during the acquisition period, all parameter data for a complete sweep are loaded into Dual Port VRAMs located on the Beam Former board. Each beam has one Page in the VRAMs and this page is transferred into the FOCUSOR after the current beam is acquired:

- First the page is transferred into the Parameter RAM inside BAL2 in 4 bit serial form clocked by a BA generated SCLK. This action is triggered by LD_DATA.
- Then the Parameter RAM is transferred to all four FOCs connected to this BAL2 by reversing the direction of the busses between the BA and the FOCs. This action is triggered by PGM_FOC.

The VRAM is a high speed, dual port CMOS dynamic random access memory containing 1,048,576 bits. They can be accessed either by a four bit wide DRAM port or by a 512 x 4 bits serial access memory (SAM) port. Data can be transferred bidirectionally between the DRAM and the SAM. In our application the DRAM port is used

for Front End Bus access and the SAM port is used for transferring one page of 256 x 4 bits into four FOCUSORs.

29.5 Clock Distribution

It is essential to control the skew of the Encode signal to all ADCs. This skew (measured on inside one BF board or between two BF boards) will affect the accuracy of the Beam Forming. The Encode signal for CSPA1220 is a 20 MHz clock (C20) that is produced by dividing the 40 MHz Master clock by 2 in a D Flip-Flop. To ensure that C20 is in the same phase on all BF boards the Flip-Flop is reset by the Synchronous Reset signal SRES* after power up.

In addition the clocks must be protected from digital noise to avoid clock jitter. To accommodate this ECL logic is used to distribute the C40 Master clock between the boards and for C40 and C20 internally on the BF board.

Internally on the BF board the C40 and C20 clocks are distributed to circuits located far apart: All ADCs, FOCUSORs and BEAM ADDERs use one of these clocks. We have made sure the delay and noise aspect (including jitter) are acceptable by:

- using “low-skew” Clock Drivers (High Speed ECL)
- routing the clock signal as an “analog signal” with a characteristic impedance of 50 ohm for the track
- using “tree-distribution” and keeping the routing distance approximately equal for each part of the tree

Note that the CSPA1220 requires a 50% Duty Cycle of ±5%.

29.6 Front End Bus Interface

The interface signals for the parameter cache transaction sequencer are shown in *Fig. 29.3*.

The Beam Former board is accessed from the FEC board through a 9 bit Page Address bus, a 5 bit Select Address bus, an 8 bit data bus and 6 control bits.

Since all BF boards shall be identical the address decoding for selecting one particular board is slot dependent. The 16 bit FE Data Bus is utilized by connecting alternating BF board slots to the low byte (FE_D[0:7]) and high byte (FE_D[8:15]), respectively, in order to improve the data rate (see *Table 7:*).

The slot signals SLOT[0:1] are pulled high on the board, but will be grounded on the motherboard according to *Table 7:*

Slot	Data	SDS*	SLOT0	SLOT1
BF1	FE_D[0:7]	FE_SLDS*	L	L
BF2	FE_D[8:15]	FE_SUDS*	L	H
BF3	FE_D[0:7]	FE_SLDS*	H	L
BF4	FE_D[8:15]	FE_SUDS*	H	H

Table 7: FE Bus Slot Determined Signals

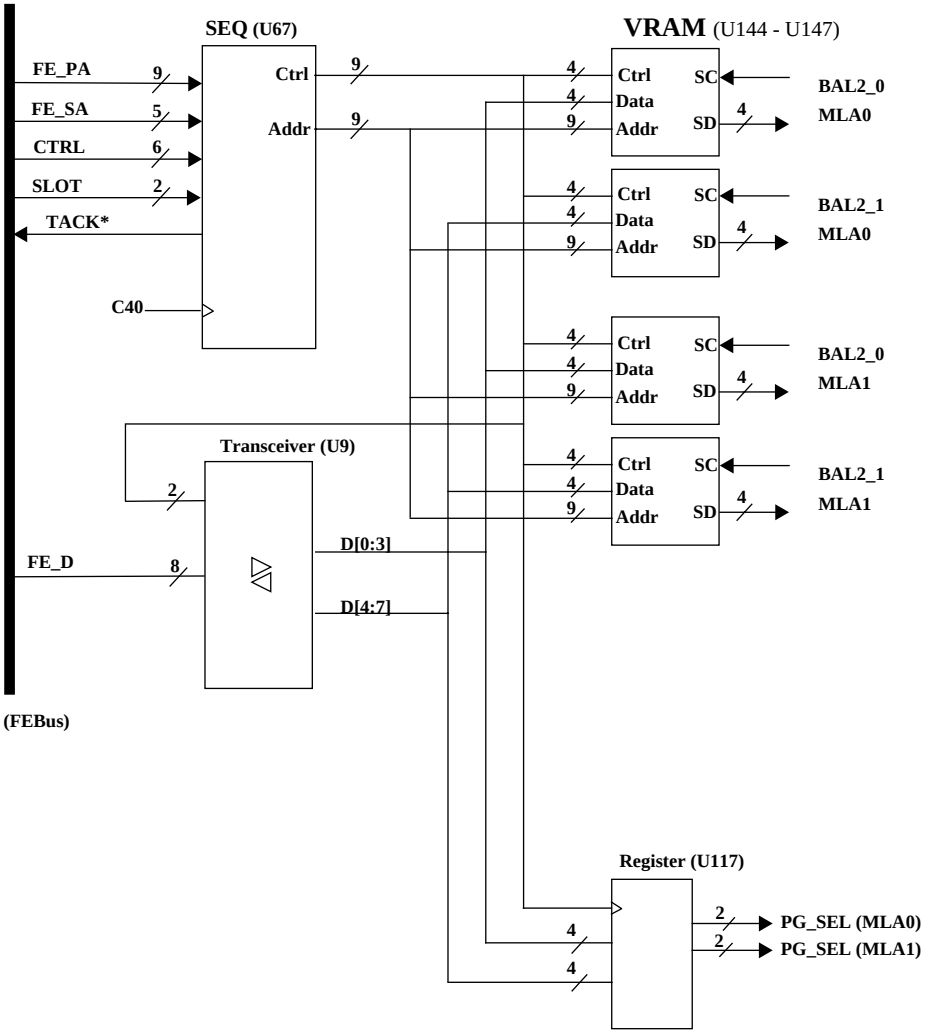


Fig. 29.3 Parameter Cache Interface signals

30 Outputs

The main outputs from the BF board are the MLA outputs from the beam adder 3.

Outputs from BF1 are input to BF2,output from BF2 are input to BF3,output from BF3 are input to BF4,output from BF4 are input to the RFT board.

Signal	Description	Destination	Level
ML0o-D[0:18]	MLA0 Data output	BF/RFT	TTL
ML1o-D[0:18]	MLA1 Data output	BF/RFT	TTL
ML2o-D[0:18]	MLA2 Data output	BF/RFT	TTL

Front End Controller - FEC

31 Overview

31.1 Abstract

This document is a description of the Front End Controller board (FEC) in System FiVe. The board controls the other board in the Front End. Most of the control is done through a synchronous and bidirectional bus called the Front End Bus. Among the different tasks performed by the FEC board are the following:

- System master clock generator
- Transmitter control
- ATGC control
- Receive focusing control
- Analog test signal generator
- High voltage control
- Probe sensing (PA/LA probes)
- Control of RLY board
- AA transmit and receive synchronization

FEC boards with artwork rev. F and onwards also contain:

- Probe sensing for AA and DP probes
- Temperature sensing for TEE probes

31.2 Document History

Rev.	Date	Sign.	Description
01	8. Aug. 1994	GRL	First version of document
02	24. Apr. 1997	GRL	Updated acc. with probe and temp. sense
03	21. Oct. 1999	LHS	Updated.
04	1. Oct. 2000	LHS/JB	Updated.Test Fatures moved to Ch.K

31.3 Definitions/Abbreviations/Nomenclature

Please refer to the *Abbreviations, Definitions, Glossary, Terminology, Nomenclature* list starting on *page P-1*.

31.4 References

- *Front End Controller Board Block Diagram – rev. 02, page B2-8.*
- *Board Revision History* starting on *page H4-1*

32 Inputs

Some of the signal inputs are listed below:

1. Probe Present, PRPRES[3:1]: 3 lines from the RLY board (low when probes installed).
2. AA XDCTRL signals: 5 lines at TTL level (LSACN_L, RSCAN_L, STAT_L, TLREQ_L and FLREQ_L) telling the status of the AA probe sweep status.
3. High Voltage V & I sense: Voltages and currents from the two HV supplies.

33 Description

33.1 System Clock Generator

The FEC module provides the source for the global system 40 MHz (C40) clock. The clock is available as a 4-quadrature signal, i.e. both 0, 90, 180 and 270 degree phases are generated. The 0 and 180 phases are named C40I[3:1]H and C40I[3:1]L, while the 90 and 270 phases are named C40Q[3:1]H and C40Q[3:1]L.

The clock is generated from a 160 MHz ECL signal level oscillator, and the counters and buffers used are all F100300 series ECL logic based circuits.

Of the three ([3:1]) copies of the clock, the first (1) is intended for the Front End only. This copy of the clock can be “slowed” to 1.25 MHz (40 Mhz further divided by 32) to conserve power when possible. Special care is taken so that when the clock switches, system integrity is preserved (i.e. no Front End reset is necessary after switching the clock back to “full speed”).

33.2 Front End Bus Interface

The front end bus consists of a 16 bit data bus, a 6-bit device address bus, a 10-bit page address bus and 8 strobe signals controlling the data transactions. The FEC board is the bus master, and the other boards in the Front End (+ RFT) are the slaves. The bus is among other things used to load focusing and steering delays into the transmitter (TX Board) and the Beam Former (BF1-4). During data reception, the bus is “quiet”, meaning there are no bus transactions during this period. Loading of new data is done between reception of one beam and the tx pulse for the next.

The FE Bus can be accessed directly through the VME interface, or from the FE sequencer and controller (DSP). In the first case, the FEC board functions just as a port between the CPU and the other FE boards. In the second and most used case, the FEC board controls the FE bus.

33.3 VME Bus Interface

The VME interface consists of bidirectional data buffers, unidirectional address buffers and a controller handing strobes, interrupts etc. Only the 16 least significant bits of the 32 bit VME data bus are used on the FEC board. The FEC board represents two VME Address spaces; one for the direct download of data from the CPU to the other FE boards (e.g. to the TX Board and BF caches), and the other for communicating control information (like loading of scan programs, error handling etc.) be-

tween the CPU and the FEC. The FEC board can issue interrupts to the CPU, and it will always respond to CPU accesses, provided it is not scanning (FE bus “quiet”).

33.4 ATGC Generator

An Analog Time Gain Compensation (ATGC) Counter (ATGCCT) and Prescaler [counter] (ATGPCT) is the FEC hardware sequencer responsible for stepping through a table of ATGC values stored in the ATGC RAM during beam data acquisition. The values in the RAM are fed to a DAC followed by a buffer, a low pass filter and single-ended to differential “conversion”, giving two signals, ATGCVP and ATGVVN with a range of +/- 10V.

33.5 Test Signal Generator

An analog test signal, TSIG, is generated by a DAC followed by a low pass filter.

33.6 XDCTRL Interface

A Timer Event Controller (TIMCTL) chip is used to poll the scanner control signals from the XDCTRL board section of the PRC board, and make them available to the DSP. TIMCTL also controls the signals returned to the XDCTRL board.

33.7 PA/LA Probe Select

In order for the system to know if probes are connected, the FEC board reads a probe present line from each of the 3 PA/LA probe connectors. This line will be grounded when a probe is installed.

In order to select one of the three probe connectors, 3 lines (PRSEL1-3) are fed to the relays on the RLY board, thus routing the tx/rx signals between the system FE and the selected probe.

33.8 PA/LA Probe Identification

All PA/LA probes contains a EEPROM where information about the probe is stored. After a probe has been selected, the contents of the EEPROM is read over one of the serial lines, PCF-SDA1-3, going to each of 3 connectors. The information is used to set up the front end correctly, and it can also be used to correct for unlinearities/ inaccuracies in the probe.

33.9 LA Probe Multiplexer Select

The Probe Multiplexer (PMX) Special Adapter (SPA) chip is an independent customized parallel to serial converter used to set the probe multiplexer switches. The PMX adapter will load 128 bits (PMX_SDA[127:0]) serially to the probe multiplexer using a shift clock, eight data lines and a load strobe.

The FEC uses a TPC1225 FPGA to implement this function.

33.10 Revision Detect

Each of the board in the FE contains a serial EEPROM, containing information like part number, serial number and revision. The contents of each EEPROM is read by the FEC board, and can then be transferred to the CPU so that the FE can be correctly programmed.

33.11 AA and DP Probe Sense (from artwork F only)

The Annular Array probes and Stand Alone Doppler probes are recognized in the same way as they are in the CFM-7XX and CFM-8XX products. A 2.5V voltage reference will always be in parallel with one of the resistors selected by a multiplexer (by PS_CUR[0:1]). Thus, depending on the size of the resistor, one of four constant currents can be fed through the probe code resistor. The currents are ranging from 3.3uA to 1mA in order to cover the range of probe code resistors from 0 to 3.3 Mohm. Three different probe resistors can be selected through a multiplexer (by PS_PRB[0:1]). In addition, a fourth onboard resistor can be selected for automatic test purposes.

A voltage will develop across the probe code resistor. This voltage is buffered, low pass filtered (150Hz) and scaled (A=0.4), before fed (as AAPRBCD) to a multiplexing A/D converter. The digitized values (D[0:7]) are then fed to the CPU board.

33.12 Temperature Sensors (from artwork F only)

33.12.1Annular Array TEE Probes

A temperature sensor is implemented for monitoring the temperature in the TEE probes. A reference voltage, 10.00V, is scaled down and fed to the temperature transducer (AD590), inside the TEE probe tip. This device outputs a current proportional to the temperature (1uA/Kelvin) or

$$I(T) = 273.2 + T, \quad [I\{uA\}, T\{^oC\}] \tag{33.1}$$

A voltage proportional to the current, develops on the inverting input of the instrumentation amplifier, AD620. A reference voltage corresponding to ~15°C, is connected to the non-inverting input. The voltage difference is then amplified, low pass filtered and fed to the A/D converter for digitizing.

The temperature will be displayed on the monitor. The system monitors the temperature and when exceeding a certain limit, (typ. 41.1 ^{o}C) necessary actions will be taken in SW to prevent further scanning.

A motor current shutoff mechanism is implemented: The amplified and low pass filtered voltage (AA_TEMP) is fed to two comparators (U10), so that when exceeding certain thresholds (below15 ^{o}C on the low end and above 41.3 ^{o}C on the high end), a TEMPOK signal goes low. This signal is fed to the PRC board and is used to switch off the motor signals to the mech. MPTE probe

As a self test of the circuitry, 3 test resistors can be selected by TMP_SEL[0:2] to simulate three different known temperatures.

33.12.2Phased Array TEE Probes

A similar circuit as described above, is also provided for the Phased Array TEE probes. A PA_TEMPIN voltage is proportional to the temperature at a thermistor located inside the probe tip. This voltage is compared to a “0-volt output level” set at ~15°C. Since the thermistor is nonlinear, correction for this is done in a formulae in software.

33.13 High Voltage Control

33.13.1HV Programming

The High Voltage Supply (HVS) Special Adapter (SPA) chip is an independent customized parallel to serial converter used to set the output voltage for the two outputs of the HV Supply. The HVS adapter will load 16 bits (HVS_SDA[15:0]) over a serial line to the HV supply using a shift clock, a data line and 4 select bits (HVS_SEN[2:1], HVS_LD[2:1]) addressing either HV Supply 1 or 2 for an update.

The FEC uses a TPC1225 FPGA to implement this function.

33.13.2HV Readback

The FEC employs a Maxim MAX158 (or Analog Devices AD7828) eight-channel ADC to convert eight separate analog signals from the HV Supply module to an 8-bit unsigned representation of the input voltage. The eight analog signals represents the output voltage and current drain for both the positive and negative side of the two separate high-voltage outputs from the HV Supply module. The output power is calculated, and if exceeding a certain limit, FEC will disable the HV Supply by enabling a HVDIS_L signal.

34 Control

34.1 VME Interface

The FEC board is controlled by the CPU board over the VME bus. The CPU communicates with a DSP on the FEC board.

34.2 DSP

The FEC board contains a TMS320C31-40 digital signal processor which is used for control purposes. When clocked at 40 MHz, this device executes instructions using a 5 stage pipeline with a cycle time of 50 ns (corresponding to 20 MIPS).

The TMS320C31 generates two complementary-phase 20 MHz clocks labelled H1 and H3.

The TMS320C31 has an external bus interface with a 24 bit address bus, a 32 bit data bus and the STRB_L and R/W_L control signals. External read transactions take minimum one H1 cycle, writes take two cycles. Both reads and writes may be extended with an integral number of H1 cycles by keeping the RDY_L input to the TMS320C31 high.

1. Serial/XF Interface Buffers.
2. Reset Generator (DRSTG).
3. Primary Address Decoder (DADEC1).
4. Debug Piggyback Address Decoder (DADECX).
5. Secondary Address Decoder (DADEC2).
6. DSP Wait State Generator (DWSTG).
7. DSP Read/Write Enable Generator (DRWED).

8. DSP Sbus to Tbus Address register/Buffer.
9. DSP Sbus to Tbus Data register/Buffer.
10. Local External RAM (XRAM).

    Local memory are 8 128Kx8 MT5C1009-20 SRAM devices, divided into two 128Kx32 banks. The access to the local memory is completely controlled by the address and the STRB_L and R/W_L strobes, and requires no extension cycles (wait states) on read nor write.
11. Local Boot EPROM
12. DSP Interrupt Controller

35 Outputs

Some of the output signals are listed below:

1. Transmit trigger, TXTRIG_L: Signal starting the transmitter sequence in the TPGs on TX128 and PRC.
2. Receive synchronization, SYNC_L: Signal used to synchronize the beam-former.
3. Test signal, TSIG: Analog test signal used by the RX Board and PRC.
4. Analog Time Gain Compensation voltage, ATGCVP and ATGCVN: Differential signals used to control the VCAs on the RX Board and PRC.
5. High Voltage Control: One serial data line and several select lines to the HV Supply.

Patient I/O

36 Overview

36.1 Abstract

This document is a description of the Patient I/O board (PAT I/O) in SYSTEM FIVE. This module records and process the analogue traces in SYSTEM FIVE. The signal conditioning circuitry (instrumentation amplifiers and analogue filters) are located on separate daughter boards that are plugged into a main board containing the A/D converters and the isolation barrier. The DSP performing the final signal processing is located on the Internal I/O board, and is therefore not described in this document.

36.2 Document History

Rev.	Date	Sign.	Description
01	9 Aug. 94	GRL	First version of document
02	01.11.00	JB	Maintenance Aids moved to Chapter K

36.3 Definitions/Abbreviations/Nomenclature

DSP: Digital Signal Processor

ECG: Electro CardioGram

QRS, QRS complex: Characteristic part of the ECG signal

SDP: Spectrum Doppler Processor Board

36.4 References

Patient I/O Block Diagram – rev. 02, page B2-9

37 Mechanical Assembly

Refer to *Fig. 37.1* for an assembly drawing of the patient I/O modules. The daughter board is attached to the main board through two dual row 100 mil pitch connectors.

37.1 Main Board

The patient I/O main board is a modified single Europe circuit board with overall dimensions of 160.0 x 104.8 mm.

37.2 Daughter Boards

The patient I/O daughter boards have overall dimensions of 95.0 x 70.0 mm (type I) or 95.0 x 150.0 (TBD) mm (type II). Type I boards support up to four analogue channels, while type II boards support up to eight analogue channels.

For the time being, only one board has been implemented, a type I ECG & Phono module with four channels (ECG, phono, respiration and pressure).

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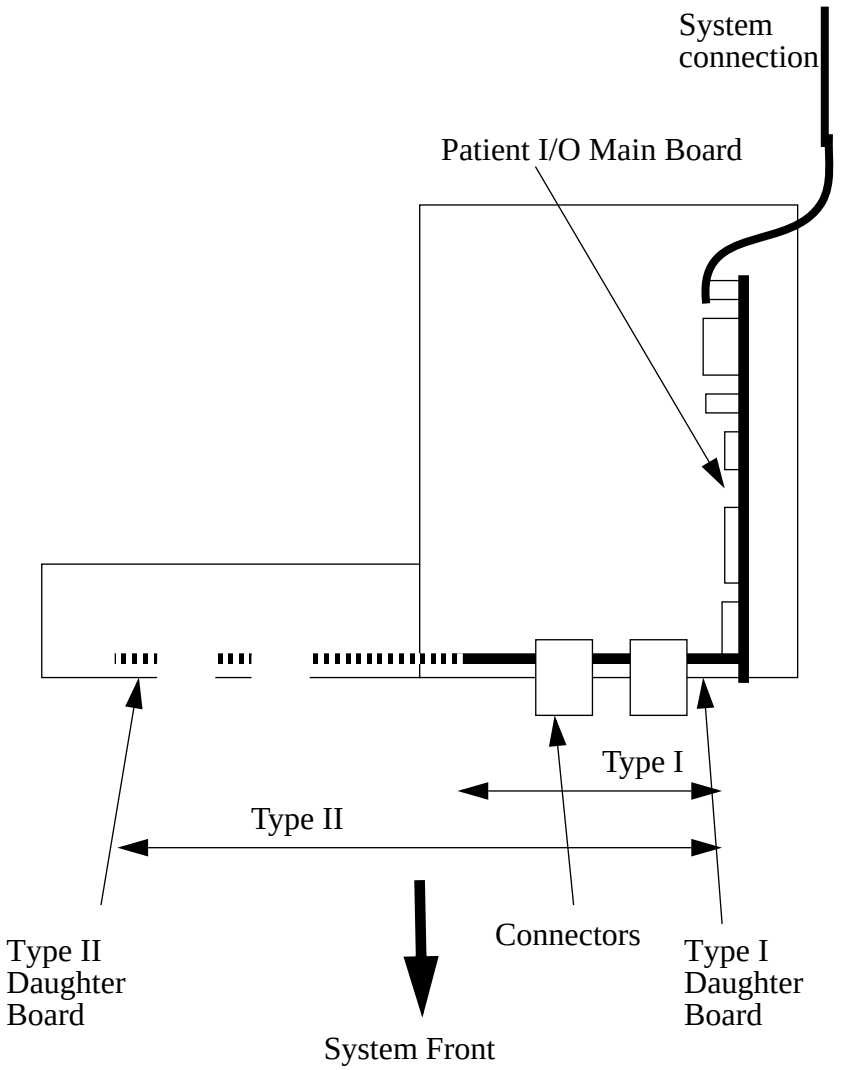


Fig. 37.1 Mechanical Assembly

38 Inputs

1. ECG input: For connection of 3-lead ECG electrode cable.
2. Phono input: For connection of heart microphone.

3. Respiration input: For connection of respiration transducer.
4. Pressure input: For connection of pressure transducer.

39 Descriptions

39.1 Overview

Fig. 39.1 illustrates the different operations that are performed in hardware and software.

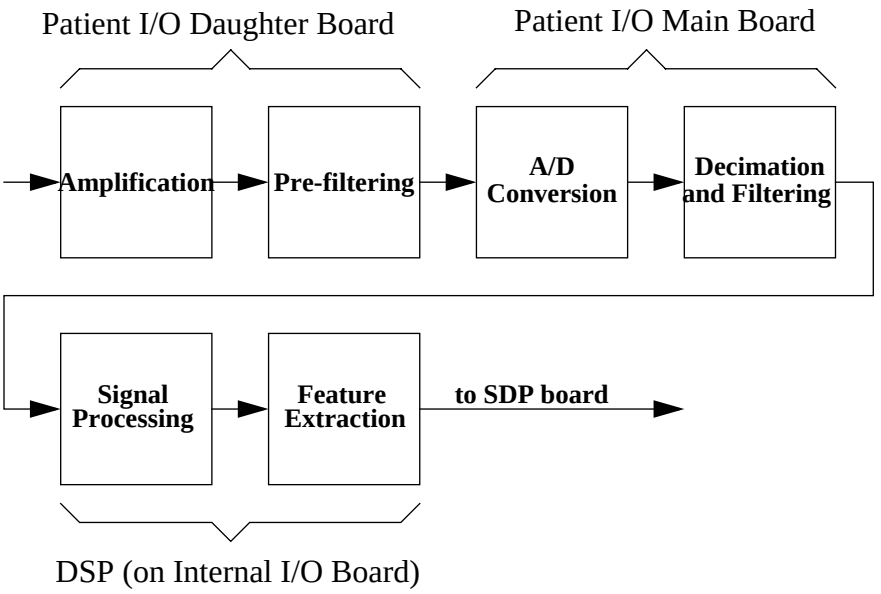


Fig. 39.1 Signal Flow Diagram

The daughter board connects to the patient I/O sensors (ECG, phono, pressure, respiration etc.) and provides sensor dependent amplification and first order pre-filtering.

The main board performs the analogue-to-digital conversion of the sensor signals in a high resolution sigma-delta convertor. This A/D converter also contains a decimating IIR filter that provides most of the bandwidth limiting and provides a low rate serial data stream to the DSP's serial input port.

The DSP first performs simple signal processing, such as decimation, low-pass/ high-pass filtering and power line filtering. The last block in the figure includes extraction of features such as QRS complexes, respiration direction, heart sounds etc. In addition it detects whether there are physiological signals present at all (e.g. sensors connected).

Processed signals and detected features are then transmitted serially to the SDP board on request.

39.2 Main Board

Refer to *Fig. 39.2* for a block diagram of the patient I/O main board. For the circuit diagram, refer to functional diagram 330 FA201193.

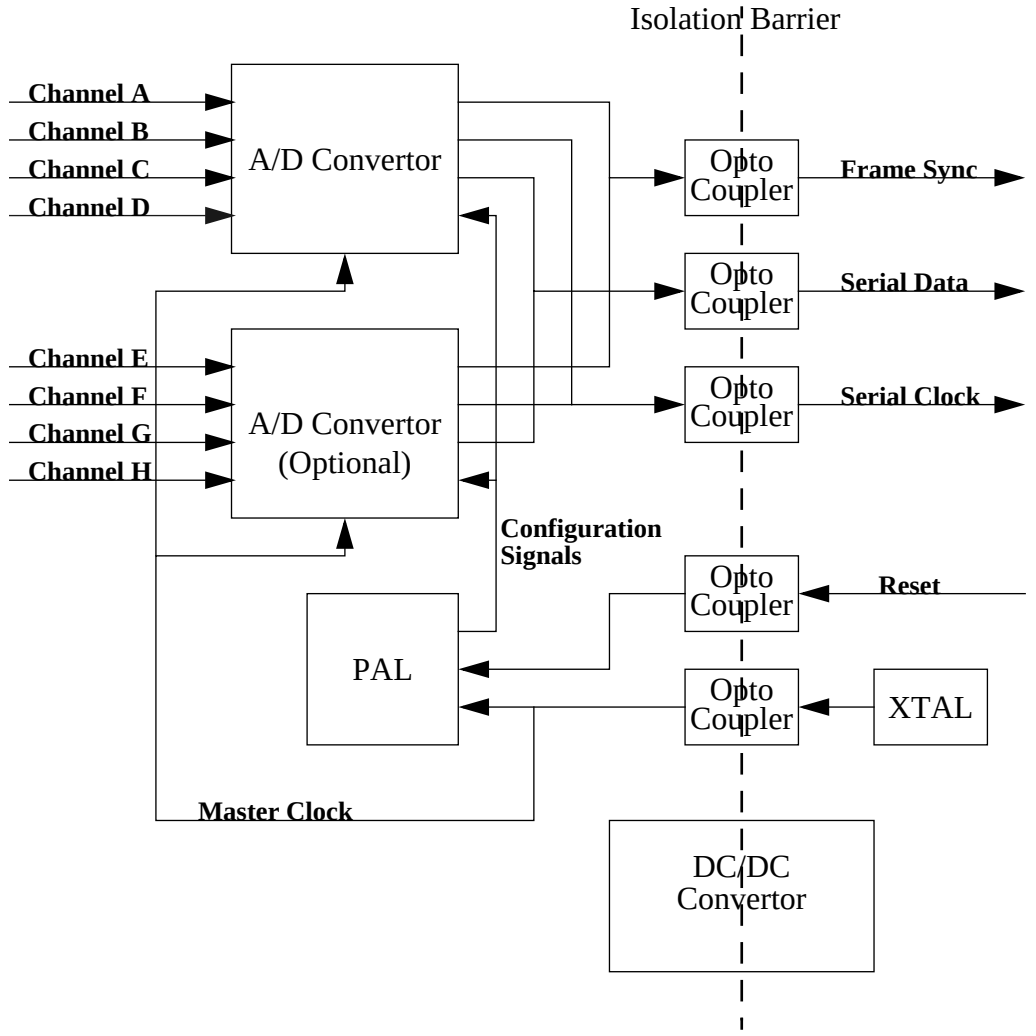


Fig. 39.2 Block Diagram Patient I/O Main Board

The sensor signals from the daughter board are input to two Analog Devices AD7716 A/D converters (U1 and U2) though a set of RC antialiasing filters (R1 to R8 and C1 to C8). The AD7716 is a complete four channel 22 bit sigma-delta data acquisition system with built-in digital decimation filter. The A/D converters use external reference U3, and are controlled by a 7.5264 MHz master clock generated in crystal oscillator X2. This master clock is divided by 14 internally to yield an input sample rate of 537.6 kHz. The built-in IIR filter reduces this sample rate by a factor of 256, yielding an output update rate of 2100 Hz per channel. The output data are transferred to the DSP through a three wire serial interface, consisting of serial data, serial clock and a frame sync signal. The A/D converters are configured during system reset by serial transfer of configuration data from a PAL (PALCE 22V10, U5). Counter U4 divides the master clock by eight to provide a suitable transfer rate for the configuration data.

Opto couplers PC1 to PC5 provide galvanic isolation of the digital signals running between the isolated (patient) and the non-isolated (system) side of the patient I/O main board. The isolated side is powered through isolation DC/DC convertor U8, a

PWR1303 from Burr-Brown. Extensive decoupling is used on both sides of the DC/DC convertor to reduce conducted switching noise to a minimum.

One half of tri-state line-driver U6 buffers the digital control and data signals to and from the main board, while the other half is used as a four bit board configuration register, with solder pads SP1 to SP4 determining its contents. For the current version of the patient I/O main board, the configuration register is set to 1111.

The contents of 8 bit configuration register U7 is determined by the type of daughter board that is attached to the main board. The following configurations are supported:

Address	Description
$00 - $7F	Reserved for type II daughter boards
$80 - $FD	Reserved for type I daughter boards
$FE	ECG & Phono Board (type I)
$FF	No daughter board present

39.3 ECG & Phono Board

Only one daughter board has so far been implemented, the ECG & Phono board. This is a four channel type I board which interfaces to Electro cardiogram, heart microphone, respiration and pressure sensors.

Refer to drawing 330 FA201193 for the circuit diagram of the ECG & Phono board.

The ECG signals enter the board through circular AMP connector P3. The signals from the left and right arm electrodes are buffered by dual JFET opamp U1, before they are amplified by instrumentation amplifier U2. Dual opamp U3 drives the left leg electrode and the ECG cable screen with signals derived from the common mode voltage at the instrumentation amplifier inputs. Input filter R3/C1 and R4/C2 reduces susceptibility to RF noise, while output filter R8/C3 limits the signal bandwidth to about 1600 Hz.

The phono signals enter the board through phono connector P4, and are amplified by instrumentation amplifier U4 with input filter R16/C5 and R17/C6. One half of dual opamp U5 is used as a shield driver in order to improve the AC common mode rejection. The signal bandwidth is limited to about 1600 Hz by output filter R20/C7.

The respiration sensor, an NTC resistor (thermistor), connects to the board through phono connector P5, and is the variable element in a standard wheatstone bridge, with fixed elements R22 to R24, and reference U6. Dual opamp U7 is used to linearize and buffer the bridge signals, while filter R27/C10 is used to limit the output bandwidth to about 160 Hz.

The pressure signals enter the board through phono connector P6 and are buffered by dual JFET opamp U8, before they are amplified by instrumentation amplifier U9. One half of dual opamp U5 is used as a shield driver in order to improve the AC common mode rejection. Input filter R34/C11 and R35/C12 reduces susceptibility to RF noise, while output filter R39/C13 limits the signal bandwidth to about 160 Hz.

40 Control

The Patient I/O board is controlled by the DSP on the Internal I/O board through an 8 bit parallel data bus (DSP_DATA[0:7]) on connector P3.

41 Outputs

1. Serial data from A/D converter (DR, P3-4) to DSP on Internal I/O board.
2. Serial clock from A/D converter (CLKR, P3-2) to DSP on Internal I/O board.
3. Serial frame sync from A/D converter (FSR, P3-6) to DSP on Internal I/O board.

Transducer Bus Board - XDBUS – rev. 04

42 Introduction

42.1 Abstract

This document is a description of the Transducer (Xducer) Bus Board (XDBUS) in SYSTEM FIVE. The board routes the 128 tx/rx signals between the RLY board and the Transmitter and receiver.

42.2 Document History

Rev	Date	Sign	Description
01	10 Nov. 1994	GRL	First version of document
02	20 Sep. 1995	LHS	Updated layout, corrected minor errors
03	27 Aug. 1999	LHS	Included references. Moved Definitions/Abbreviations/ Nomenclature to the Glossary (Section P)
04	21 Oct. 1999	LHS	Updated text in illustration.

42.3 Definitions/Abbreviations/Nomenclature

Please refer to the *Abbreviations, Definitions, Glossary, Terminology, Nomenclature* list starting on *page P-1*.

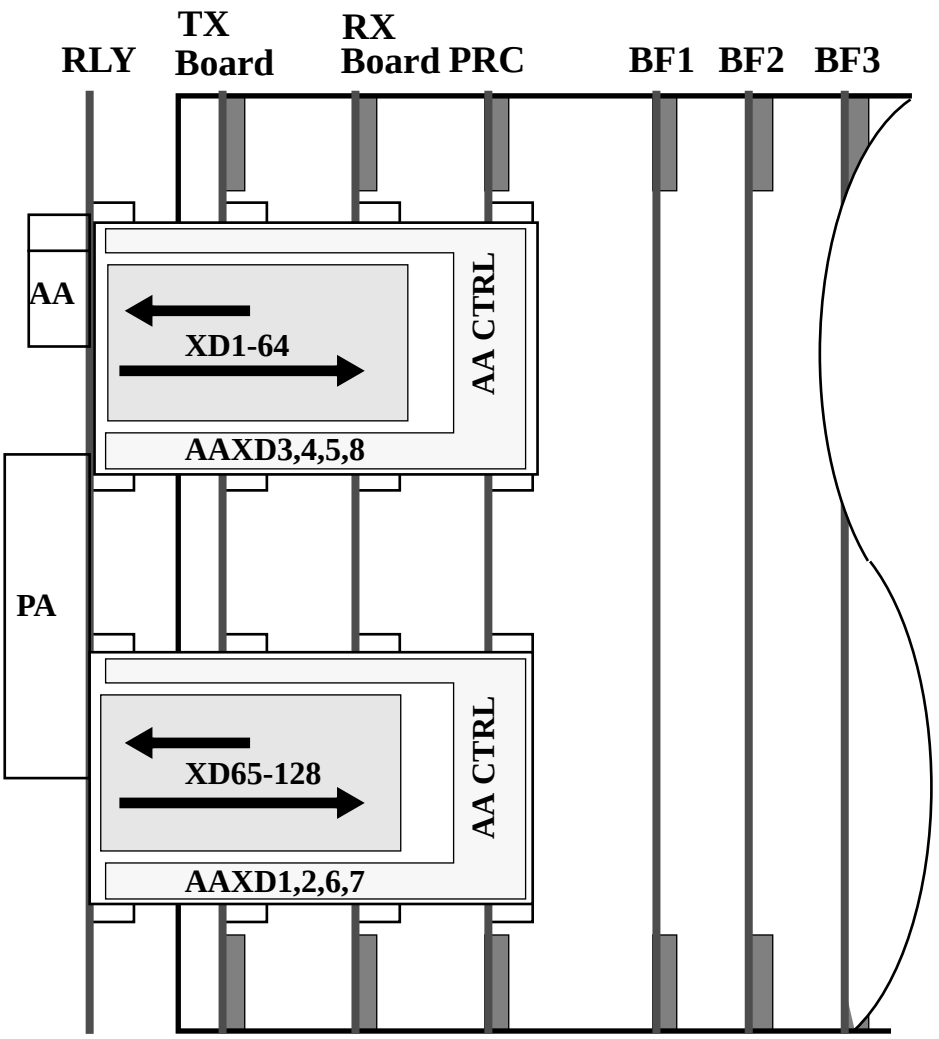
42.4 References

- *Front End and Mid., rev. 10* Block Diagram on *page B1-3*
- *Front End – rev. 04* Block Diagram on *page B1-5*
- *Board Revision History* starting on *page H4-1*

43 Description

The XDBUS boards are two identical and interchangeable boards mounted on the

front of RLY, TX Board, RX Board and PRC.



- The rx/tx signals for the PA- and LA probes are routed between RLY, RX Board and TX Board.
- Eight rx/tx signals for the AA- and DP probes are routed between RLY, RX Board and PRC.
- Several AA control signals (for e.g. motor, position, probe sense and temperature sense control) are routed between RLY and PRC.

The Mid Processor Modules

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the Mid Processor modules.

Modules and sub-systems described in this part of the manual

These modules and subsystems are described in this part of the manual:

Module / subsystem	Page
RF- and Tissue Processor board – rev. 04	A3-3
Spectrum Doppler Processor – rev. 03	A3-9
2D Flow Board - rev.01	A3-12

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A3_01_Mid_Proc.lnnh.02.
Printed: December 5, 2000.

Your notes:

RF- and Tissue Processor board

1 Overview

1.1 Abstract

This document describes the RF and Tissue Processor board (RFT). Several versions have been used, containing support for up to three (3) parallel RF-processing units, an IQ-buffer, a Tissue-processing unit (detection, compression, composite beam handling, peak detection and digital filter) and a Doppler High Pass filter unit (digital filter). The board is located between the Beam Former and the PipeLink. On earlier versions of the board, two of the RF-processing units (RFP) were made as separate add-on modules (daughter modules), to allow only the number of units needed (equal to the number of MLAs), to be installed. On newer boards, called RFT1, one or two MLAs are included on the board (no daughter module needed).

The RTF1 boards are produced in two versions, RFT and RFT-NOMLA. The NOMLA version is a depopulated board with only one RF-processing unit, reduced IQ-buffer memory, and the spectrum doppler filter replaced by a sw filter performed by the DSP.

The RFT1 board receives its input data from the Beam Former board. In case of MLA, Multi Line Acquisition, the input may be from up to two (2) parallel data streams. After the signal processing of the data has been done, the RFT board sends its output data out on the PipeLink.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A3_02_03.fm.
Printed: December 5, 2000.

1.2 Document History

Rev.	Date	By.	Description
01	5 Aug. 94	GRL	First version of document
02	27 Mar. 95	LHS	Added block diagram, updated.
03	29 Mar. 99	MLH/LHS	Included description for the RFT1 boards (including the RTF NOMLA board)
04	01Nov.00	JB	Moved Test features to Ch.K. Edited Fonts.

1.3 Definitions/Abbreviations/Nomenclature

Please refer to the Abbreviations, Definitions, Glossary, Terminology, Nomenclature list starting on page P-1.

1.4 References

Block Diagrams: *and the* RF & Tissue Proc. Block Diagram – rev. 02 on page H1-10.

Board history:RFT, FA200373 on page H1-8

Board formats:A1-72

System description:A1-49

Trouble shooting guide:*K1-1*

1.5 Mechanical specifications

- The RFT board consists of a baseboard with one RF processing module. Optional, can one (or two) RFP daughter module(s) be added to fit the need for RF-processors. The number of RF-processors is the same as the number of MLA sections.
- Even if the RFT board was originally designed to support up to three MLAs, that have never been utilized in System FiVe.
- The RFT1 board holds one or two RF processing modules as an integrated part of the board. The RFP daughter modules will not be used on this board.

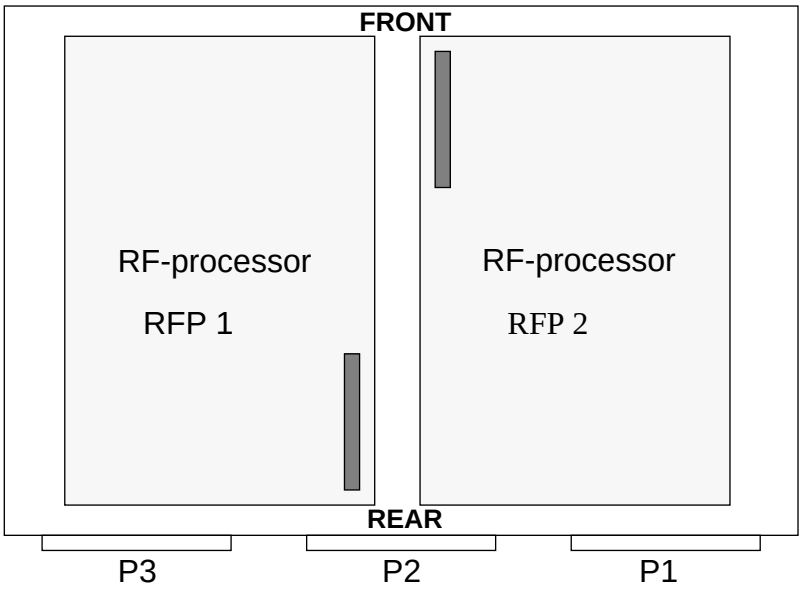


Fig. 1.1 RFT board with two RF-processors

Fig. 1.1 shows a RFT board with the maximum number of RF-processor modules.

In Fig. 1.2, a drawing of the RF-processor stacking is shown, viewed from the side.

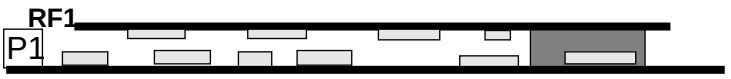


Fig. 1.2 Side view of the RFT with RF-processors

2 Inputs

The RFT board/RFT1 board have the following major inputs:

1. Beam Former Interface

Real time data input port.

1, 2 or 3 parallel data streams can occur simultaneously in case of MLA, or two data streams containing range intermixed data can occur simultaneously in case of full band mode. The MLA streams are named MLA0, MLA1 and MLA2.

The input data to MLA1 or MLA2 can be selected to occur at an alternative set of input pins, in case of a 128 element probe used as two 64 element probes in parallel with one Beam Former.

2. FEbus interface

Real time information input port.

Prior to data received from an Xmit, a set of information is transferred from the FEC to the RFT specifying how to handle the input data stream, and how to control the output data stream.

3 Descriptions

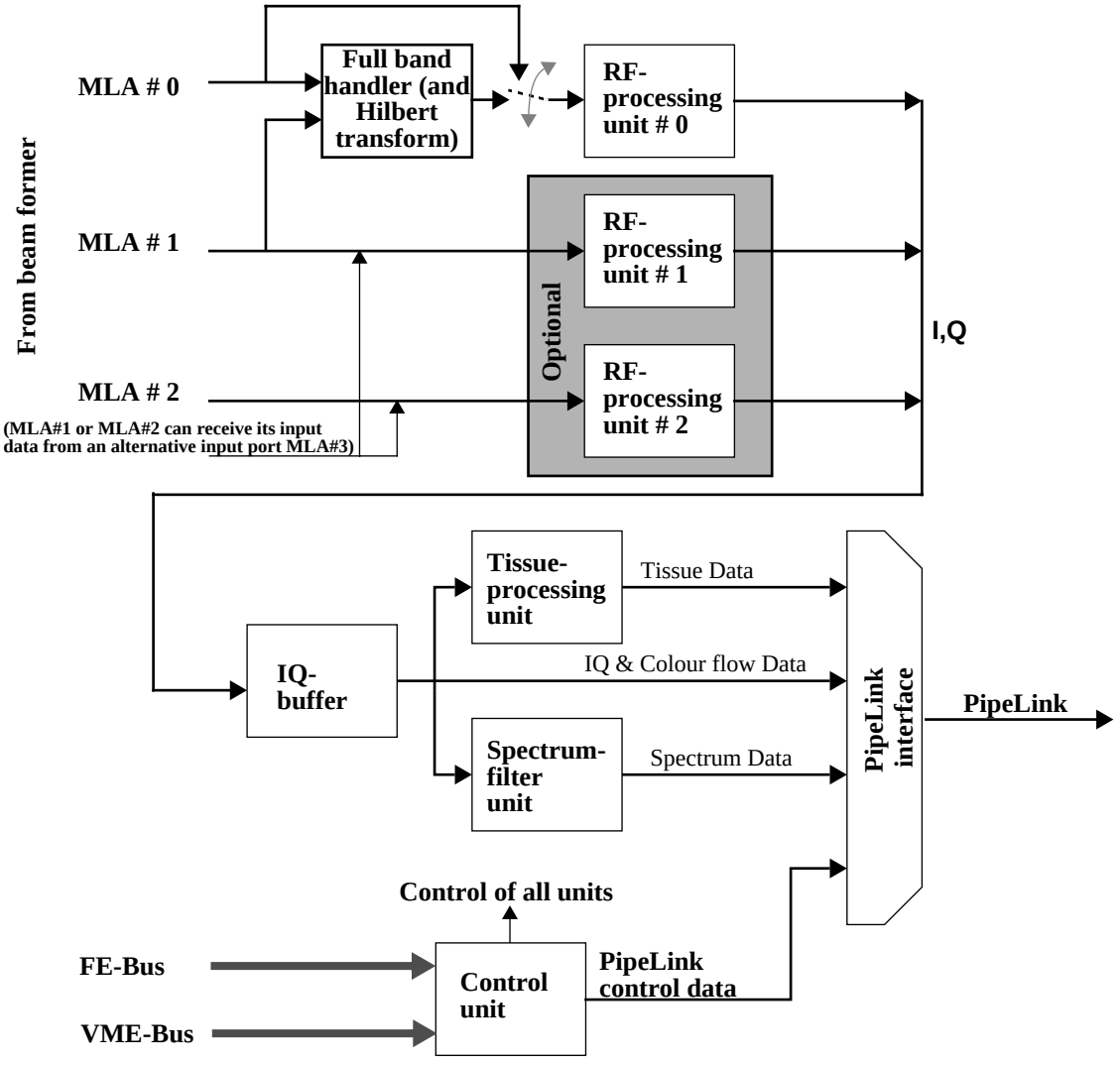


Fig. 3.1 RFT block diagram

Below are the different blocks of the block diagram described in some detail.

3.1 Full band handler (and Hilbert transform)

The data transfer from the Beam Former is made synchronously. To make this interface robust, a set of input registers are used. For test purposes, the DSP can start a test pattern generator that generates a known test input pattern instead of using data from the input registers. The test data will be

processed by the input processing part of the RFT as if it had been normal data received from the Beam Former.

One MLA section will produce data with a rate of 20 MHz. If a data rate of 40 MHz is needed (used for high frequency probes), MLA0 and MLA1 will be used to each produce every other data respectively. Conceptually the full band handler will merge the data stream from MLA#0 and MLA#1 to one data stream with a data rate of 40 MHz.

A data rate of 20 MHz is called *half band* mode, while a data rate of 40 MHz is called *full band* mode.

(GEVU have not yet started to utilize the Hilbert transform nor the fullband mode. All RFT boards produced have this feature de-populated, RFT1 boards have it removed. The Hilbert transform converts the two-sided spectrum of its real input signal to a positive-sided, complex signal on the output. The Hilbert transform will decimate the data stream by two nearly without loss of information. Input data rate to the RF-processing units will therefore be 20 MHz in all modes. The Hilbert transform is only used in full band mode.)

3.2 RF-processing unit (RFP)

An RF-processing unit consist of a complex multiplier and two real FIR filters. The following signal processing tasks will be made on the data stream while the data flows through the RF-processing unit:

- TGC
- Complex demodulation
- Filtering
- Decimation

3.3 IQ-buffer

The IQ-buffer is used for transforming the input data flow sequence and rate to an output data flow sequence and rate that is more suited for the signal processing of the data to follow. The IQ-buffer will also have some timing elastic regarding the input data rate vs. output data rate.

Typical transformations are

- Data from N_1 tissue Xmits with different TX focused in the same direction
  -> one (composite) tissue beam (N_1>1)
- Data from N_2 flow or spectrum Xmits in the same direction
  -> N_3 data set each with N_2 data from the same range.
  (N_3 is the number of range samples)
- Data from one Xmit
  -> two or more data set contains the same data but with different use.

The IQ-buffer can handle a simultaneous input and output data rate of 20 MHz complex data.

3.4 Tissue Processing Unit

The Tissue Processing Unit contains signal processing hardware for:

- Detection $\sqrt{I^2 + Q^2}$
- Compression
- Composite beam handling - Zone stitching - Line compounding
- Peak detection and Edge Enhancement
- Tissue filtering

3.5 Doppler High Pass Filter

The Doppler filter unit contains a digital filter where the cutoff frequency can be changed according to the Low Velocity setting on the front panel. The filter reduces the dynamic range of the signal down to 16 bit.

Color flow data will be sent directly out from the IQ-buffer, since all filtering needed will be done one the 2DF board.

3.6 Local processor

For the control of the RFT and for some signal processing tasks in SDCW a DSP of type TMS320C31-40 is used.

The local DSP have its EPROM based start up program, containing the following functions:

1. Local power up self test.
2. Routines for receiving a downloaded application program from disk.
3. A local test monitor used for production board level test and board level failure localization.

As soon as the application program is downloaded and the rest of the instrument is operating, the DSP will handle the following tasks:

1. Communication with the cpu.

   Most changes of the instrument control will result in a message sent from the CPU to the RFT, specifying how the RFT shall be used. The local DSP program must react according to these specifications. There is only communication from the CPU to the RFT when the operator changes a setting on the instrument, except for during certain test modes.

2. Xmit to Xmit control.

   The FEC controls most of the data flow until data have been written into the IQ-buffer. There might be cases where the DSP needs to update some filter coefficients before data from a new Xmit occurs. In that case a message is sent from the FEC to the RFT via the FEbus. The RFT receives message one Xmit before a new coefficient set is needed, and the hardware is designed so the DSP without any synchronization can update the coefficient set as soon as the message is received.

3. The output event tags generated by the FEC are used for starting pre-calculated downloaded PipeLink data transfers. As soon as an output event occur the DSP can set up the output control hardware for transferring a data set out on the PipeLink.
4. Based on the timer interrupt with a rate TS [2.0ms or 4.0ms], the DSP must set up a time slot data transfer. In some instrument scan modes the timer interrupt is replaced with a output event message with a fix interval [4.0, 8.0 or 16.0 ms]
5. In SDCW mode the DSP shall perform a matched filter calculation on the data stream. The filter consists of adding a number of samples together and the result is passed through a filter

The DSP is mainly involved with two processes a) react on output events received from the FEC, and b) react on the timer interrupts at a rate of TS [2.0ms or 4.0ms] and set up for a time slot transfer. These two are asynchronous in time.

4 Control unit

The RFT board contains hardware for control of different sections of the board. The following is important:

- input control (ICTRL), controls the data flow until the data has been written into the IQ-buffer.
- output control (OCTRL), controls the data flow out from the buffer and out on the PipeLink.
- the local DSP is used for all control tasks not directly implemented in hardware. The hardware implemented control functions are set up / controlled by the local DSP.
- The VME interface is used for CPU to RFT communication. The VME interface may also be used for replay of IQ-data. The interface is quite slow.

5 Connectors

5.1 The RFT board

VME-bus:	P1
Clock distribution	P2
PipeLink:	P3
Front End bus:	P2
MLA section 0:	P2
MLA section 1:	P2
MLA section 2:	P2
RF-processor 1:	J1
RF-processor 2:	J2
TMS320C31 emulator	P4
RS232 serial line	P5

P1, P2, P3 are at the rear side of the board.
P4, P5 are at the front of the board.
J1, J2 are at the component side of the board.
Pn is a male connector, Jn is a female connector.

5.2 The RFT1 board

VME-bus:	P1
Clock distribution	P2
PipeLink:	P3
Front End bus:	P2
MLA section 0:	P2
MLA section 1:	P2
TMS320C31 emulator	P4
RS232 serial line	P5

P1, P2, P3 are at the rear side of the board.
P4, P5 are at the front of the board.
Pn is a male connector.

6 Outputs

6.1 PipeLink interface

The PipeLink interface is an output port only. Data and control signals are sent out on the PipeLink to SDP, 2DF or Image Port.

Spectrum Doppler Processor – rev. 03

7 Overview

7.1 Abstract

1. This document describes the Spectrum Doppler Processor board (SDP). The SDP board performs spectrum analysis, performs missing signal estimation and generates the analog Doppler signals used for audio. It also generates the velocity traces as well as taking serial trace data from the Internal I/O board onto the pipelink bus. The board receives high pass filtered data from the RFT board and outputs processed data to the Image Port. System control is done by System Processor via the VME interface.

7.2 Document History

Rev.	Date	Sign.	Description
01	5 Aug 1994	GRL	First version of document
02	3 Jan 1995	HN/LHS	Updated information and layout.
03	12. Aug 1999	LHS	Corrected some typos.
04	01Nov.00	JB	Moved Test Features to Ch.K

7.3 Definitions/Abbreviations/Nomenclature

RFT: RF and Tissue Processor board

DSP: Digital Signal Processor

PW: Pulsed Wave Doppler

CW: Continuous Wave (Doppler)

I: In phase

Q: Quadrature phase

DFT: Discrete Fourier Transform

MSE: Missing Signal Estimation

7.4 References

Block Diagram: See page B2-11.

8 Inputs

The SDP board have the following major inputs:

1. Pipelink Interface

   Data from the RFT board is received on the pipelink bus. The signals are located on the P3 connector.

2. Serial Trace Data

   Analog traces (e.g. ECG) are received serially on a line from the Internal I/O board.

9 Descriptions

Below are the different blocks of the block diagram described in some detail.

1. Data Buffer

The Data Buffer is a buffer for the *I* and *Q* Doppler data to be analyzed. It also has the option to store M-Mode data for signal processing by the Master DSP. The read process of the Data Buffer is controlled by the Master DSP.

In order to perform the modified DFT on the PW mode Doppler signal, the data acquisition must be done as a function of both time and space. In CW mode the data acquisition is done as a function of time only. That is, only data from one range is used for the DFT estimation. The appropriate addressing for Doppler data acquisition is done in Data Read/Write Address Generators.

9.1 Spectrum Analyzer

Spectrum analysis is performed in the below mentioned blocks (details not shown on the block diagram).

9.1.1 Spectrum Window Function and Addressing

Before DFT the Doppler data is weighted by a smoothing window function. This is done by multiplying selected samples from the Data Buffer with selected coefficients stored in a Window RAM. The selection of appropriate coefficients is done in a Window Address Generator block

9.1.2 Complex Exponential Multiplier and Accumulator

Once the Doppler data has been weighted by the window function, the modified DFT operation is implemented. It performs the complex multiplication between the complex Doppler data and the complex exponential function and accumulates the result. The resulting complex frequency component is fed to Master DSP for further signal processing.

9.1.3 Digital Signal Processor 1

The Master DSP block computes the magnitude squared, performs the spatial and temporal averaging, calculates the magnitude of the averaged spectrum, and estimates the velocity traces.The Master DSP administer the overall data flow to and from the PipeLink. It is interfaced as a slave module for data transfer via the VME-bus.

The Master DSP is connected to a Boot Strap Flash-PROM which is used for Master DSP initialization and test programs. It also contains a bootstrap initialization program for MSE DSP. This program is down loaded from Master DSP to MSE DSP via the serial port.

9.2 Audio and Missing Signal Estimation

9.2.1 MSE Digital Signal Processor

The main task for the MSE DSP is to perform the data acquisition for the audio analog-to-digital conversion as well as generate the MSE for the audio in Time Shared Mode (TSM). The data used to generate the analog Doppler signals is transferred from the Pipelink via the Audio FIFO's to the MSE DSP.

9.3 Digital-to-Analog Converter

The output of MSE DSP is a digital Doppler signal, or a combination of the real and a synthesized Doppler signal, which is converted to a complex analog signal by the Digital-to-Analog Converter (DAC) to analog *I* and *Q* components. The analog signals are low pass filtered in order to obtain a clean and crisp audio.

10 Control

10.1 VME Interface

The VME Interface provides for communication between the system CPU and the SDP. The Master DSP is a slave of the VME bus and responds to interrupts signalling the transfer of data from the CPU to the Master DSP Memory block. The VME Interface on the SDP is based on a general architecture used for several modules in the system.

10.2 Master DSP Control and Administration Tasks

The Master DSP administers the data flow and parameter update on the SDP. The following tasks are performed by Master DSP:

- Respond to VME Interface interrupt at initialization.
- Respond to VME Interface interrupt for updating of parameters and tables.
- Provide for Data and Window READ/WRITE Address Generation control and synchronization.
- Perform interpolation on spectral output data.
- Supply output FIFO with spectrum and trace data in the appropriate sequence.

11 Outputs

The SDP board has two major data outputs:

1. Pipelink Interface

   Spectrum data is transferred from the output FIFO onto the pipelink bus when one spectrum line is processed, and the board at the same time receives new data on the pipelink input.

2. Audio Output

   The analog Doppler signals AN_DOP_I and AN_DOP_Q are output on two pins on the P3 connector; A26 and A27. They are fed to the front panel and the VCR, via the Internal I/O board.

2D Flow Board

12 Overview

12.1 Abstract

This document describes the 2D Flow Processor board (2DF) performing Fixed Target Cancelling, Autocorrelation, averaging and Velocity Parameter Estimation.The board utilizes DSPs to accomplish the functions listed above. Data is received from the RFT board, processed and fed out on the pipelink bus to the Image Port board.

12.2 Document History

Rev.	Date	Sign.	Description
01	5 Aug. 94	GRL	First version of document
02	11Nov.00	JB	Moved Test Features to Ch.K

12.3 Definitions/Abbreviations/Nomenclature

RFT: RF and Tissue Processor board

DSP: Digital Signal Processor

FTC: Fixed Target Cancelling

IQ: In phase / Quadrature phase components of complex signal

LUT: Look-Up-Table

12.4 References

2D Flow Board Block Diagram – rev. 01 on page B2-12

Board formats on *page A1-73*.

2D Flow Board (this document)

System description on *page A1-51*

Theory of Operation on *page A1-24*

13 Inputs

The main data input to the 2DF board is the pipelink, a bus located on the P3 connector. Data is transferred range by range from the IQ buffer on the RFT board.

14 Descriptions

14.1 General Description

As can be seen from the block diagram, the design contains 16 FTC processors handling filtering and autocorrelation, 4 Velocity processors handling averaging and parameter estimation and 1 *Master processor* controlling the other 20. This gives a total of 21 processors. The purpose of having this many DSPs is to get the desired processing speed. The VME is used for communication between the Master DSP and the CPU. There is no ultrasound data transfer on the *VME bus*. A dedicated bus known as the *Pipelink* is used for data transfers.

14.2 Input Dispatcher

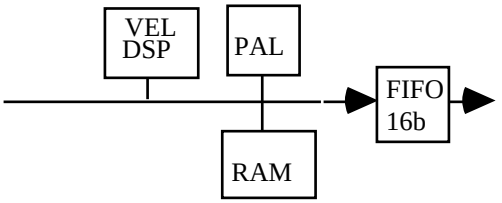
Data that arrives on the PipeLink have to be separated and given to the appropriate FTC processor. The FTC processors handles data from the different ranges. To do this a so-called Input Dispatcher implemented in an Actel FPGA .This device is placed between the PipeLink input and the FIFOs going to the FTCs. The Dispatcher checks if this mid-processor is the destination of the data. If so, the Input Dispatcher then gives write signals to the dedicated FIFOs.

14.3 FTC DSPs

16 of the DSPs are called FTC DSPs. These DSPs perform both fixed target cancelling and autocorrelation on the different ranges. The number of ranges to be processed can vary between 64 and 512. Two different autocorrelation algorithms will be supported; the conventional one used in the CFM products and an advanced one, which main advantage is unwrapping of frequency aliasing. When doing the advanced algorithm, two ranges must overlap into the neighboring FTC processors. Below is shown one of sixteen FTC processing modules.

14.4 VEL DSPs

Data from four FTC DSPs are fed to one VEL DSP. Here both radial averaging and velocity parameter estimation is performed. The 3 types of velocity parameters; intensity (or power) [4 bits], velocity [8 bits] and bandwidth [4 bits] are packet into one 16 bit word sent to the Master DSP. Below is shown one of the four VEL processing modules.



14.5 Master DSP

The Master DSP controls all the processing:

1. **Booting**

   The 2DF programs and Look-Up tables are stored at the CPU. During system start-up these are loaded to the Master DSP. The Master DSP has a demultiplexer at the output of the serial link. With this demultiplexer the Master DSP can decide which FTC or VEL module to write to. It is possible to write to a single module, or to all modules at the same time. Some special combinations of modules can also be written to. This way we can have different programs in the different processors in the different modules.

2. **Look-Up Tables**

   The CPU loads the Master DSP external RAM, this one contains the LUTs. The Master DSP then transfers these on to the Velocity DSPs via the serial links.

3. **Configure Input Dispatcher**

   The Master data bus is also connected to the Input Dispatcher, which enables writing of control words. This way we can configure the Input Dispatcher to the specified algorithm and to the specified number of ranges.

4. **Data organization**

   The Master DSP reads the results coming from the different module FIFOs. These results are then put together to form a complete beam, and the head and tail control words are attached.

5. **Checks the amount of data**

   The Master DSP ensures that the desired amount of data comes from the Velocity processors.

6. **Write data to the PipeLink**

   The Master DSP writes the output data with control words to the PipeLink FIFO.

7. **Error situations**

   When an error situation has occurred, the Master analyzes it. Then the slave DSPs normally must be restarted.

   During such an error situation, the processing will be stopped. However, the Pipelink must not be affected, therefore the Master DSP must write dummy data with control words to the PipeLink FIFO. In some special situations this could be difficult, e.g. if the Master DSP looses control of the number of beams in process etc.

15 Control

15.1 VME interface

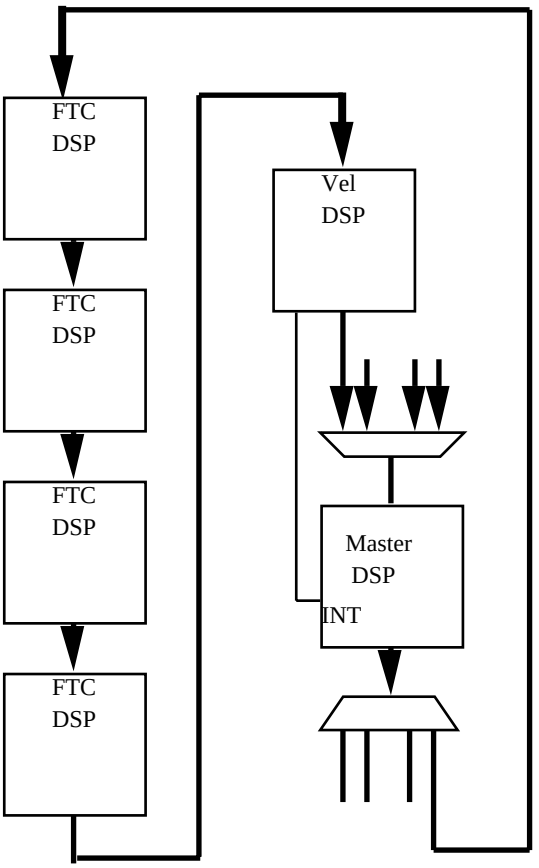
The Master DSP has all the communication with the CPU. When there is a new control word in the VME interface FIFO, the Master gets an interrupt.

15.2 Serial links for program loading and communication

There is one serial port on each of the DSPs. This port uses three pins for input and three for output. The purpose of the serial port is the following:

1. Program loading
2. LUT downloading
3. Parameter changes
4. Error handling
5. Testing of general functionality

Below is shown the serial link for one module (4 FTC DSPs and 1 VEL DSP).



16 Outputs

Pipelink Interface

The main output from the board is the pipelink bus carrying the color flow data from 2DF to the Image Port.

Your Notes:

The Display and Control System

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the Display and Control modules in the instrument.

Modules and subsystems described in this part of the manual

The listed modules and subsystems are described in this part of the manual:

Module / subsystem	Page
Image Port Board - rev. 02	A4-3
Image Port Board - rev. 02	A4-3
Image Memory board - rev. 03	A4-10
Scan Converter Board - rev.01	A4-12
Graphic Processor - rev.01	A4-15
CPU board - rev.02	A4-17
Mother Board - rev. 01	A4-20

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A4_01_Displ_Contr_innh.03.
Printed: December 5, 2000.

Your notes:

Image Port Board - rev. 02

1 Overview

1.1 Abstract

The system function of the Image Port (IMPORT) is to capture signal processed data from the mid section boards, RFT, SDP and 2DF, or a VCR, and route this data to the appropriate locations in the Image Memory.

The generated data sets are organized as ring-buffers in the Image Memory. The data sets will either be picked up by the Scan Converter for real time imaging, or by software for replay or history processing.

1.2 Revision History

Rev.	Date	Sign.	Description
01	5 Aug. 1994	GRL	First version of document
02	21 Sep 1999	LHS	Minor update

1.3 Definitions/Abbreviations/Nomenclature

Please refer to “Abbreviations, Definitions, Glossary, Terminology, Nomenclature” on page P-1.

1.4 References

- Image Port on page A4-53
- Image Port Block Diagram – rev. 01 page H4-14
- Board Revision History page H4-1

2 Inputs

2.1 PipeLink input

The PipeLink data entities are called Frame, Packet and Tuple. At the Image Port the Packet will be collapsed. The data entities at the Image Port will hence be referenced Frame and Vector.

The Vector size will be between 64 Bytes and 8 KBytes depending on the data type:

2.2 Video input

Video or S-VHS is received from the VCR via the Internal I/O board.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A4_02_03.fm.
Printed: December 5, 2000.

3 Descriptions

3.1 Pipelink Data Type Decoder

The data and control parts of the incoming data flow are demultiplexed and dispatched to the respective FIFOs.

3.2 Video A/D conversion and decoding

The luma data, chroma data and control parts of the incoming data flow are first digitized, then demultiplexed and dispatched to the corresponding FIFOs.

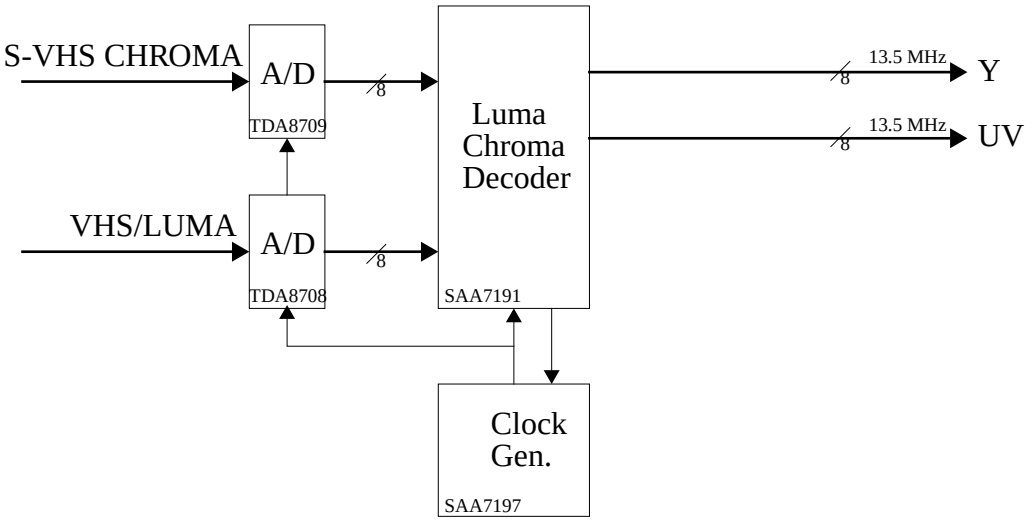


Fig. 3.1 Video input quantization and decoding

Fig. 3.1 shows the Video input dataflow. There are physically one VHS and one S-VHS input. which are individually digitized. The digital video multi-standard decoder generates the decoded luminance and chroma data. The decoder is programmable to take either PAL or NTSC format in either digitized S-VHS or VHS.

3.3 FIFO buffers

The task of the FIFO buffers is to ensure that the Image Port can consume the incoming data in absence of VME mastership, and to buffer full VME block size before requesting the VME slave.
A dedicated control FIFO is connected to the PipeLink input in order to make the target Vector address calculation in parallel with the VME block transfer of the previous Vector.

3.4 Image Port Controller

The purpose of this block is to control the data flow through the FIFOs. It also generates the addresses for the Image Memory board, so that the different data types is placed in the correct ring buffers.

4 Outputs

4.1 Output to Image Memory

The dataflow destination is the Image Memory board. Data transfer is done over the VME bus.

4.1.1 Data sets

Each scan mode will produce data to a corresponding data set in the Image Memory. The data sets are represented in ring-buffers. Each active data set will be allocated to one of the following types of acquisition data:

- 2-D tissue data
- Doppler data
- M-mode data
- Colour flow
- Trace data
- Video Y-component data
- Video UV-component data
- Colour M-mode data
- RF data

The Image Port can support dynamic demultiplexing of the input flow and corresponding mapping to up to 8 different data set ring-buffers.

Image Port 2 Board - rev. 01

5 Overview

5.1 Abstract

The system function of the Image Port 2 (IP2) is to capture signal processed data from the instrument or a VCR, and route this data to the appropriate locations in the on-board Image Memory.

The generated data sets are organized as ring-buffers in the Image Memory. The data sets will either be picked up by the Scan Converter for real time imaging, or by software for replay or history processing.

5.2 Revision History

Rev.	Date	Sign.	Description
01	10 Sep.1999	TS/LHS	First version of document

5.3 Definitions/Abbreviations/Nomenclature

Please refer to “Abbreviations, Definitions, Glossary, Terminology, Nomenclature” on page P-1.

5.4 References

- Image Port on page A4-53
- Board Revision History starting page H4-1

6 Inputs

6.1 PipeLink input

The PipeLink data entities are called Frame, Packet and Tuple. At the Image Port the Packet will be collapsed. The data entities at the Image Port will hence be referenced Frame and Vector.

The Vector size will be between 64 Bytes and 8 KBytes depending on the data type:

6.2 Video input

Video or S-VHS is received from the VCR via the Internal I/O board.

7 Board Description

7.1 Scanner Dataflow

- The scanner data input format is the PipeLink format.
- Demultiplexing and mapping of scanner dataflow can be done in up to eight data set ring-buffers in the onboard Image Memory.

- The peak data rate is 20x1 MBytes/s or 20x2 MBytes/s in bursts of 32-2048 Bytes.

7.2 Video Dataflow

- Video input is supported in these formats:
  - SVHS - PAL,
  - SVHS - NTSC,
  - PAL,
  - NTSC.
- Physically there is one S-VHS and one composite video input from VCR and one SVHS input from the Graphic Board.
- The VCR data is mapped separated into one Y (luminance) ring-buffer and one UV (chroma) ring-buffer in the Image Memory.
- It is possible to map only the luminance component to the Image Memory.
- It is possible to lower the input dataflow rate by selecting a Region Of Interest and/or by lowering the spatial resolution within the selected region and/or by decimation in time.

7.3 Mixed Scanner/Video Input Dataflow

- It is possible to run the input dataflow from Scanner and Video simultaneously.

7.4 Data Set Ring Buffers

- The Image Port 2 supports DMA to up to a total of 8 ring buffers simultaneously.

7.5 Video Input

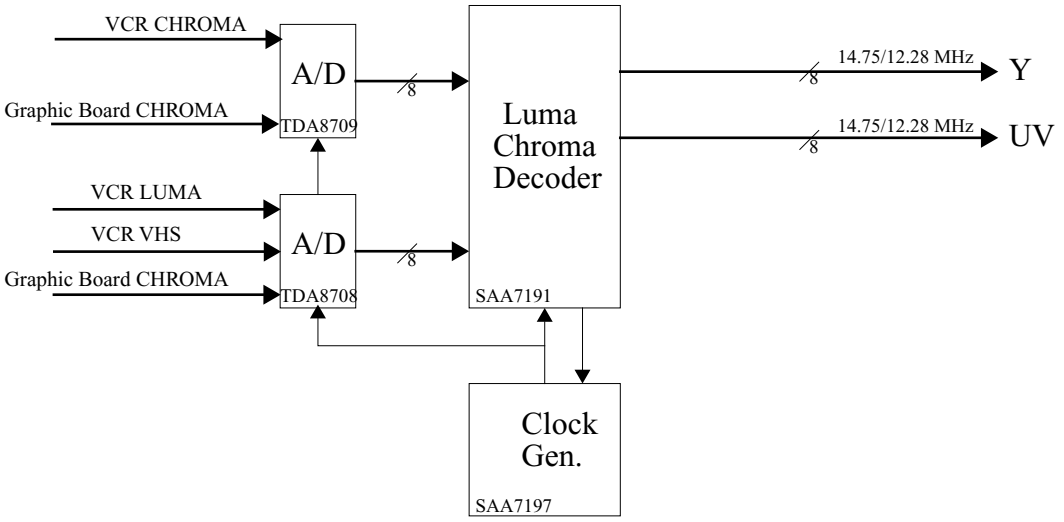


Fig. 7.1 Video input quantization and decoding

Fig. 3.1 shows the Video input dataflow. There are physically one VHS and one S-VHS input for VCR and one S-VHS input from the Graphic Board. The digital video multi-standard decoder generates the decoded luminance and chroma data. The

decoder will detect the Video Standard; either PAL or NTSC format in digitized S-VHS or VHS. The decoder is programmed to differ between VHS and S-VHS.

7.6 FIFO buffers

The task of the FIFO buffers is to ensure that the Image Port 2 can consume the incoming data in absence of local bus mastership, and to buffer local bus burst width for best bus utilization before requesting the local bus.

There are three data FIFOs:

- one for PipeLink,
- one for Video Luma and
- one for Video Chroma.

There are one dedicated control FIFO for both the PipeLink and Video input, storing control information of the vectors in the data FIFOs. One entry is pushed into the control FIFO by HW after the complete data vector is pushed into the corresponding data FIFO. The vector will however be split by HW in pieces of 2048 bytes if the PipeLink vector exceeds this 2048 byte size; an entry in the PipeLink control FIFO will correspond to <= 2048 bytes in the data FIFO.

7.7 Output to Image Memory

The dataflow destination is the onboard Image Memory. The local SW will get an interrupt when a control FIFO gets non-empty. This will make the local SW start reading the control FIFO, identifying its source and calculating the destination address in the Image Memory. The data FIFO data corresponding to the control FIFO entry will be pulled over to the Image Memory destination initiated by the local SW that write the address to an address register. This address registers can be updated by four local bus addresses; one for each data FIFO bank identifying the source data FIFO and one for just updating (testing) the address register without data FIFO pulling. The HW will decode an address update with FIFO pull, requesting the local bus and start to empty one data FIFO entry to the Image Memory. The end of the data vector is defined by two tag bits in the data FIFOs (which are 36 bits wide). When a split termination is tagged, the termination tagged data FIFO entry is part of the vector entering the Image Memory. When a no-split vector termination tag is encountered, the tagged data FIFO entry is not part of the vector entering the Image Memory.

7.7.1 Data Sets

Each scan mode will produce data to a corresponding data set in the Image Memory. The data sets are represented in ring-buffers. Each active data set will be allocated to one of the following types of acquisition data:

- 2-D tissue data
- Doppler data
- M-mode data
- Color flow
- Trace data
- Video Y-component data
- Video UV-component data

- Color M-mode data
- RF data

The Image Port 2 will support dynamic demultiplexing of the input flow and corresponding mapping to up to 8 different data set ring-buffers.

8 Dataflow Control Description

8.1 Input Flow Decode / Capture

8.1.1 PipeLink

The data and control parts of the incoming data flow are demultiplexed and dispatched to the respective FIFOs.

8.1.2 Video

The luma data, chroma data and status data parts of the incoming data flow are demultiplexed and dispatched to the corresponding FIFOs.

8.2 Output Flow Control

8.2.1 The Image Port DRAM

Image Port 2 supports up to 4 SIMM banks of either 16MByte/bank or 64MByte/bank of 72 pins SIMM EDO modules. There are 4 SIMM sockets (1:4) which can contain one or 2 banks; all 4 sockets can be used when using 1 bank SIMM modules while SIMM sockets 1 and 3 may be used for 2 bank SIMM modules.

There must always be mounted a SIMM module in SIMM socket 1.

8.2.2 The Image Port FLASH

The boot code and the production configuration information is situated in the so called boot block of the FLASH. This block has hardware protection which can be overrided by inserting the un-protection jumper on the board. The minimum size of the FLASH will be 512 Kilobyte with optional sizes up to 2 Mbyte.

The Image Port will after power-up (i.e. PCI reset) Retry PCI configurations cycles until the boot code has set our PCI memory size, Vendor Subsystem ID, Subsystem ID and turned off the control bit that makes the PCI slave interface Retry PCI configurations cycles. In this way our boot code is able to program our memory size and IDs before any Host CPU can read it with a PCI Configuration cycle.

8.2.3 The Image Port Video Decoder

The Image Port Video Decoder is based on the SAA7191 from Philips. It is connected to the I^2C bus mastered by the I960RP. The CSR registers in the Video Decoder is accessed over the I^2C bus by I960RP code using the I^2C interface registers.

The Video Decoder supports both PAL and NTSC video formats and will be programmed prior to Video capture.

Image Memory board - rev. 03

9 Introduction

9.1 Abstract

This document is a description of the Image Memory board (IMMEM) in SYSTEM FIVE. The board is commercially available from Micro Memory Inc., USA, and the description is based upon information found in the Users Guide for the board.

Starting second half of 1999, a new Image Port board with onboard memory was introduced as an alternative to the Image Port board/ Image Memory board combination. See “Image Port Board - rev. 02” on page A4-3 for details.

9.2 Document History

Rev.	Date	Sign.	Description
01	22 Aug. 1994	GRL	First version of document
02	1.Nov. 1999	LHS	Included info about IP2 board
03	01 Nov.2000	JB	Moved Test and Diagnostics to Ch.K

9.3 Definitions/Abbreviations/Nomenclature

RAM – Random Access Memory

PLD – Programmable Logic Device

LED – Light Emitting Diode

9.4 References

Image Memory Block Diagram – rev. 01 on page B2-15

Image Port Board - rev. 02 on page A4-3

10 Descriptions

10.1 General

The Image Memory board is fully compatible with the VME bus specifications. It can handle data widths of 8, 16, 32 or 64 bits and address widths of 24 or 64 bits.The memory array can be addressed as 8 bit bytes, 16 bits words or 32 bit longwords, using conventional Read/Write, Read/Modify/Write or high-performance block transfers.

10.2 Memory Size

The board can be stuffed with different amount of RAM, ranging from 32 MBytes to 512 MBytes. It is designed to accept 4096K x 9 dynamic RAM modules with 80 ns typical delay. (Eight of the 9 bits are used for data, one for parity).

10.3 Address Decoding

The board contains its own address register and data buffers for each port, and responds to various Address Modifier Codes, decoded by an address decoder PLD. Various combinations are available.

10.4 Parity Control

A parity Generator/Checker stores and checks an even parity bit for each byte written on write cycles. In case errors are found, a bit can be set in a Control Status Register, and a bus error signal activated, lighting up a red LED.

10.5 Refresh

The RAM is refreshed once every 15 us. The cycle interval is generated by a free running oscillator, providing a refresh transparent to memory access cycles. If a memory access cycle takes more than 15 us, the board counts the number of refresh requests, and upon completion of the cycle, the refresh circuit runs up to 31 stored refresh requests. If memory cycles last more than 420 us, thus preventing refresh, data will possibly be corrupted.

Scan Converter Board

11 Overview

11.1 Abstract

This document describes the Scan Converter board (SCONV). The SCONV board fetches the different types of data from the Memory board using VME DMA transfers. Its main purpose is to convert the data stored in the image memory to a display format which gives a true view of what was actually scanned.

11.2 Document History

Rev.	Date	Sign.	Description
01	1/13/98	GRL	First version of document

11.3 Definitions/Abbreviations/Nomenclature

11.4 References

Scan Converter Block Diagram – rev. 01 on page B2-16

12 Inputs

VME Interface

The main input to the board is the VME bus, where data from the Image Memory board is fetched. The VME bus is located on both the P1- and the P2 connector.

13 Descriptions

13.0.1 VME Interface and Input FIFOs

The VME Interface is located between the VME bus and the Input FIFOs. It is 64 bit wide (32 bit data and 32 bit address). The even and odd vectors are grouped in a certain way. Maximum vector length is 1024 bytes (2D). Each FIFO is 512 bytes deep and they operate at 40 MHz using 32-bit interleaving. The output of the FIFOs are read at 25 MHz.

13.1 Time Domain Processor

Address and data is fed from the Input FIFOs into a so-called Time Domain Processor (TDP). The TDP performs *recursive filtering* of the data which is still on a sample/vector format, and stores the data in one of three memory banks depending on data type. The three banks are for simultaneous storage of tissue data, flow-frequency data and flow-bandwidth data.

13.2 Space Domain Processor

The different types of data are now stored in separate *memory banks*, and can be read out in three parallel paths for further simultaneous processing in the Space Domain Processors (SDP).When addressing these memories, the actual *scan conversion* takes place. Each of the banks have separate addresses since the output formats/shapes are different for e.g. a 2D Tissue sector and a 2D Flow sector. The addresses to the memories are derived from the CRT x and y counters and the selected format shapes.

Sector for 2D tissue and 2D flow (phased array and annular array probes).

Rectangle for tissue and parallelogram for color (linear array probes).

Rectangle for tissue, M-Mode tissue, M-Mode color, spectrum, traces, video.

Parallelogram for both 2D tissue and 2D flow.

Full circle for tissue (intravascular catheters).

Samples are read out four by four in three parallel paths. Four samples are first mapped through compression PROMs before they are used for *interpolation* of the value of the closest pixel. There are different interpolation filters for tissue, flow-frequency and flow-bandwidth. The interpolation scheme for the flow-frequency component is done in such a way that frequency aliasing is avoided. The output of the interpolator is fed to a pixel encoder.

13.3 Pixel Encoding

The different data types have different encoders or look-up tables to get from data codes to 24 bit RGB. After conversion to RGB, all data types are input to a multiplexer, where only one type can be output at the time (pixel by pixel).

13.3.1 Video Encoder

Video information (back from the VCR) which is demodulated on the Image Port board and stored on the Memory board, can also be fed through the Scan Converter board. Video is stored as digital luminance and chrominance, and is fed through an encoder and converted to digital RGB in a special matrix multiplier chip.

13.3.2 Tissue Encoder

This is a look-up table which purpose is to provide the compress- and reject functions.

13.3.3 Flow Encoder

The CFM signal is re-encoded from two components (velocity-intensity or velocity-bandwidth) to the three-component RGB signal in look-up tables.

13.3.4 Tissue/Flow Arbitration

The two CFM components are fed to a look-up table (within the Tissue/Flow Arbiter block) and is given an “equivalent” 2D Image value. This value is compared to the 2D Tissue pixel value, and the greater is selected in the Pixel Multiplexer. Eight choices of look-up tables are available, thus, different arbitration levels can be selected depending on use.

13.4 Pixel Port Interface

The Pixel Port is a synchronous multiplexed 24 bit bus. It is capable of transferring up to one scan-line in a single burst. Data is coming from the The 24 bit address uses 12 bit for line address, and 12 bit for pixel position within a line.

By interfacing the bus through a FIFO, the SDP can run asynchronously on the pixel level with the Pixel Port. The FIFO can hold up to two scan-lines.

Before pixel data is presented out on the Pixel Bus, it is multiplexed with the pixel address.

14 Control

The SCONV board is entirely controlled by the CPU board through the VME bus.

15 Outputs

15.1 Pixel Bus

The main output of the board is the above mentioned Pixel Port, taking the digital 24 bit RGB signal to the Graphics board. This bus is located on the P2 connector.

Graphic Processor

16 Introduction

16.1 Abstract

This document is a description of the Graphics board (GRAPH) in SYSTEM FIVE . The board converts a 24 bit digital RGB code from the Scan Converter board (via the pixel bus) to analog RGB for both a high resolution monitor and a standard PAL/NTSC monitor or printer. In addition, the board provides support for an X-server and several under- and overlays.

16.2 Document History

Rev.	Date	Sign.	Description
01	13 Jan 1998	GRL	First version of document

16.3 Definitions/Abbreviations/Nomenclature

16.4 References

Graphic µP Board Block Diagram – rev. 01 on page B2-17.

17 Descriptions

17.1 Pixel port

The Graphics board gets its data from the Scan Converter board over the Pixel bus which is a high speed bus providing 24 bit “true color” (8 bit each for R, G and B) at a burst bandwidth of 20 Mpixels /second. The bus is both writable and readable.

17.2 Video RAMs

The board can drive two independent monitors, one high-resolution main screen and one video monitor (or VCR); the screen formats can range from 640*480 to 1024*1024 pixels. Data from the pixel port is demultiplexed and fed to four banks of dual port video RAMs providing a 24 bit underlay for imaging. The RAMs can be accessed simultaneously for both the main screen and the standard video output.

17.3 VME Interface

From the VME interface, two separate overlays are provided. One overlay is for the window system, and the other is for video.

17.4 X-server

The Graphics board supports a window system x-server.

17.5 RAMDAC and RGB outputs

Two RAMDACs, one for system the monitor RGB and one for PAL/NTSC RGB convert the digital 8 bit R, G and B words to analog RGB, which is buffered before fed out of the GRAPH board. System RGB is available on three coax connectors on the motherboard, while PAL/NTSC RGB is routed to the INT I/O board over the motherboard.

17.6 Video and S-VHS outputs

Both PAL and NTSC video and S-VHS outputs are provided for VCRs and printers. The signals are routed to the INT I/O board for buffering and further distribution to both internal peripherals and external devices (via the EXT I/O board).

17.7 Serial Interfaces

The GRAPH board provides serial RS-232 communication with the front panel. In addition there are two more serial ports routed to the INT I/O board.

17.8 MC68040 uP

A standard MC68040 microprocessor is the controller on the board.

CPU board

18 Introduction

18.1 Overview

This document is a description of the CPU board in SYSTEM FIVE. The board is based upon the MC68040 microprocessor and contains the following circuitry:

- 4 to 64 MB DRAM
- 8 kB NV RAM (with battery backup)
- 128 kB static RAM
- Clock (with battery backup)
- Ethernet transceiver interface
- Four serial ports with EIA-232-D interface
- Four tick timers
- Watchdog timer
- EPROM sockets
- SCSI bus interface
- Centronics parallel printer port
- VME bus interface and VME bus controller

18.2 Document History

Rev.	Date	Sign.	Description
01	19 Aug. 94	GRL	First version of document
02	22. Sep. 95	LHS	Updated layout
03	01 Nov.00	JB	Moved Test and Diagnosticsto Ch.K

18.3 Definitions/Abbreviations/Nomenclature

RXD – Receive data

TXD – Transmit data

CTS – Clear to send

RTS – Request To Send

ASIC – Application Specific Integrated Circuit

18.4 References

CPU Block Diagram – rev. 01 on page B2-18.

19 Descriptions

19.1 MC68040 Microprocessor

The device has on-chip instruction and data caches and a floating point processor.

19.2 Internal Data Bus Structure

The bus is a 32-bit synchronous bus that is based upon the MC68040 bus. The various devices use this bus to communicate. The devices are given different priorities in a arbiter, and in general, any master device can access any slave. However, there are restrictions.

19.3 EPROM

The 4 EPROMs are organized as two 32-bit wide banks that support 8-, 16-, and 32-bit read accesses. They are mapped at address 0, following a local bus reset, thus, the uP can access the stack pointer and execution address following a reset.

19.4 Static RAM

The 128 kB of 32-bit wide static RAM supports 8-, 16-, and 32-bit accesses, providing possibilities for debugging and limited diagnostics without having to access the DRAM piggyback.

19.5 Dynamic RAM

The DRAM is located on a piggyback board. These boards are available with 4, 8, 16 and 32 MB, and two boards can be used with one CPU board. (One stacked on top of the CPU as a piggyback, and the other requiring a separate slot in the rack).

19.6 NVRAM and Clock

A combined RAM and clock chip (MK48T08) provides the time of day clock, oscillator, crystal, power fail detection, memory write protection, 8KB of RAM and a battery, all in one chip.

19.7 VME bus Interface

An ASIC (VMEchip2) provides the interface between the local bus and the VME bus, and the local-VME bus DMA controller functions.

19.8 Serial Port Interfaces

Four serial; ports are provided by a CD2401 serial controller chip. Baud rates ranges from 110 to 38.4K. Serial port 1 is a minimum function asynchronous port using RXD, CTS, TXD and RTS. Serial ports 2 and 3 are both full function asynchronous ports and serial port 4 is a full synchronous or asynchronous port. All four ports have drivers and receivers routing the input/output lines to the P2 connector.

19.9 Parallel Port Interface

An ASIC (PCCchip2) provides an 8-bit bidirectional parallel port. In addition to the 8 bits of I/O data, there are two control signals and 5 status signals, which can interrupt

the uP. The port can be used as a Centronics-compatible printer port, or as a general parallel I/O port.

19.10 Ethernet Interface

A 82596CA is used to implement the Ethernet transceiver interface. The device accesses local RAM using DMA operations to perform its normal functions. Each MVME167 board is assigned an Ethernet Station Address (displayed on a label attached to the P2 connector). The address is also stored in the NVRAM.

19.11 SCSI Interface

A NCR 53C710 SCSI I/O controller provides support for mass storage subsystems to be connected. Such devices are hard-, optical- and floppy disk drives.

Mother Board

20 Introduction

20.1 Overview

The Motherboard design includes a 16 slot VME 64 bus architecture. It does also include a 16 bit FE bus and some analog buses, video and analog signals.

20.2 Document History

Rev.	Date	Sign.	Description
01	25 Aug. 97	LHS	First version of document

20.3 Definitions/Abbreviations/Nomenclature

FE bus: Front End data bus.

VME 64 bus: A data bus following the VME standard

20.4 References

Motherboard with Major “Buses” — rev. 02 on page B3-6.

21 Description

21.1 Overview

The Mother Board is acting as a back plane for most of the other cards in System FiVe. It is routing both power and data to and between the cards and the I/O.

There is only one active component on the Motherboard, an IC used for configuration
purposes.

21.2 Main Data Buses

- VME-bus, see “VME Bus (VME 64)” on page A1-65.
- PIXEL BI, see “from IMMEM to CPU/GRAPH (a.o. for test).” on page A1-66.
- Pipelink bus, see “Pipelink Bus” on page A1-62.
- MLA bus, see “MLA Buses” on page A1-61.
- Clocks, see the description starting on page A1-68 and the block diagram on page B3-3.

The Front Panel

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the Front Panel module in the instrument.

Modules and sub-systems described in this part of the manual

The subsystem described in this part of the manual:

Module / subsystem	Page
Front Panel – rev. 02	A5-3
Front Panel Controls – rev. 04	A5-7

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A5_01_Front_Panel_inmh.03.
Printed: December 5, 2000.

Your Notes:

Front Panel

1 Overview

1.1 Abstract

This document is a description of the Front Panel in SYSTEM FIVE . It consists of a Main board, a Rotary/display board, an Audio Amplifier board and a Qwerty Adapter board. The Front Panel is constructed around a uP6809 processor and contains several types of inputs/output registers which are used in encoding/decoding of the different devices connected to the Main board. It has serial communication with the rest of the system through an RS-232 link to the Graphics board.

1.2 Document History

Rev.	Date	Sign.	Description
01	10 Aug. 94	GRL	First version of document
02	01 Nov.00	JB	Moved Test Features to Ch.K

Macintosh HD:User:James:@I-arb:Service:S5_ServiceMan:S5_serv_files:A5_02_01_FP.
Printed: December 5, 2000.

1.3 Definitions/Abbreviations/Nomenclature

TGC: Time Gain Compensation

LED: Light Emitting Diode

1.4 References

Front Panel Block Diagram – rev. 01 on page B2-19.

2 Inputs

Below is a table showing the main inputs.

PIN #	SIGNAL	DESCRIPTION	SOURCE	LEVEL
P8-10, 11 and 12	FOOTSW0-2	Footswitch signals	Footswitch via INT I/O	TTL
P8-8	ACSYFP	Serial communication from system to front panel	GRAPH via INT I/O	RS-232 (+/- 12V)
P8-9	FPRES_L	Front Panel reset	INT I/O	TTL
	FP_AUDIO_L/R	Doppler audio left and right	SDP via INT I/O	1 Vrms (max)

3 Descriptions

3.1 Local uP

The uP (U2) is a Motorola MC6809 microprocessor running at 2 MHz, derived from a local 8 MHz crystal oscillator. All I/O devices described later are memory mapped. The uP can be interrupted by timers, the trackball, the IR remote control and the two serial ports. The uP can be reset by the system (FPRES_L), by pressing a local reset switch (SW1) or during power-up by a power-up-reset circuitry.

3.2 RAM and EPROM

The front panel contains 32 kB RAM (U4), where the lower part of the memory space is used for the I/O devices, and the upper part is used for the stack and the 32 kB program EPROM.

3.3 Address Decoder

Two PALs, ADDEC (U1) and DISPL (U3) provide the chip select signals to the different devices.

3.4 Revision Detection

The board part number and revision is written into a PAL, FPREV (U6). This information can be read by the uP and transferred to the system.

3.5 Serial Interface

There are two asynchronous RS-232 serial ports based upon a MC68681 DUART. One port is for communication with the system (Graphics board) and another (not currently used or shown on block diagram) can be used for VCR control.

3.6 VIA

The Versatile Interface Adapter (VIA) contains two 8 bit parallel I/O ports used to control the below described devices.

3.6.1 Beeper

The beeper can be activated by pulling the BEEP_L signal low.

3.6.2 LED activators / backlighting

The keys are lit in two steps: Backlighting is provided by enabling a BLEN_L signal, giving a quit dim light. This signal is automatically turned low when the ambient light is low, sensed by a light dependant resistor (RL1).

Whenever a button is depressed, the LED_EN_L signal (specific for each LED) is enabled, causing the current through the LED to increase, again increasing the light strength.

3.6.3 Trackball

The trackball interrupts the uP through the VIA when moved. Both it's X, Y and two quadrature outputs are connected to the VIA.

3.6.4 Toggle switches

The state of both toggle switches are sensed through the VIA.

3.6.5 Infrared (IR) Remote Control

The remote control interface has provisions for 32 different keys. The receiver and amplifier located on the Rotary/display board sends serial data to a receiver chip on the Main board. This device is connected to the VIA with five data signals and a IRDR_L (data ready) signal.

3.7 TGC slide potentiometers

The center tap of each of the 8 slide pot's are buffered and fed to a multiplexing 8 bit A/D converter giving out a digital value every 9 ms. The uP reads the TGC values independently of the conversion rate from a dual port RAM built into the A/D converter.

3.8 QWERTY keyboard and switch decoding

The overall keyboard matrix is 23 rows by 8 columns giving a maximum of 192 keys. One part of the matrix is used for the QWERTY keyboard, the rest is used for the other push-button keys. The matrix is address mapped. All columns are pulled high with resistors, and pushing a button causes that particular line to go low.

3.9 Rotary / displays board

3.9.1 Rotary decoding

The rotary switches are address mapped and read in pairs. They have 16 positions per revolution, and each position represents a four bit gray code which can be read by the uP.

3.9.2 Displays

The two displays (DP1, DP2) are character LCD units, with built-in control LSI. They operate under control of the uP, and displays alphanumeric characters and symbols. Two control signals (EN0 and EN1) from the address decoder, enables the displays.

4 Control

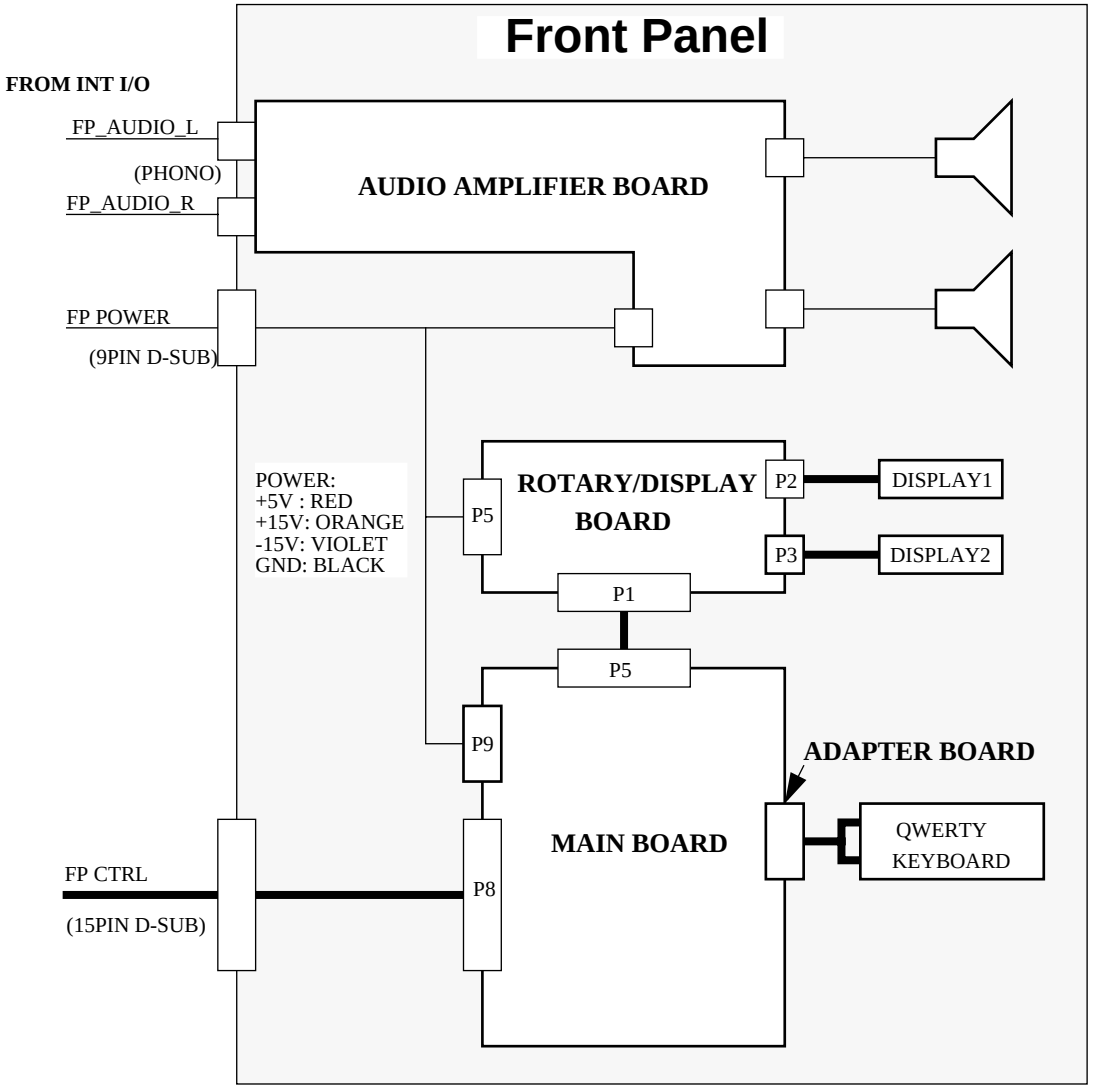
The front panel uP communicates serially with the system over an RS-232 port. Locally, the uP controls the front panel.

5 Outputs

Below is a table showing the main outputs.

Pin #	SIGNAL	DESCRIPTION	DEST.	LEVEL
P8-7	ACFPSY	Serial communication from front panel to system.	GRAPH via INT I/O	RS-232 (+/- 12V)

6 FP Cable Harness



7 Control

The front panel uP communicates serially with the system over an RS-232 port. Locally, the uP controls the front panel.

Front Panel Controls – rev. 04

1 Introduction

1.1 Abstract

This document lists the Front Panel Controls and the boards which are affected when these controls are adjusted.

The controls are implemented via:

- keyboard knobs,
- assignable rotaries,
- assignable keys or
- paddlesticks.

1.2 Document History

Rev.	Date	Sign.	Description
01	2. May 1995	GRL	First version of document
02	18 Oct. 1996	GRL	Updated per V111 release
03	21. Oct. 1999	LHS	Updated text
04	01 Nov 00	JB	Corected text

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A5_03_FP_ctrl.04.
Printed: December 5, 2000.

2 Description

Table 1: 2D Controls

Control parameter	Implemented on...
2D Gain	RFT
TGC	RFT
Depth	FEC, RFT, SCONV
Zoom	FEC, RFT, SCONV
Left/Right	SCONV
Compound (FLA only)	FEC, RFT, SCONV
Compress	SCONV
Reject	SCONV
Angle (or Width)	FEC ->TX, BF, RFT, SCONV
Contour	RFT
Freq	FEC->TX, RFT
Framerate	FEC, RFT

Table 1: 2D Controls (Continued)

Control parameter	Implemented on...
Focus	FEC->TX, RFT
Dynamic Range	RFT
Tilt	FEC->TX, BF
DDP	SCONV
B-Color	SCONV
Power	FEC-> TX POWER-> TX

Table 2: Color Flow Controls

Control parameter	Implemented on...
Gain	RFT
TGC	RFT
Depth	FEC, RFT
Zoom	FEC, RFT, SCONV
ROI Width	FEC->TX, BF, RFT, SCONV
ROI Span	RFT
Color Maps	SCONV
Variance	SCONV
LV Reject	2DF
PRF	FEC, RFT, 2DF
Sample Volume	RFT
Sample Volume Pos. (t.b)	RFT
Tilt (FLA only)	FEC->TX, BF, RFT,
Baseline	SCONV
Tissue Priority	SCONV
DDP	SCONV
Lateral Averaging	2DF
Radial Averaging	2DF
Framerate	FEC, RFT
Power	FEC -> HV POWER -> TX

Table 3: M-Mode (specific) Controls

Control parameter	Implemented on...
Horizontal Sweep	RFT, SCONV

Table 4: Color M-Mode (specific) Controls

Control parameter	Implemented on...
Horizontal Sweep	RFT, SCONV

Table 5: Doppler Controls

Control parameter	Implemented on...
Gain	RFT
Velocity range	SDP, FEC
Baseline	SDP
Horizontal Sweep	
Compress	SDP live, SCONV frozen
Tracking	SDP
Sample Volume	RFT
LV Reject	RFT
Temp Res	SDP
Radial Averaging	SDP
Reject	SDP live, SCONV frozen
Overrange	SDP
Framerate	FEC, RFT
Power	FEC -> TXPOWER -> TX

Your Notes:

The I/O modules

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the I/O modules in the instrument.

Modules and sub-systems described in this part of the manual

The listed modules and subsystems in this part of the manual:

Chapter	Module / subsystem	Page
1 - 2	Internal I/O Board - rev. 03	A6-3
3 - 4	External I/O board - rev.02	A6-11

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A6-01_io-innh.02.
Printed: December 5, 2000.

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Internal I/O Board - rev. 03

1 Overview

1.1 Abstract

This document describes the Internal I/O board (INT I/O) in System FiVe. The board buffers all signals used for internal peripherals, for disk drives and for the Front Panel, and is also the interface between the External I/O board and the system.

1.2 Document History

Rev.	Date	Sign.	Description
01	5 Aug. 94	GRL	First version of document
02	20 Apr. 95	GRL	Change on Ethernet interface.
03	22. Apr. 99	LHS	Updated the Ethernet description pluss some smaller changes.

Macintosh HD:User:James:@h-arb:Service:S5_ServiceMan:S5_serv_files:A6_02_Internal.03.
Printed: December 5, 2000.

1.3 Definitions/Abbreviations/Nomenclature

Please refer to the Abbreviations, Definitions, Glossary, Terminology, Nomenclature list starting on page P-1.

1.4 References

- Internal I/O Block Diagram – rev. 01 on page B2-20,
- Board formats, INT I/O on page A1-75,
- Board Compatibility List on *page H2-1,*
- Internal I/O and Peripheral Control on page A1-55
- Assembly drawing, Internal I/O — Component Side - rev. E on *page M-5*
- Assembly drawing, Internal I/O — Solder Side - rev. B on *page M-6*
- Internal I/O Replacement Proc. - rev. 01, on *page L-15*

2 Descriptions

2.1 VME Interface

The VME interface consists of a common VME DSP control interface used on all MID boards. The VME interface consists of:

- Input message FIFO
  Make it possible for the CPU to send a message to the INT I/O board.
- Output message register
  Make it possible for the DSP to send a message to the CPU.
  Make it possible for the DSP to generate a VME interrupt.
- VME interface status register
- VME interface control register

2.2 Video buffers and video switches

Composite video out, S-VHS out and RGBS out are buffered with operational amplifiers before fed to the peripherals.

Composite video in and S-VHS in (from VCR or external devices) are fed through video multiplexers before routed to the Image Port board.

2.3 Audio buffering and audio switching

Audio from the SDP board is first buffered by operational amplifiers, then fed through an analog switch which selects between the SDP audio and the replay audio from the VCR. The output from the switch is fed to the Front Panel Audio Amplifier.

2.4 Footswitch Interface

The three input lines from the footswitch is read directly by the DSP. Assignment of the lines can be configured in software.

2.5 Patient I/O Interface (incl. DSP)

Fig. 2.1 illustrates the HW necessary for the Patient I/O at the Internal I/O board. The DSP will perform all overhead required for chip selects, in/out selection, and other tasks required for controlling all interfaces.

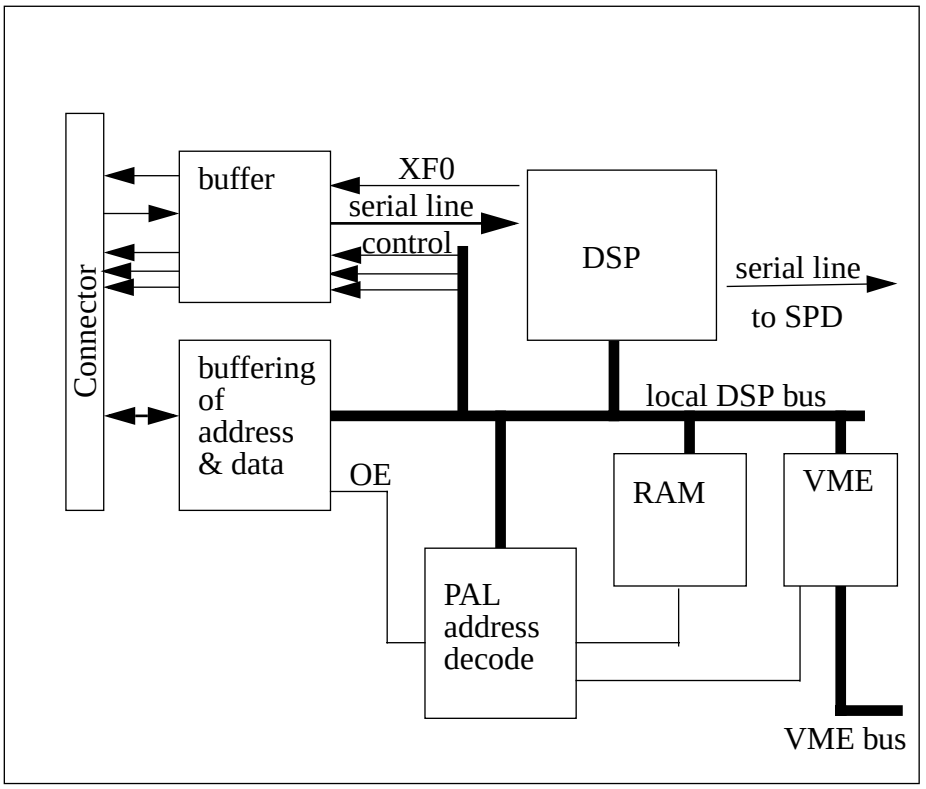


Fig. 2.1 HW block schematics for the DSP at the Internal I/O board.

The Patient Interface is built around the TMS320C40 Digital Signal Processor. The DSP has a data and address bus (multiplexed) for Patient Module gain programming.

A 37 pins DSUB (FEMALE) connector includes all serial and parallel signals, and power (± 15V) for the Patient I/O module. All transducer input signals are A/D con-

verted and transferred serially from the Patient I/O module to the Internal I/O module. The DSP on the Internal I/O board performs all required signal processing, like decimation, powerline filtering and detection (of ECG, QRS, heart sound, respiration). Hardware for data transfer to the SDP module and the Patient I/O for configuration setup is also included on the Internal I/O board.

2.5.1 SDP Interface

After processing of the traces, they are fed to the SDP board. When the SPD requests data, all channels are resampled and the data are sent serially to the SPD. Information about the detected features are embedded with the data samples.

2.6 SCSI Interface

This interface is located on the CPU and is dedicated for hard disks or other data storage devices. Required components are only the connector.

The SCSI Interface follows the SCSI-2 standard for 8 bits bus.

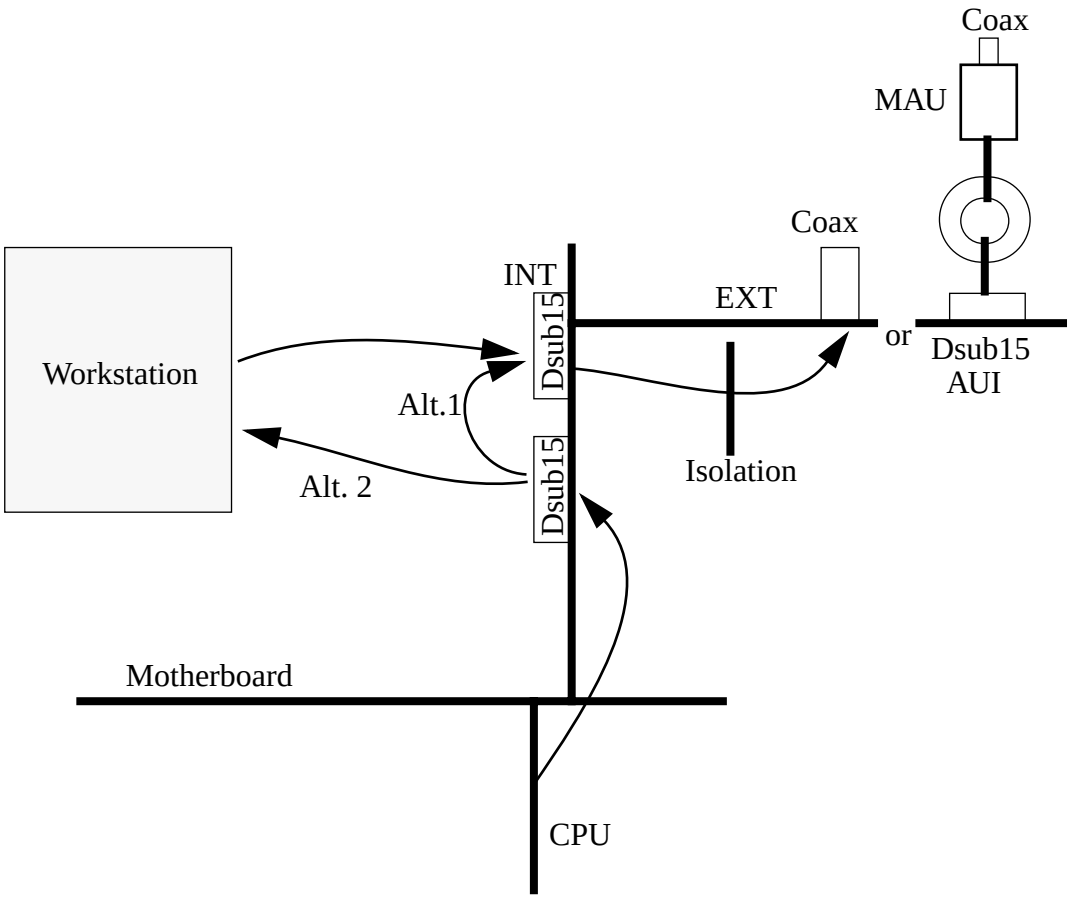
2.7 Ethernet

The Ethernet signals from the system CPU are looped through the Internal I/O board before routed to the External I/O. On the first systems (~15), the signals are fed to a Coaxial Transceiver Interface (CTI), and then to a BNC. This interface is designed for Thinwire Ethernet only, and can not be used with thickwire or twisted pair.

On the newer systems, the Ethernet signals are fed to a 15 pin D-connector (the Attachment Unit Interface - AUI) on the External I/O panel. This allows for connection of all types of Ethernet to the system; one has to use the correct Medium Attachment Unit (MAU). Thus, there will be a cable from the 15 pin D-connector on the I/O panel to a similar connector on the MAU. To minimize interference from the Ethernet connection, this cable should be looped through a ferrite a few turns.

The Ethernet connection is made to the other end of the MAU.

Fig. 2.2 Ethernet connection alternatives



2.8 RS-232 lines

All RS-232 interface are located on the CPU and the GRAPH-5 module. Required components are only 9 pin D-SUB connectors.

The internal I/O board have as a total of 7 serial lines. These are supported from the CPU (4) and the GRAPH 5 board (3), respectively.

The following modules will use these signals:

- VCR remote control (CPU).
- Front Panel (GRAPH 5).
- 2 Internal RS-232 TBD (CPU).
- 3 External RS-232 (GRAPH 5/CPU)

The internal lines will be connected to standard configurated 9 pins DSUB connectors. The number of control signals vary from line to line.

- All GRAPH 5 and CPU line 1 contains only TD/RD/RTS/CTS.
- CPU line 2 and 3 contains in addition DTR/DCD.
- CPU line 4 contains in addition DTR/DCD/RTXC/TRXC.

2.9 AC Power Remote Control

Remote control lines from IV & DP Connector Board to the AC power are supported. The AC power remote control interface detects a remote button action and gives an interrupt to the system CPU. The AC power will not switch off until a grant signal from the CPU is activated.

2.10 Battery backup power

The Internal I/O board will include a lithium or a rechargeable NiCad battery for system data backup RAM.

2.11 Remote Control

These are single lines used to control Hard Copy from Cameras and Printers. Two lines will be supported from the I/O board. The active level is defined in the system configuration menu.

2.12 Parallel signals

The I/O module will include a bidirectional parallel interface (Centronics) for image/text printing on B/W printers and data transfer between a post processing unit.

The parallel interface controller is included on the module. Required components are only a 25 pin D-SUB connector. In order to use as much standard cable assemblies as possible, a standard PC parallel pin out is choose.

This is a standard Centronics port used to support Printers in the system:

2.13 Power Distribution

Voltages available on the Internal I/O module are: +5V, +/- 12V and +/- 15V.

These voltages are required for Disk Drives and Front Panel.

Fuses on the I/O boards for external outputs are provided.

The following units will be supported with DC power from the I/O board:

- The Front Panel.
- Flexi disk (mounted in the Front Panel?)
- HD mounted in free space near to the CPU and I/O board.
- Optical Disk. This may be served with AC power if it is based on a free standing cabinet unit, or with DC power if it is built into the system.
- Patient I/O module.
- External I/O module.

2.14 External I/O signals

Following signals to External I/O module are buffered/routed through the Internal I/O module.

2.14.1 Composite Video

The signal is prepared for driving composite video to an external monitor or printer. It consists of the following lines:

- Video Sync and Ext. Video GND.
- Composite Video and Ext. Video GND

A BNC connector for composite video input is included.The external video input is multiplexed with the internal video input.

2.14.2 HC Video signals

The signal is prepared for driving RGBS video signals to an external monitor or printer. It consists of the following lines:

- Red line and Ext. Video GND
- Green line and Ext. Video GND
- Blue line and Ext. Video GND
- Video Sync and Ext. Video GND.

2.14.3 S-Video signals

The signals are prepared for driving one external unit.

The S-Video signals consist of the following lines:

- SVHS Luma output and Ext. Video GND.
- SVHS Chroma output and Ext. Video GND.
- SVHS Luma input and Ext. Video GND.
- SVHS Chroma input and Ext. Video GND.

Each output signal is buffered and capable of driving one unit. The external SVH-video inputs are multiplexed with the internal SVHS - video inputs.

2.14.4 SCSI-2 Fast bus

This will be delivered with an internal and external termination from the factory. The external termination is to be mounted on the outside of the system at the rear side. By simply removing this and connecting SCSI devices in a chain, they will be served. The termination must be connected to the last one in the chain.

The output lines will be according the SCSI-2 Fast standard for 8 bits bus.

2.14.5 RS-232 signals

These signals are standard RS-232 running at a maximum 38.400 baud if possible.

- One line for connection to the CPU host signal. For this function we need a separate EPROM set for monitoring the system during fault conditions.
- One line for optional connection to a modem.
- One line TBD. This could either be connected to the GRAPHIC 5 board or to the CPU board.

2.14.6 Ethernet signals

The signals into the I/O board is supported by the CPU. On the I/O board, the signals are converted to a Thin-Wire Ethernet (BNC/RG58) coaxial cable (old systems) or to AUI on newer systems. See Fig. 2.2 Ethernet connection alternatives.

2.14.7 Digital signals

The signals are prepared for the following input output:

- 3 input-lines and GND for Foot switch connection. This signal will be decoded on the I/O board.
- Output of a 5V signal trigger pulse.

2.14.8 Analog Signals

There will be 4 inputs on the External I/O module.

All the analog signals will be A/D converted on the External I/O board, and scaled before they are transferred to the SDP board.

Empty page.

External I/O board

3 Introduction

3.1 Abstract

This document is a description of the External I/O board (EXT I/O) in System 5. The board performs buffering and galvanic isolation (not in the first version) of the signals present on the External I/O Connector Panel.

3.2 Document History

Rev	Date	Sign	Description
01	11 Aug 1994	GRL	First version of document
02	20 Apr 1995	GRL	Changes to Etherner interface

Table 1: Revision control.

Macintosh HD:User:James:@:iarb:Service:S5_ServiceMan:S5_serv_files:A6_03_External.02.
Printed: December 5, 2000.

3.3 Definitions/Abbreviations/Nomenclature

In the following the various I/O signals are divided into groups. The following definitions are used:

Internal I/O: All signal used of peripherals mounted in the system with power from internal isolation transformer.

External I/O: All signals made available to the user at the outside of the system. These signals are galvanically isolated to take care of patient safety.

EMC: Electro Magnetic Compatibility.

I/O: Input/Output signals.

SDP: Spectrum Doppler Processor Board

DSP: Digital Signal Processor

ECG: Echo Cardio Gram

3.4 References

External I/O Block Diagram – rev. 02 on page B2-21.

4 Descriptions

4.1 Video out

The composite video signal is buffered and capable of driving several devices like monitors and printers. It consists of the following lines:

- Video Sync and Ext Video GND.
- Composite Video and Ext Video GND

4.2 Video in

A composite video signal from an external source can be input to the system The signal is routed directly through to the Internal I/O board.

4.3 RGB out

The signal is prepared for driving RGBS video signals to an external monitor or printer. It consists of the following lines:

- Red line and Ext Video GND
- Green line and Ext Video GND
- Blue line and Ext Video GND
- Video Sync and Ext Video GND.

The signals are buffered and capable of driving one unit.

4.4 S-Video out

The signals are prepared for driving one external unit. The S-Video signals consist of the following lines:

- SVHS Luma output and Ext Video GND.
- SVHS Chroma output and Ext Video GND.
- SVHS Luma input and Ext Video GND.
- SVHS Chroma input and Ext Video GND.

4.5 S-Video in

The signals may come from an external device like a VCR or a color printer. They are routed directly to a multiplexer on the Internal I/O board. The S-Video signals consist of the following lines:

- SVHS Luma output and Ext Video GND.
- SVHS Chroma output and Ext Video GND.
- SVHS Luma input and Ext Video GND.
- SVHS Chroma input and Ext Video GND.

4.6 SCSI-2 interface

(Not installed on first version of board).

The SCSI Interface will be delivered with an internal and external termination from the factory. The external termination is to be mounted on the outside of the system at the rear side. By simply removing this and connecting SCSI devices in a chain, they will be served. The termination must be connected to the last one in the chain.

The number of SCSI devices is limited to 8.

- Internal devices:
  - CPU board.
  - Flexi Disk drive.

- Hard Disk drive.
- Optical Disk drive.
- (Optional High Performance printers i.e. SONY D7000 SCSI printer.)

• External devices:
  - Due to the 4 (5) internal SCSI-2 Fast devices the amount of external devices will be limited to a number of 4 (3) units.

The output lines will be according the SCSI-2 Fast standard for 8 bits bus.

4.7 RS-232 interface

These signals are standard RS-232 running at a maximum of 38.400 baud.

- One line for connection to the CPU host signal. For this function we need a separate EPROM set for monitoring the system during fault conditions.
- One line for optional connection to a modem.
- One line TBD. This could either be connected to the GRAPHIC 5 board or to the CPU board.

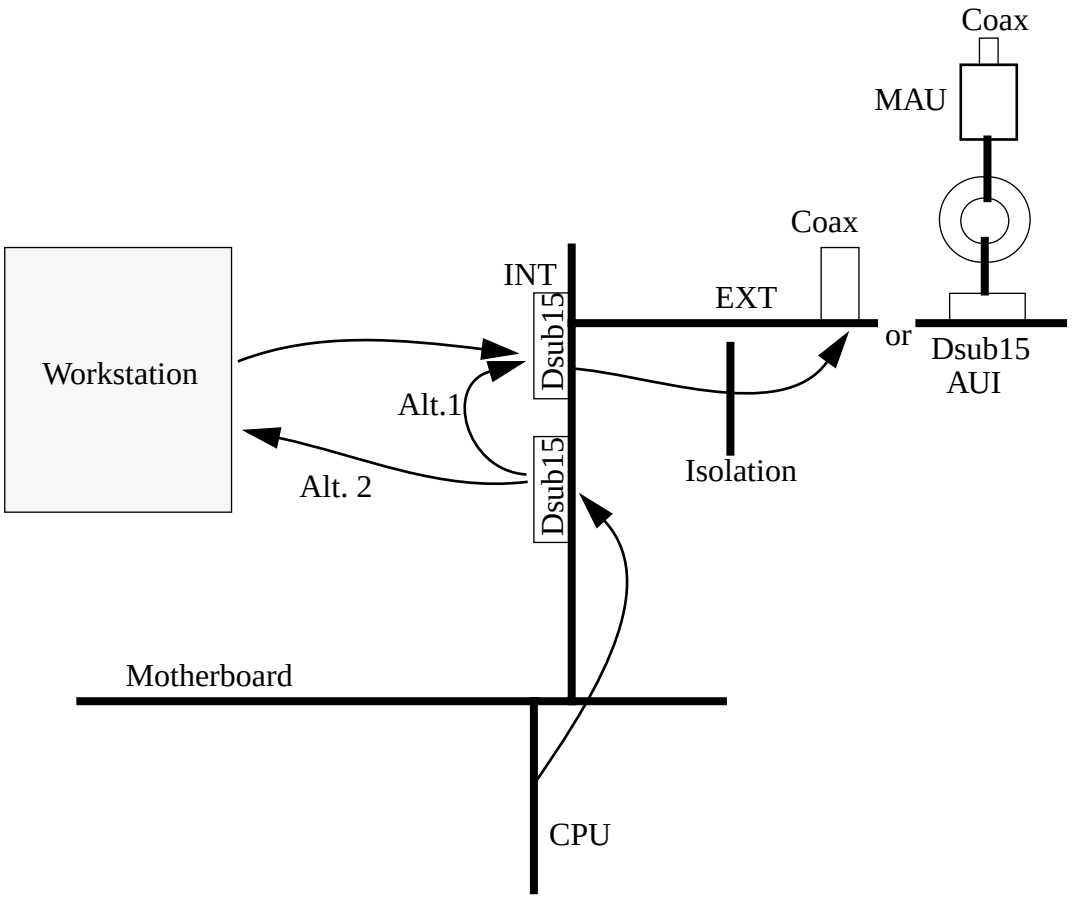
4.8 Ethernet interface

The signals into the I/O board are provided by the CPU. The Ethernet signals from the system CPU are looped through the Internal I/O board before routed to the External I/O board. On the first systems (~15), the signals are fed to a Coaxial Transceiver Interface (CTI), and then to a BNC. This interface is designed for thinwire Ethernet only, and can not be used with thickwire or twisted pair.

On the newer systems, the ethernet signals are fed to a 15 pin D-connector (the Attachment Unit Interface - AUI) on the External I/O panel. This allows for connection of all types of Ethernet to the system; one has to use the correct Medium Attachment Unit (MAU). Thus, there will be a cable from the 15 pin D-connector on the I/O panel to a similar connector on the MAU. To minimize interference from the Ethernet connection, this cable should be looped through a ferrite a few turns.

The Ethernet connection is made to the other end of the MAU.

Fig. 4.1 Ethernet connection alternatives



The application, protocols and necessary isolation voltage is not yet determined.

4.9 Trigger output

A software defined trigger signal (TTL level), e.g. an ECG trigger, is output on a BNC connector. The signal is generated by the DSP on the Internal I/O board.

4.10 Analog inputs

4 analog signal can be input on the External I/O board. They are buffered and fed to a multiplexing A/D converter with a serial interface with the DSP on the Internal I/O board. After processing in the DSP, the SDP board can fetch the data so that they can be displayed as traces on the monitor.

The Peripheral Modules

Overview

Introduction

This part of the SYSTEM FiVE Service Manual lists the Peripherals that may be connected to the scanner.

The content in this part of the manual

The content in this part of the manual:

Module / subsystem	Page
Peripherals – rev. 03	A7-2
Monitors – rev. 01	A7-3
VCRs, Video Recorders – rev. 02	A7-4
S5 - EchoPAC Transfer Kit – rev. 02	A7-6
Footswitch – rev. 01	A7-7
BW Printer – rev. 03	A7-8
Color Printer – rev. 02	A7-10

Macintosh HD:User James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_01_Periph_Innh.03.
Printed: December 5, 2000.

Peripherals – rev. 03

1 Introduction

1.1 Abstract

System FiVe is a platform for a variety of applications. The different applications needs different peripherals or combination of these.

This document describes the legal peripherals for System FiVe and their configurations.

1.2 Document History

Rev	Date	Sign	Description
01	28 Aug 1997	LHS	First Edition
02	6 Apr 1998	JE/lhs	Updated Configuration Matrix
03	21 Oct. 1999	LHS	Updated pr. sw. 1.7.1/1.8 release. Removed the Configuration matrix (it's a manufacturing document). Added new chapter; Monitor.

Table 1: Revision control.

1.3 Definitions/Abbreviations/Nomenclature

PAL - Color television standard used in most of Europe and in some other countries.

NTSC - Color television standard used in USA, Japan and in some other countries.

1.4 References

Spare Parts – 02, see Chapter O

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_02_Peripher.03.
Printed: December 5, 2000.

Monitors – rev. 01

1 Introduction

1.1 Abstract

This document describes the Video Monitor types that have been used on System FiVe.

1.2 Document History

Rev	Date	Sign	Description
01	26. Oct. 1999	LHS	Initial version

1.3 Definitions/Abbreviations/Nomenclature

1.4 References

- Monitor Setup Procedure on page K04-1
- Monitor Setup Procedure, (from sw. 1.5 and up) on page K04-2
- Monitor Replacement Procedure - rev. 01 on page L1-17
- Peripheral and MAC Devices on page O1-6

2 Descriptions

2.1 EIZO TX-C7 - 17“

- Video System: VGA (1024 x 768)
- Mains Voltage: 110 VAC

2.2 EIZO T57S - 17“

- Video system: VGA
- Mains Voltage: 220 VAC

2.3 EIZO 562 - 17”

- Video system: VGA
- Mains Voltage: 220 VAC
- (Used on old systems)

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_025_Monitor.01.
Printed: December 5, 2000.

VCRs, Video Recorders – rev. 02

1 Introduction

1.1 Abstract

This document describes the VCRs that may be installed in System FiVe.

1.2 Document History

Rev	Date	Sign	Description
01	6 Apr 1998	LHS	Initial description
02	21. Oct. 1999	LHS	Updated per sw.1.7.1/1.8 release.

Table 1: Revision control.

1.3 Definitions/Abbreviations/Nomenclature

NTSC - Color television standard used in USA, Japan and in some other countries.

PAL - Color television standard used in Europe and in some other countries.

1.4 References

- VCR Related Problems on page K03-11
- Installation Procedure, Sony SVO-9500MDP2 PAL, GEVU PN: FB194012
- Installation Procedure, Sony SVO-9500MD2 NTSC, GEVU PN: FB194013

2 Descriptions

2.1 Sony SVO-9500MD2/SVO-9500MDP2

These VCRs are available in both PAL and NTSC versions.

- SVO-9500MDP2: PAL
- SVO-9500MD2: NTSC

2.2 Panasonic MD830

The MD830 VCRs are also available in both PAL and NTSC versions.

These VCRs are used on some System FiVe systems, and they are usually mounted on the system's left side.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_03_VCR.02.
Printed: December 5, 2000.

2.3 Panasonic AG7350 p/AG7350 n

AG 7350 p is the PAL version and AG7350 n is the NTSC version.

The AG7350 VCRs are used on earlier System FiVe systems, – the tall models (“Tall Boys”).

An AG7350 VCR mounted in a System FiVe is shown in this picture (see the arrow).

S5 - EchoPAC Transfer Kit – rev. 02

1 Introduction

1.1 Abstract

This document gives a brief overview of the System FiVe - EchoPAC Transfer Kit.

1.2 Document History

Rev	Date	Sign	Description
01	21.Apr.1998	LHS	Initial version
02	29.Oct. 1999	LHS	Updated.

Table 1: Revision control.

1.3 Definitions/Abbreviations/Nomenclature

1.4 References

Wiring Diagram S5-EchoPAC Transfer Kit – rev. A on *page C1-6*.

Wiring Diagram Internal Cable Harness – rev. E on *page C1-2 (internal EchoPAC)*

2 IDescriptions

A Transfer Kit is used for downloading data from the System FiVe scanner to a Stand Alone Macintosh or compatible, running the EchoPAC™ application.

The installation of EchoPAC is described in the EchoPAC Installation Manual (see the references above).

A wiring diagram for the S5-EchoPAC Transfer Kit – rev. A, is included on *page C1-6* in this Service Manual.

Macintosh HD:User:James:@:-ant:Service:S5_ServiceMan:S5_serv_files:A7_04_EP_S5_Tmsfr_K.02.

Footswitch

1 Introduction

1.1 Abstract

This description is a brief description of the footswitch on System FiVe.

1.2 Document History

Rev	Date	Sign	Description
01	31.03.1998	LHS	Initial version

Table 1: Revision control.

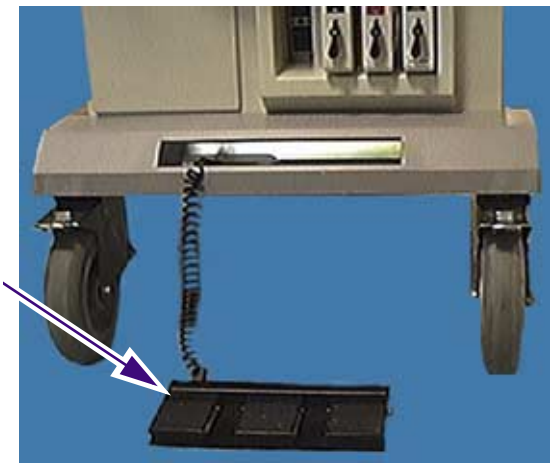
1.3 Definitions/Abbreviations/Nomenclature

1.4 References

Footswitch Interface on page A6-4.

Display, Control and I/O – rev. 09 on page B1-4.

2 Descriptions



The Footswitch is connected to the Internal I/O where the Footswitch signals are routed to the Footswitch Interface/Patient I/O interface.

There are three switches on the Footswitch.

The Footswitch functionality is selected in software.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_05_Footswitch.
Printed: December 5, 2000.

BW Printer – rev. 03

1 Introduction

1.1 Abstract

This description is a brief description of the black and white (BW) printers used in System FiVe.

1.2 Document History

Rev	Date	Sign	Description
01	6 Apr 1998	LHS	Initial document release.
02	2. Nov. 1999	LHS	Updated
03	8. Dec. 1999	LHS	Updated (new printer)

Table 1: Revision control.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A7_06_BW_Printer.03. Printed: December 5, 2000.

1.3 Definitions/Abbreviations/Nomenclature

BW – Black and white

1.4 References

Keyboard, I/O and Peripherals on page A1-55

I/O - rev. 02, on page B1-8

Internal I/O Subassembly - rev. A on *page D-6*

I/O Signals - 05 starting on *page F-3*

Spare Parts – rev. 13 on page O1-3.

Installation Procedure, Video Printer, b/w, Sony UP890MDG, GEVU PN: FB194016

2 Descriptions

The SONY UP890 printers are used both on NTSC and PAL System FiVe systems.

Note:

Before May 1999:

There are different GE Vingmed Part Numbers for the NTSC and the PAL version of the printer, so please check for the correct GE Vingmed Part Number before ordering, see the Spare Parts – rev. 13 on page O1-3.

After May 1999:

The Sony video printer UP-890 MDG Supports both NTSC and PAL, and both 120 VAC and 220-240 VAC 50/60 Hz.

The SONY UP890 printer is connected to *Video Out* and *Rem Cntrl* on the Internal I/O. See Internal I/O without PosDet and PAMPTE support on page F-12 for more info.

Color Printer – rev. 02

1 Introduction

1.1 Abstract

This is a brief description of the color printers used in System FiVe.

1.2 Document History

Rev	Date	Sign	Description
01	7. Apr. 1998	LHS	Initial document release.
02	2. Nov. 1999	LHS	Updated contents

Table 1: Revision control.

1.3 Definitions/Abbreviations/Nomenclature

1.4 References

Keyboard, I/O and Peripherals on page A1-55

I/O - rev. 02, on page B1-8

Internal I/O Subassembly - rev. A, on *page D-6*

I/O Signals - 05, starting on *page F-3*

2 Descriptions

- SONY UP2950MD printers are used for both PAL and NTSC.
- SONY UP2800P printers is used only on PAL System FiVe systems.
- SONY UP1800 printers have been used on both NTSC and PAL System FiVe systems.
- SONY UP1950 printers have been used only on NTSC System FiVe systems.
- Epson Stylus Color 740 Stand Alone printers may be used both for PAL and NTSC systems.

Note: There are different GE Vingmed Part Numbers for the NTSC and the PAL versions of the printers, so please check for the correct GE Vingmed Part Number before ordering, see “Spare Parts – rev. 13” on page O1-3.

The color printers are connected to the RGBS OUT outlet on the Internal I/O, see the drawing on page F-12.

Macintosh HD:User:James:@+arb:Service:S5_ServiceMan:S5_serv_files:A7_07_Color_Printer.02.
Printed: December 5, 2000.

The Power Modules

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes the Power modules in the instrument.

Modules and sub-systems described in this part of the manual

The listed modules and subsystems in this part of the manual:

Chapter	Module / subsystem	Page
1 - 4	AC Controller - rev.02	A8-2
5 - 8	Temperature Sense Board - rev.01	A8-4
9 - 12	DC Power Module - rev.03	A8-6
13 - 16	DC Power Extention Board - rev.01	A8-9
17 - 20	High Voltage Power Supply - rev.02	A8-11

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A8_01_Power_innh.02.
Printed: December 5, 2000.

AC Controller

1 Overview

1.1 Abstract

This document describes the AC Controller.The AC Controller take care of Power distribution, Power control and system fan regulation.

1.2 Document History

Table 1: Document History

Revision	Date	By	Description
01	09.08.94	L. H. Semb	Initial release
02	14.07.95	L. H. Semb	Added references

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A8_02_AC_P_Cont.
Printed: December 5, 2000.

1.3 Definitions/Abbreviations/Nomenclature

AC: Alternating Current

RPM: Rotations Pr. Minute.

1.4 References

AC Power Block Diagram – rev. 02 on page B2-22.

2 Inputs

The input voltages to the module are: 12VAC, 115VAC and 230VAC.

Signal	Description	Source	Level
TEMPIN	Temp sensor input	Temp Sense board	Analog
HITEMPIN	High temperature warning	Temp Sense board	Digital
ONOFSW_L	ON/OFF (Standby) control	Remote switch	Digital - TTL

3 General Description

3.1 AC CONTROLLER

3.1.1 Power Control and Distribution

The AC CONTROLLER module is used for power control and distribution of 115 and 230V mains voltages. The internal logic controls the relays according to the input signal from the remote switch and the VME master.

The 115 and 230 V are used as system power to the DC power (Card Rack), the monitor and peripherals.

3.1.2 Airflow Control

The AC CONTROLLER module also includes a thermal fan speed regulation for optimal air flow through the card rack.

The 12V input is used for the fans.

The fan regulation is based on linear regulation, continuously regulating the fan RPM from 40% at + 15°C to 100% at 60°C air temperature, measured on top of the card rack.

3.1.3 High Temperature Warnings, and System Shut Down

An alarm output signal will go active under certain conditions:

- Temperature above 60°C.
- Temp. sensor malfunctions, (short circuit).

The AC CONTROLLER module does also include a high temperature warning and system shut down in case of harmful high temperature >70°C.

3.1.4 Remote Control

Relays are switched on and off by pressing the remote power switch.

The green LED lit when the relays are in ON position and the yellow LED lit in OFF (stand-by) position.

4 Outputs

The output signals from the AC Controller is shown in the table below.

Table 2: Outputs from the AC Controller.

Signal	Description	Destination	Level
LEDPWR	LED power, current limited	IV/DP/STBY	+5V
ONLED_L	ON LED drive	IV/DP/STBY	TTL
STBLED_L	Stand By LED drive	IV/DP/STBY	TTL
POFREQ_L	Power off re. output and grant input	INT I/O	TTL
HITEMP_L	High temperature warning	INT I/O	TTL
RLYCOIL	Relay coil		
RLYDRIVE	Relay drive		
REGOUT	Fan regulator output	Fans	0-12VDC

Temperature Sense Board

5 Overview

5.1 Abstract

This document describes the Temperature Sense Board. The Temperature Sense Board contains an NTC resistor and two temperature fuses.

5.2 Document History

Revi-sion	DATE:	BY:	Description
01	05.08.94	L. H. Semb	Initial release

5.3 Definitions/Abbreviations/Nomenclature

NTC: Negative Temperature Coefficient

Temp: Temperature

Macintosh HD:User-James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A8_03_Temp_Sns.
Printed: December 5, 2000.

6 Inputs

This card is only used for temperature sensing, and has no electrical inputs.

7 General Description

7.1 Overview

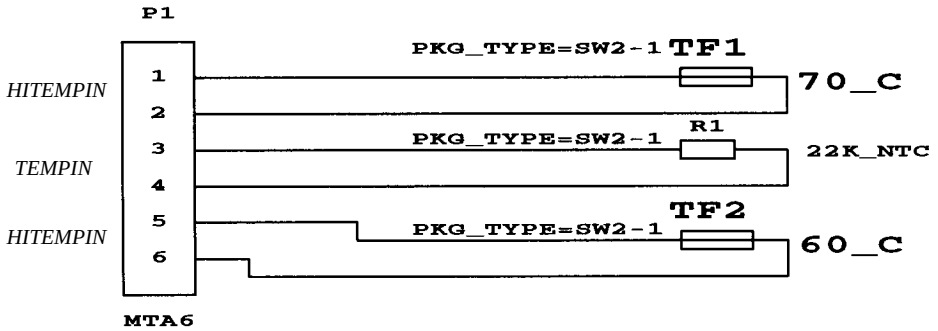


Fig. 7.1 Temp Sense board function diagram

The Temp Sense board contains an NTC resistor, R1, and two temperature fuses, TF1 and TF2.

R1 is sensing the air flow temperature in the card rack. The sense signal is used for controlling the fan speed.

TF1 and TF2 are temperature fuses.

TF1 will break if the temperature is higher than app. 70 °C.

TF2 will break if the temperature is higher than app. 60 °C.

8 Outputs

The outputs from the Temp Sense board are the TEMPIN and the two HITEMPIN signals. They are fed from the P1 connector to the AC Power Controller.

Signal	Description	Destination	Level
TEMPIN	Temperature sensing signal	AC Power Controller	Analog
HITEMPIN	Temperature sensing signal	AC Power Controller	Digital
HITEMPIN	Temperature sensing signal	AC Power Controller	Digital

DC Power Module

9 Overview

9.1 Abstract

This document describes the DC Power module. The DC Power module generates all DC voltages required in SYSTEM FIVE , except the high voltages for the transmitter, the fan power regulator and the AC Controller.

9.2 Document History

Table 3: Document History

Revi-sion	Date	By	Description
01	11.08.94	L. H. Semb	Initial release
02	14.07.95	L. H. Semb	Added references
03	06.11.95	L. H. Semb	Added output description, updated table 4.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A8_04_DC_Pwr.03.
Printed: December 5, 2000.

9.3 Definitions/Abbreviations/Nomenclature

AC: Alternating Current

DC: Direct Current

9.4 References

DC Power Supply Block Diagram – rev. 02 on page B2-23.

DC Power Replacement Procedure - rev. 01 on page L-5.

10 Inputs

Table 4: Input signals to the DC power

Signal	Description	Source	Level
230 V AC	AC input voltage	AC Power Supply	230 V AC (184 — 264 VAC / 47 — 63 Hz)

11 General Description

11.1 Overview

The DC Power module is shown in the figure below (Fig. 11.1).

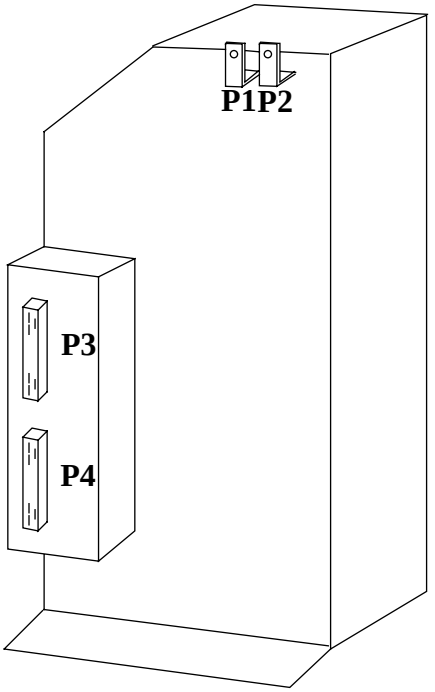


Fig. 11.1 The DC Power module

The DC Power module generates all DC voltages required in SYSTEM FIVE, except the high voltages for the transmitter, the fan power regulator and the AC Controller.

230 VAC is fed from the AC Power to the DC Power module's input. Inside the DC Power module, the 230 VAC is filtered, rectified and converted to the respective output voltages through three switched power converters.

The output voltages are galvanic separated from the input voltage.

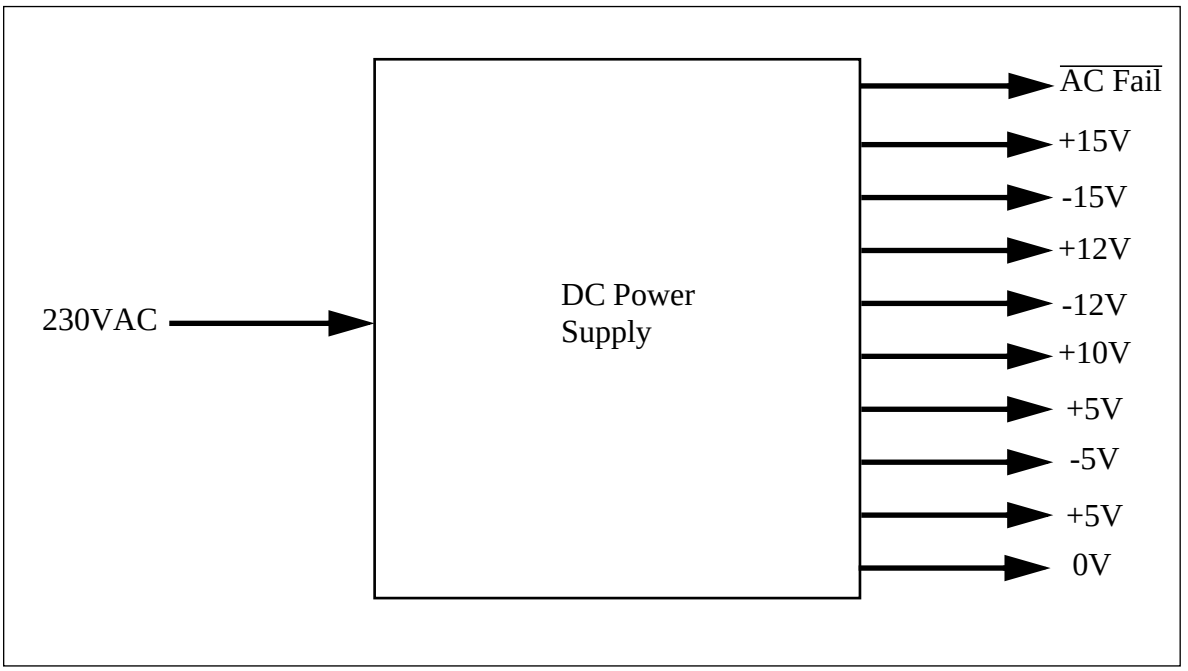


Fig. 11.2 DC Power supply Block Diagram

12 Outputs

12.1 AC Fail

This signal will be active low when the input is below 184 VAC. During normal operation (System Five turned on) this signal will be high (+ 5V). The AC Fail signal is connected via the DC Power Extention board to the VME bus on the Mother board.

12.2 Power Supply Connectors:

P1 and P2: Copper bars with screw fixing. These two terminals are fixed to the Current Rails by allen screws.

P3 and P4: H15 male.

Connector layout:

P1: +5V(d)
P2: GND(d)

Table 5: Connector layout P3 and P4

Pin	P3	P4
4	15/4A+	5/15A+
6	15/4A-	5/15A+
8	15/3A+	5/15A-
10	15/3A-	5/15A-
12	12/4A+	10/3A+
14	12/4A-	10/3A-
16	12/1A+	5/25A+
18	12/1A-	5/25A+
20	0V (ACFAIL)	5/25A+
22	nc	5/25A+
24	ACFAIL	5/25A-
26	nc	5/25A-
28	nc	5/25A-
30	nc	5/25A-
32	nc	nc

DC Power Extention Board

13 Overview

13.1 Abstract

This document describes the DC Power Extention board. On this board, all the DC voltages from the P3 and P4 on the DC Power module are filtered. Diodes ensures that the voltages are “coming up” correctly.

The AC Fail signal is routed from the DC Power module to the VME bus.

13.2 Document History

Table 6: Document History

Revi-sion	Date	By	Description
01	07.11.95	L. H. Semb	Initial release

13.3 Definitions/Abbreviations/Nomenclature

DC: Direct Current

13.4 References

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:A8_05_DC_Ext01.
Printed: December 5, 2000.

14 Inputs

- The DC voltages from P3 and P4 on the DC Power module
- The AC Fail signal from P3 on the DC Power module

15 General Description

15.1 Overview

All the DC voltages are filtered by use of five line filters and 14 discrete capasitors. Seven diodes are used to ensure that the voltages are “coming up” correctly when the power is turned on.

The AC Fail signal from the DC Power module is routed to the VME bus.

16 Outputs

- Filtered DC voltages to the Mother board
- The AC Fail signal to the VME bus

High Voltage Power Supply

17 Overview

17.1 Abstract

This document is a description of the High Voltage Power Supply (HVPWR) in System 5. This module provide digitally controlled supply voltages to the transmitters in the front end.

It also provides +/- 80V power supply for the linear array probe multiplexers.

17.2 Document History

Rev.	Date	Sign.	Description
01	9 Aug. 94	GRL	First version of document
02	22 Sept. 95	GRL	Added info on output power protection

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:A8_06_HV_Power.02.
Printed: December 5, 2000.

17.3 Definitions/Abbreviations/Nomenclature

FEC: Front End Controller board

CW: Continuous Wave (Doppler)

17.4 References

High Voltage Power Supply Block Diagram – rev. 02 on page B2-24

18 Inputs

1. High Voltage Control: One serial data line (HVS_SDA, P2-A3) and several strobe and clock lines from the FEC board.
2. High Voltage Disable: HVDIS_L, which is an open collector signal which can be activated both by the HVPWR and by the FEC.
3. Mains Voltage: 230 VAC.

19 Description

19.1 General Description

The module consists of three linear power supplies: one supply is designed to generate symmetrical output voltages from 0 V up to ± 80 V (High voltage supply 1), one supply is designed to generate symmetrical voltages from 0 V up to ± 40 V (High voltage supply 2) and one supply provides +/- 80V (PMX_80V) for the multiplexers in the probe connectors.for the linear probes.

The mains input circuit consists of a step down transformer and full wave rectifiers for generation of the 55 VDC voltage and the 110 VDC voltage to the output regulators; HV1 and HV2.

In order to minimize excessive regulator heat dissipation in CW mode, the transformer include two 10V windings. When HV2 output voltage decrease below 6V, a comparator controls a relay for selection of 7V transformer outputs.

The output voltages are controlled by two serial 11 bit interfaces from the FEC board, one for each output, in order to program each output individually.

The output currents are sensed through shunt resistors and converted to 0 to + 3.75 V voltages that can be read externally.

The output voltages are converted to 0 to + 4 V voltages that can be read externally.

The output voltages and currents can be monitored by the FEC board for transmit power calculation.

19.2 Output Power Protection

A power surveillance circuit senses the output voltage and current and calculates the power fed to the Front End transmitter boards.

If a preset limit is exceeded, this circuit will switch off all outputs and set HVDIS_L low. This signal (TTL, OC) is sensed by the Front End Controller module, and if active, the FEC module will switch off HV1 and HV2 outputs. The HV output may be disabled by storing $000 in the DAC register, or by set setting the HVDIS_L line low.

The HVDIS_L signal is bidirectional and, if set low from an other external source e.g. the PRC module (over-temperature sensing in a TEE probe), the HV1 and 2 outputs are switched off.

The FEC module should send an alarm to console for warning and allow for probe or cable replacement if no hardware errors are detected.

A watch-dog circuit is implemented in the sense that the FEC board continuously has to pulse the SDA line in order for the HVDIS_L line to be high.

20 Outputs

1. High Voltage outputs (HV1P, HV1N, HV2P, HV2N): These are DC voltages fed to the transmitters in the front end.
2. Probe Mux power outputs (PMX80P, PMX80N): +/- 80V DC voltages fed to the multiplexers in the probe connectors for the 192 element linear probes.
3. High Voltage sense lines (HV I and HV V) for both HV1 and HV2. These signals are low level voltages fed to the FEC board for surveillance of the output power to the probes.

SYSTEM FIVE Block Diagrams

Overview

Introduction

This page shows you the three main parts in the Block Diagrams section.

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
Block Diagrams – Complete	B1-1
Block Diagrams – Boards	B2-1
Block Diagrams	B3-1

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:B0_01_innh_02.fm.
Printed: December 5, 2000.

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SYSTEM FIVE Block Diagrams – Complete

Overview

Introduction

This part of the Service Manual holds the block diagrams for SYSTEM FIVE .

Table of Contents

This table gives you an overview for this part of the Service Manual:

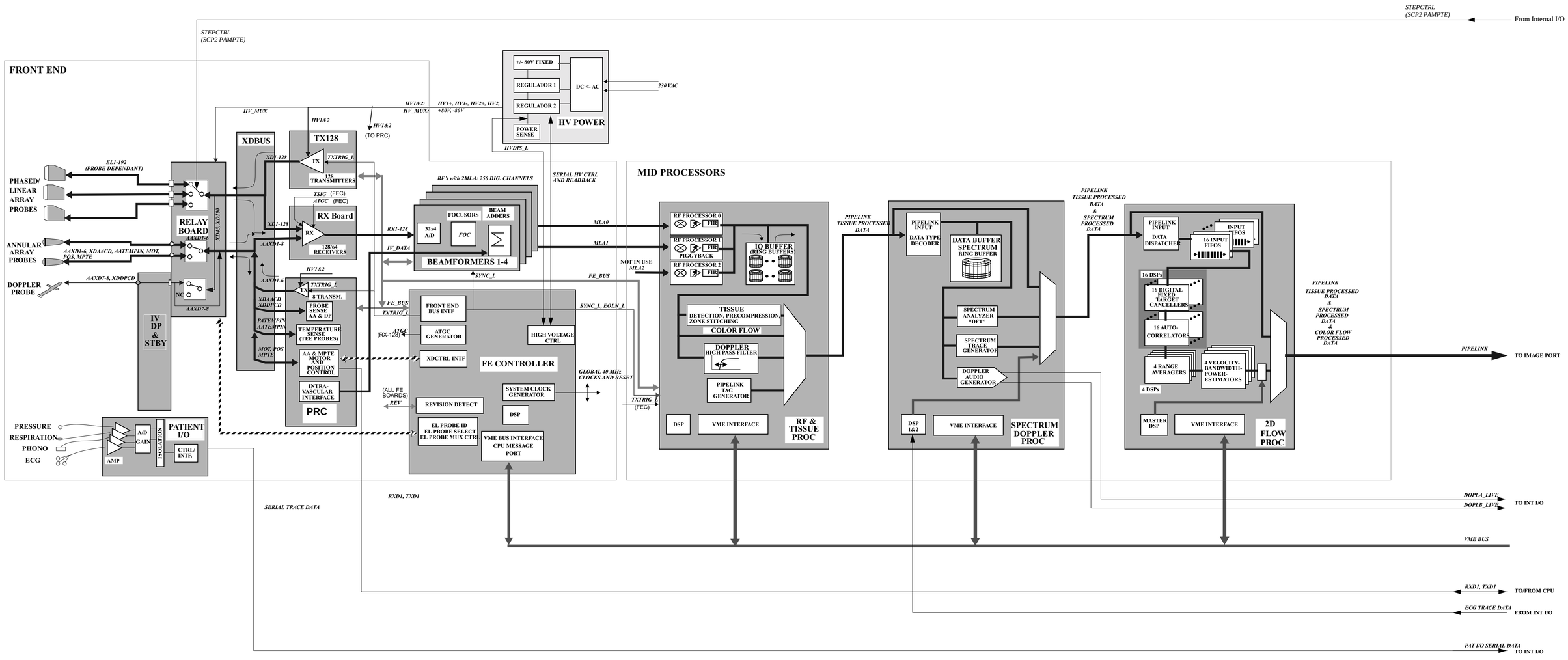
Contents	Page
Front End and Mid., rev. 10	B1-3
Display, Control and I/O – rev. 09	B1-4
Display, Control and I/O – rev. 09	B1-4.1
Front End – rev. 04	B1-5
MID Processor - rev.02	B1-6
Display – rev. 02	B1-7
I/O - rev. 02	B1-8

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:B1_01_Innh.02.
Printed: December 5, 2000.

Your Notes:.

Front End and Mid., rev. 10

System FiVe Block Schematic, Complete, Page 1 of 3



DESIGNER GRL	DATE 19/11-98	SIGN	MODULE SYSTEM (DATAFLOW & CONTROL)	System FiVe
CHECHED	DATE	SIGN	DRAWING NUMBER 330 FA299050	REV 10
APPROVED	DATE	SIGN		
FILE			TYPE OF DOCUMENT BLOCK DIAGRAM	SHEET 1 OF 3

Macintosh HD:User Jannes:@ Work:Service DS_Service:Arch DS_Vers_Rev:FA3_02_comp2_level.15
Printed: 19 November, 1998

Display, Control and I/O – rev. 09

System FiVe Block Schematic, Complete, Page 2 of 3

DESIGNER GRL	DATE 19/11-98	SIGN	MODULE SYSTEM (DATAFLOW & CONTROL)	System FiVe
CHECHED KK	DATE	SIGN		
APPROVED KB	DATE	SIGN	DRAWING NUMBER FA299050	REV 10
FILE			TYPE OF DOCUMENT BLOCK DIAGRAM	SHEET 2 OF 3

3 Display, Control and I/O – rev. 09

Supervision with Integrated Mac and RGB/S-VHS Switch Boxes

System FiVe Block Schematic, Complete, Page 3 of 3

TO PRC (XDCTRL) ← RXD1, TXD1

FROM SDP — DOPLA_LIVE

FROM SDP — DOPLB_LIVE

VME BUS

IMAGE PORT
- VME INTERFACE
- MUXES
- FIFOs
- CONTROLLER
- MUXES
- PIPELINK DATA TYPE DECODER/ DISPATCHER
- A/D (LUMA)
- A/D (CHROMA)
- LUMA/CHROMA DECODER (PAL/NSTC)

PIPELINK

VIDEO

S-VHS

MEMORY
- VME INTERFACE
- IMAGE BUFFER (32 MBYTE) (RING BUFFERS)

SCAN CONVERTER
- VME INTERFACE
- RECURSIVE FILTERING/ CFM ENCODING
- TIME DOMAIN PROC.
- SCAN CONVERSION
- A B C
- X,Y -> R, TH ADDRESS GENERATOR
- Tissue, CFM f, CFM bw
- SPACE DOMAIN PROC.
- TISSUE ENCODER COMPRESSION REJECT
- COLOR ENCODER
- PIXEL MUX AND ARBITER
- FIFO
- PIXEL ADDRESS
- MUX

PIXEL BUS

GRAPH
- RS-232 FP INTF.
- VME INTERFACE
- PIXEL PORT
- BRIDGE
- MUX
- TEXT
- VRAM
- VRAM
- VRAM
- VRAM
- IM. DATA
- IM. DATA
- TEXT
- RAMDAC
- RAMDAC
- VIDEO
- R G B

CPU
- VME CONTROLLER
- RS232 XDCTRL INTF.
- uP 68040
- 32 MByte DRAM
- SCSI INTF
- SERIAL VCR INTF.
- RS232 INTF.
- ETHERNET INTF.

VME INTF

SCSI INTF — SCSI — HARDDISC

EXTERNAL I/O
- DSP
- A/D — ANALOG INPUTS I-4
- LOOP CABLE (REMOVE IF MAC)
- INT
- EXT
- INTF.
- VIDEO BUFFERING
- VIDEO S-VHS R, G, B and S
- RS232-GR
- RS232-CPU
- TRIG OUT
- ETHERNET
- ETHERNET
- VIDEO IN
- VIDEO OUT
- S-VHS IN
- S-VHS OUT
- RGBS OUT
- RGBS OUT

TRACE DATA TO SDP

ECG FROM PATIENT I/O

PATIENT I/O

PATIENT I/O INTERFACE (FILTERING) (DSP)

VIDEO MUX

S-VHS OUT

EXT S-VHS IN

To Relay Board

STEPCTRL (SCP2 PAMPTE)

IO-PROM

ROT APAPT TV ROT

S-VHS IN

S-VHS IN/OUT

FROM VCR

RS232-GR

INTERNAL I/O

FRONT PANEL INTF.
- RS-232 SYSTEM INTF.
- OPTIONAL VCR REMOTE INTERFACE
- LOCAL uP (6809)
- ROTARY DECODER
- TGC DECODER A/D
- SWITCH DECODER
- DISPLAY DRIVER
- T.B. & TOGGL DECODER (VIA)
- SWITCH MATRIX DECODER
- ROTARY KNOBS
- TGC
- SWITCHES
- TRACKBALL
- GAIN.....REJECT DISPLAY GAIN.....REJECT
- TOGGLE SWITCHES
- QUERTY KEYBOARD

ON/OFF

POWER SWITCH

DC ON/OFF

DC POWER

AC POWER INTERFACE

VME PWR INTERRUPT

VME TEMP INTERRUPT

TO DSP

AC CTRL

AC POWER CONTROLLER
- TEMP CTRL

AC OUTLETS

TEMP/N HITEMP/N

FAN CTRL VOLT.

TEMP SENSOR

INT I/O

Integrating DSP

VIDEO BUFFERS

REMOTE CONTROL (DSP)

VIDEO BUFFERS

TO EXT I/O

RS232-INT2

B/W VIDEO OUT

B/W PRINTER

REM.CTRL n

REM.CTRL n

VIDEO OUT

SVHS OUT

PAL/NTSC RGBS OUT

COLOR PRINTER

REM.CTRL 4

12 Traces (9-rotation, 3-position)

KEYBOARD, I/O & PERIPHERALS

VIDEO S-VHS RGBS

PAL/NTSC

HIGH RES. RGBS

HIGH RES. RGBS

DOPLB_LIVE

DOPLA_LIVE

AUDIO SWITCH
- LIVE
- PLAY

VIDEO BUFFERS

FOOTSWITCH INTERFACE (DSP)

FOOTSW.

FOOTSWITCH

VCR AUDIO B

VCR AUDIO A

SVHS OUT

RS232-CPU

REPLAY A

REPLAY B

FP AUDIO B

FP AUDIO A

ETHERNET

ETHERNET

FRONT PANEL
- AUDIO AMPL.
- SPEAKERS

AUDIO A

AUDIO B

TO EXT

AUX

HUB

LCD

EchoPAC

MAC VIDEO

SERIAL DATA

LASER PRINTER (OPTIONAL)

MAC KEYBOARD

SERIAL

MACRGB

MAC S-VHS OUT

MAC

INTEGRATED ECHOPAC

RGB SWITCHBOX

RGB (BNC)

SYSTEM MONITOR

S-VHS SWITCHBOX

S-VHS OUT

VCR

S-VHS IN

BIRD POSITION SENSOR (OPTIONAL)

BIRD RECEIVER

CONTROL BOX (INSIDE SYSTEM)

RS232

POWER

RECEIVER

FERRITE

FERRITE

BIRD TRANSMITTER

(LOCATED ON PROBE)

On some Systems the Image Port 2 Board replaces the Image Port and Memory Boards

IMAGE PORT-2
- PipeLink Dispatcher
- Video AD Converter & Decoder
- PCI2Vme Bridge
- PipeLink Data FIFOs
- Video Y Data FIFOs
- Video UV Data FIFOs
- 1960RP Processor
- IMAGE MEMORY (16-256 MBYTE) (RING BUFFERS)
- PCI bus

DESIGNER GRL	DATE 19/11-98	SIGN	MODULE SYSTEM (DATAFLOW & CONTROL)	SYSTEM 5
CHECHED KK	DATE	SIGN	DRAWING NUMBER FA299050	REV 10
APPROVED KB	DATE	SIGN	TYPE OF DOCUMENT BLOCK DIAGRAM	SHEET 3 OF 3
FILE				

0 Front End – rev. 04

Macintosh HD:User Jannes @:ant-Service:05_Service\Mac:05_serv_files:B1_04_fe.04.
Printed: December 5, 2000.

REL
RELAYS
SERIAL PROBE ID
PROBE MUX CTRL
RELAYS
CONTROL INTERFACE
REV.
IV, DP & STBY
XDBUS
PHASED/ LINEAR ARRAY PROBES
ANNULAR ARRAY PROBES
DOPPLER PROBE
XD1-128
AAXD1-6, XDAACD, AATEMPIN, MOT, POS, MPTE
AAXD7-8
AAXD7-8, XDDPCD
XD45, XD100
P1/P2
P5
P6
P7
P8
P9
(HV POWER) HV1&2
(FEC) TXTRIG_L
TX-128
CACHE
8 TRANSMIT PULSE GEN. (128 CH.)
128 TRANSMITTERS
FRONT END INTERFACE
REV.
FE_BUS
REV (FEC)
TSIG (FEC)
RX-128
T/R SWITCH
RELAYS
128 PREAMP
128 VC-AMP
P1/P3
P4/P5
ATGC (FEC)
RX1-128
MLA_IN
32 CHANNELS PER BF BOARD
32 A/D CONV.
8 FOCUSORS/MLA
2 BEAM ADDERS/MLA
1 BEAM ADDER/MLA
A/D
F
FOCUSOR
BEAM ADDER LEVEL 2
BEAM ADDER LEVEL 3
MLA0 TO BAL3 ON NEXT
MLA1 TO BAL3 ON NEXT
BF BOARD
FRONT END INTERFACE
CACHE
BF 1-4
MLA0 OUT
MLA1 OUT
(RFT)
HV1&2
(HV POWER)
(HV POWER) HV1&2
(FEC) TXTRIG_L
TRANSMIT PULSE GENERATOR
6 TRANSMITTERS
AAXD1-6
XDAACD XDDPCD
PROBE SENSE AA & DP
PATEMPIN AATEMPIN
TEMPERATURE SENSE (TEE PROBES)
MOT, POS MPTE
AA & MPTE MOTOR AND POSITION CONTROL
FRONT END INTF.
ATGC (FEC)
TSIG (FEC)
RX
FILTER, DETECTOR
A/D
RF_IN
BURST
MOTOR, POSITION, CATH. CODE, HV, ON/OFF
MOTOR/POSITION CONTROL
IV
REV.
PRC
TXTRIG_L (FEC)
REV (FEC)
INTRAVASCULAR CATHETER
MOTOR POD
PATIENT ISOLATED SENSORS
ECG
PHONO
RESPIRATION
PRESSURE
OPTIONAL
PRESSURE
PRESSURE
PRESSURE
PRESSURE
PREAMP MODULE
AMP/FILTER
A/D AND ISOLATION MODULE
A/D with MUX
PATIENT ISOLATION
ISOLATED POWER +/- 5V
DC-DC
UNISO. +5V.
PATIENT I/O
SERIAL DATA
PAR. DATA
CTRL
P503
SYSTEM CLOCK GENERATOR
GLOBAL 40 MHz CLOCKS AND RESET
SYNC_L
TXTRIG_L
FRONT END BUS INTF
VME BUS INTERFACE CPU MESSAGE PORT
VME BUS
(CPU)
(TX-128,PRC) TXTRIG_L
(RX-128,PRC) ATGC
ATGC GENERATOR
(RX-128,PRC) TSIG
TEST SIGNAL GENERATOR
CPU
MEMORY
XDCTRL INTF
(REL) EL PROBE CTRL
EL PROBE ID
EL PROBE SELECT
EL PROBE MUX CTRL
HIGH VOLTAGE CTRL
SERIAL HV CTRL
(HV POWER)
(ALL FE BOARDS) REV
REVISION DETECT
HIGH VOLTAGE READBACK
HV SENSE
FEC
RXD, TXD
(INTERNAL I/O)
PARALLEL INTERFACE

DESIGNER GRL	DATE 17/10-96	SIGN	MODULE SYSTEM 5 (FRONT END)	SYSTEM 5
CHECHED HH	DATE	SIGN	DRAWING NUMBER 330 FA299047	REV 04
APPROVED KB	DATE	SIGN		
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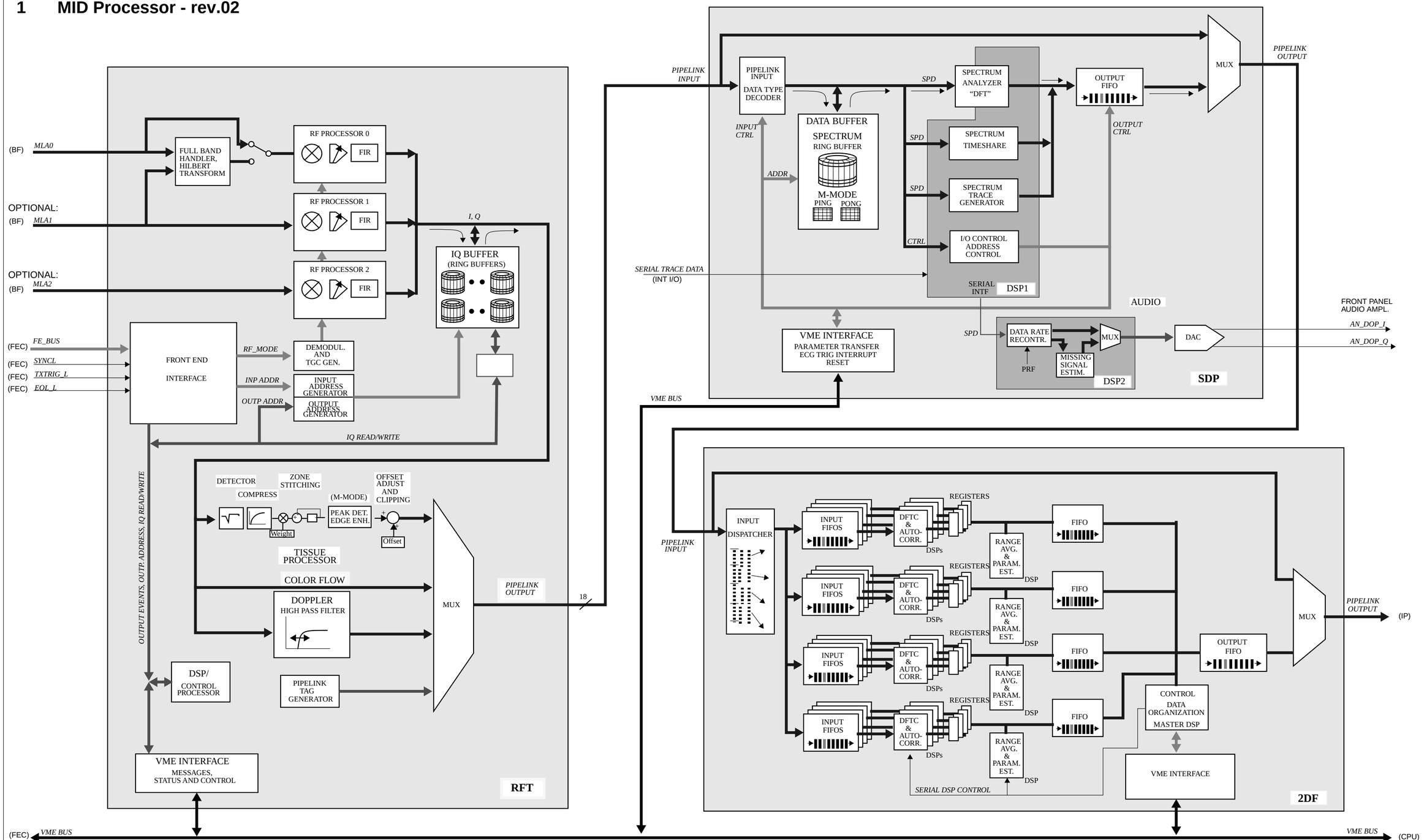
1 MID Processor - rev.02



DESIGNER GRL	DATE 22/11-94	SIGN	MODULE SYSTEM 5 (MID PROCESSORS)	SYSTEM 5
CHECKED MLH	DATE	SIGN	DRAWING NUMBER 330 FA299048	REV 02
APPROVED KB	DATE	SIGN		
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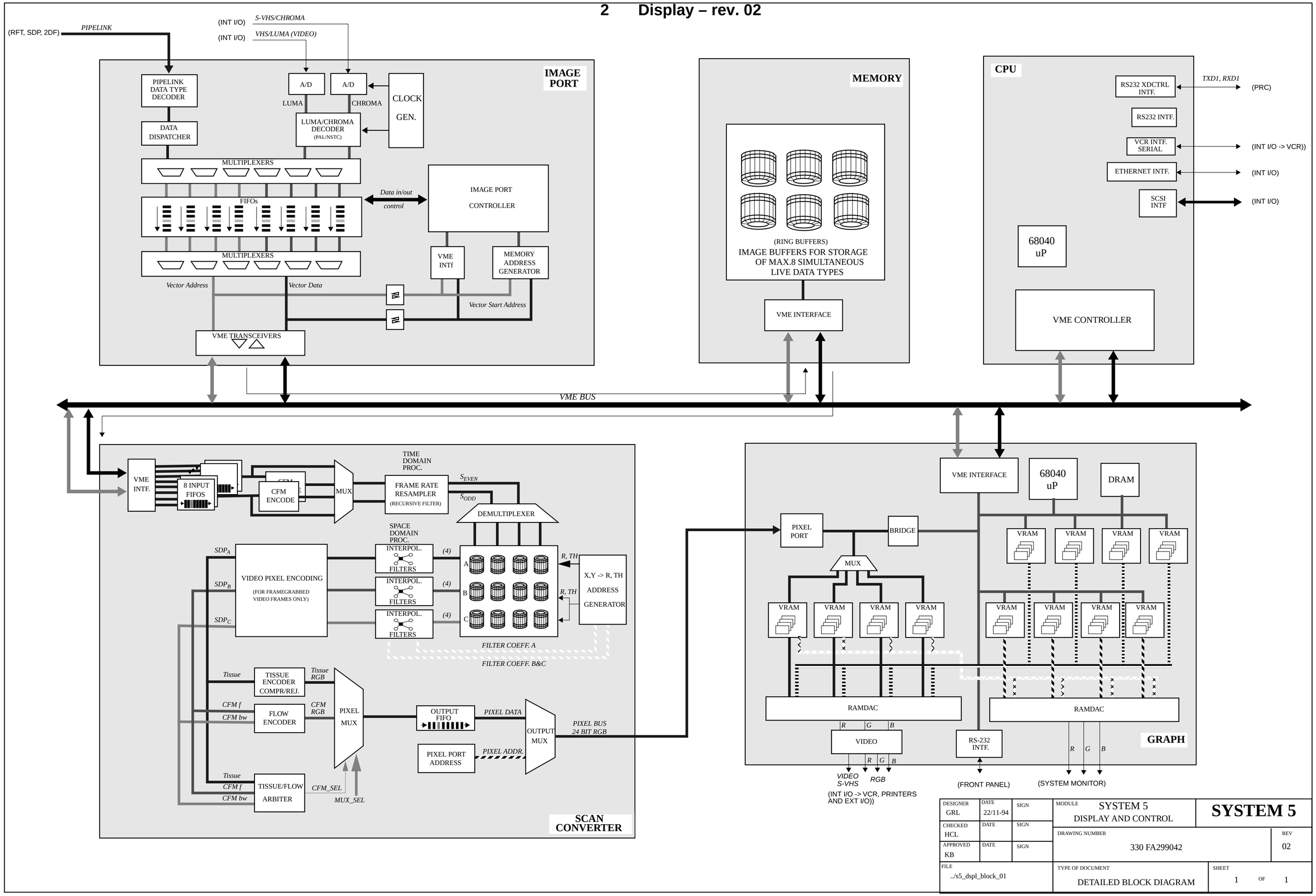
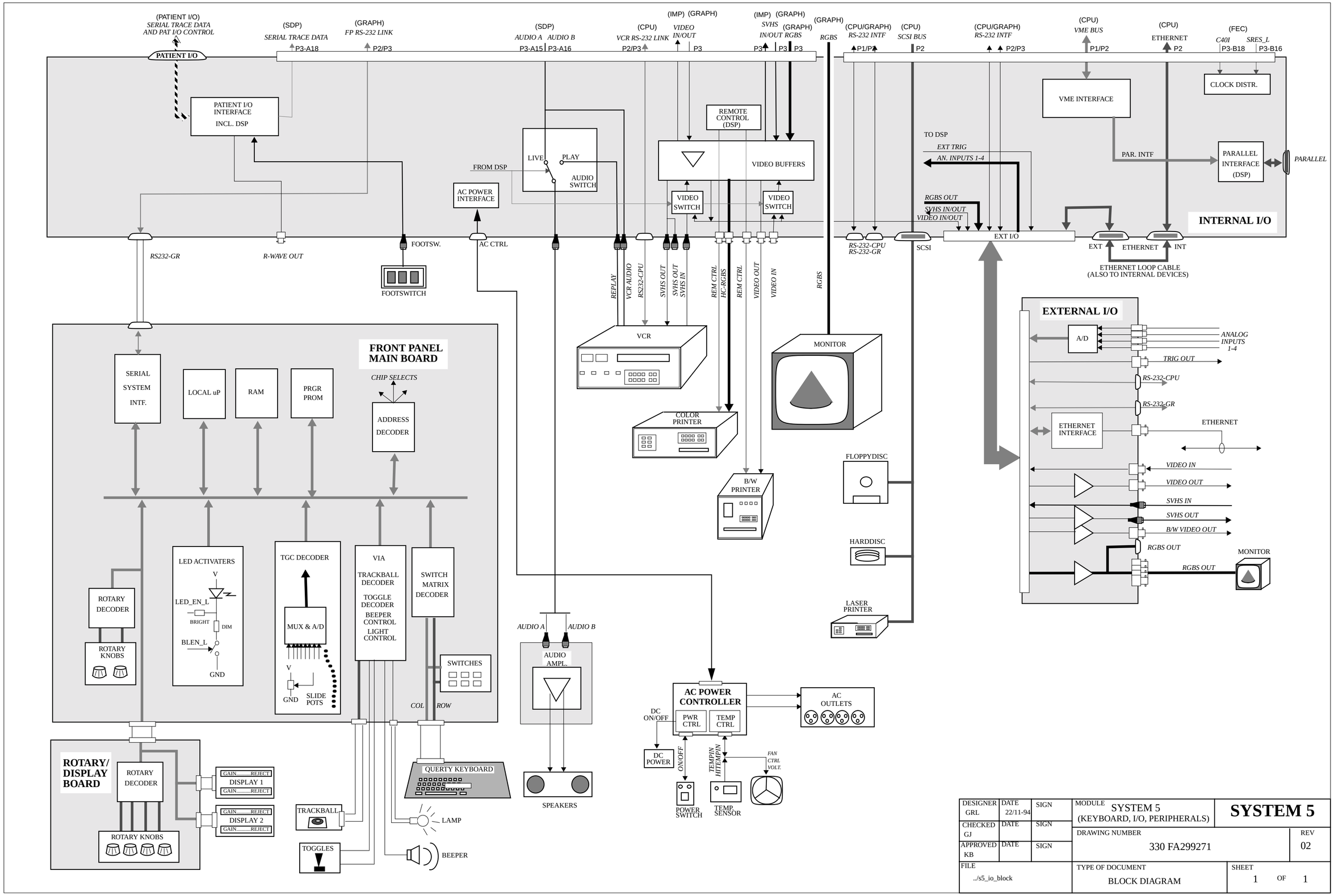
Macintosh HD:User James@hab:Service:S5_ServiceMan:S5_serv_files:B1_05_mid.02.
Printed: December 5, 2000.


2 Display – rev. 02
(RFT, SDP, 2DF)
PIPELINK
(INT I/O)
S-VHS/CHROMA
(INT I/O)
VHS/LUMA (VIDEO)
IMAGE PORT
PIPELINK DATA TYPE DECODER
DATA DISPATCHER
A/D
A/D
LUMA
CHROMA
CLOCK GEN.
LUMA/CHROMA DECODER (PAL/NSTC)
MULTIPLEXERS
FIFOs
Data in/out
control
IMAGE PORT CONTROLLER
MULTIPLEXERS
VME INTf
MEMORY ADDRESS GENERATOR
Vector Address
Vector Data
Vector Start Address
VME TRANSCEIVERS
MEMORY
(RING BUFFERS)
IMAGE BUFFERS FOR STORAGE OF MAX.8 SIMULTANEOUS LIVE DATA TYPES
VME INTERFACE
CPU
RS232 XDCTRL INTF.
TXD1, RXD1
(PRC)
RS232 INTF.
VCR INTF. SERIAL
(INT I/O -> VCR))
ETHERNET INTF.
(INT I/O)
SCSI INTF
(INT I/O)
68040 uP
VME CONTROLLER
VME BUS
VME INTF.
8 INPUT FIFOS
CFM ENCODE
MUX
TIME DOMAIN PROC.
FRAME RATE RESAMPLER (RECURSIVE FILTER)
SEVEN
SODD
DEMULTIPLEXER
SPACE DOMAIN PROC.
INTERPOL. FILTERS
(4)
SDPA
SDPB
SDPC
VIDEO PIXEL ENCODING
(FOR FRAMEGRABBED VIDEO FRAMES ONLY)
A
B
C
R, TH
X,Y -> R, TH ADDRESS GENERATOR
FILTER COEFF. A
FILTER COEFF. B&C
Tissue
TISSUE ENCODER COMPR/REJ.
Tissue RGB
CFM f
CFM bw
FLOW ENCODER
CFM RGB
PIXEL MUX
OUTPUT FIFO
PIXEL DATA
OUTPUT MUX
PIXEL BUS 24 BIT RGB
PIXEL PORT ADDRESS
PIXEL ADDR.
TISSUE/FLOW ARBITER
CFM_SEL
MUX_SEL
SCAN CONVERTER
VME INTERFACE
68040 uP
DRAM
PIXEL PORT
BRIDGE
MUX
VRAM
RAMDAC
R G B
VIDEO
RS-232 INTF.
GRAPH
VIDEO S-VHS
RGB
(INT I/O -> VCR, PRINTERS AND EXT I/O))
(FRONT PANEL)
(SYSTEM MONITOR)
DESIGNER GRL
DATE 22/11-94
SIGN
CHECKED HCL
APPROVED KB
MODULE SYSTEM 5 DISPLAY AND CONTROL
SYSTEM 5
DRAWING NUMBER 330 FA299042
REV 02
FILE ../s5_dspl_block_01
TYPE OF DOCUMENT DETAILED BLOCK DIAGRAM
SHEET 1 OF 1

1 I/O - rev. 02


(PATIENT I/O)
SERIAL TRACE DATA AND PAT I/O CONTROL
PATIENT I/O
(SDP)
SERIAL TRACE DATA
P3-A18
(GRAPH)
FP RS-232 LINK
P2/P3
(SDP)
AUDIO A AUDIO B
P3-A15 P3-A16
(CPU)
VCR RS-232 LINK
P2/P3
(IMP) (GRAPH)
VIDEO IN/OUT
P3
(IMP) (GRAPH)
SVHS IN/OUT
(GRAPH)
RGBS
P3 P3 P3
(GRAPH)
RGBS
(CPU/GRAPH)
RS-232 INTF
P1/P2
(CPU)
SCSI BUS
P2
(CPU/GRAPH)
RS-232 INTF
P2/P3
(CPU)
VME BUS
P1/P2
(CPU)
ETHERNET
P2
(FEC)
C401 SRES_L
P3-B18 P3-B16
PATIENT I/O INTERFACE
INCL. DSP
REMOTE CONTROL (DSP)
VIDEO BUFFERS
LIVE
PLAY
AUDIO SWITCH
FROM DSP
AC POWER INTERFACE
VIDEO SWITCH
VIDEO SWITCH
VME INTERFACE
CLOCK DISTR.
TO DSP
EXT TRIG
AN. INPUTS 1-4
PAR. INTF
PARALLEL INTERFACE (DSP)
PARALLEL
RGBS OUT
SVHS IN/OUT
VIDEO IN/OUT
INTERNAL I/O
RS232-GR
R-WAVE OUT
FOOTSW.
AC CTRL
FOOTSWITCH
RS-232-CPU
RS-232-GR
SCSI
EXT I/O
EXT
ETHERNET
INT
ETHERNET LOOP CABLE (ALSO TO INTERNAL DEVICES)
REPLAY
VCR AUDIO
RS232-CPU
SVHS OUT
SVHS OUT
SVHS IN
REM CTRL
HC-RGBS
REM CTRL
VIDEO OUT
VIDEO IN
RGBS
VCR
MONITOR
COLOR PRINTER
B/W PRINTER
FLOPPYDISC
HARDDISC
LASER PRINTER
EXTERNAL I/O
A/D
ANALOG INPUTS 1-4
TRIG OUT
RS-232-CPU
RS-232-GR
ETHERNET INTERFACE
ETHERNET
VIDEO IN
VIDEO OUT
SVHS IN
SVHS OUT
B/W VIDEO OUT
RGBS OUT
RGBS OUT
MONITOR
FRONT PANEL MAIN BOARD
SERIAL SYSTEM INTF.
LOCAL uP
RAM
PRGR PROM
CHIP SELECTS
ADDRESS DECODER
ROTARY DECODER
ROTARY KNOBS
LED ACTIVATERS
V
LED_EN_L
BRIGHT
DIM
BLEN_L
GND
TGC DECODER
MUX & A/D
V
GND
SLIDE POTS
VIA
TRACKBALL DECODER
TOGGLE DECODER
BEEPER CONTROL
LIGHT CONTROL
SWITCH MATRIX DECODER
SWITCHES
COL
ROW
AUDIO A
AUDIO B
AUDIO AMPL.
SPEAKERS
AC POWER CONTROLLER
PWR CTRL
TEMP CTRL
DC ON/OFF
DC POWER
ON/OFF
TEMPIN HITEMPIN
FAN CTRL VOLT.
POWER SWITCH
TEMP. SENSOR
AC OUTLETS
ROTARY/ DISPLAY BOARD
ROTARY DECODER
ROTARY KNOBS
GAIN.....REJECT
DISPLAY 1
GAIN.....REJECT
GAIN.....REJECT
DISPLAY 2
GAIN.....REJECT
TRACKBALL
TOGGLES
QUERTY KEYBOARD
LAMP
BEEPER
DESIGNER GRL
DATE 22/11-94
SIGN
CHECKED GJ
DATE
SIGN
APPROVED KB
DATE
SIGN
FILE ../s5_io_block
MODULE SYSTEM 5 (KEYBOARD, I/O, PERIPHERALS)
SYSTEM 5
DRAWING NUMBER 330 FA299271
REV 02
TYPE OF DOCUMENT BLOCK DIAGRAM
SHEET 1 OF 1

SYSTEM FIVE Block Diagrams – Boards

Overview

Introduction

This part of the Service Manual holds the block diagrams for the SYSTEM FIVE boards.

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
• Relay Board Block Diagram – rev. 04	B2-3
• TX-128 Block Diagram – Rev. 02	B2-4
• RX128 (RX64) Block Diagram – Rev. 03	B2-5
• Probe Controller Block Diagram – rev. 02	B2-6
• Beam Former Boards Block Diagram – rev. 02	B2-7
• Front End Controller Board Block Diagram – rev. 02	B2-8
• Patient I/O Block Diagram – rev. 02.	B2-9
• RF & Tissue Proc. Block Diagram – rev. 02	B2-10
• Spectrum Doppler Processor – rev. 02.	B2-11
• 2D Flow Board Block Diagram – rev. 01	B2-12
• Image Port Block Diagram – rev. 01	B2-14
• Image Memory Block Diagram – rev. 01	B2-15
• Scan Converter Block Diagram – rev. 01	B2-16
• Graphic µP Board Block Diagram – rev. 01	B2-17
• CPU Block Diagram – rev. 01.	B2-18
• Front Panel Block Diagram – rev. 01.	B2-19
• Internal I/O Block Diagram – rev. 01	B2-20
• External I/O Block Diagram – rev. 02	B2-21
• AC Power Block Diagram – rev. 02	B2-22
• DC Power Supply Block Diagram – rev. 02.	B2-23
• High Voltage Power Supply Block Diagram – rev. 02	B2-24

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:B2_01_Innh.02.
Printed: December 5, 2000.

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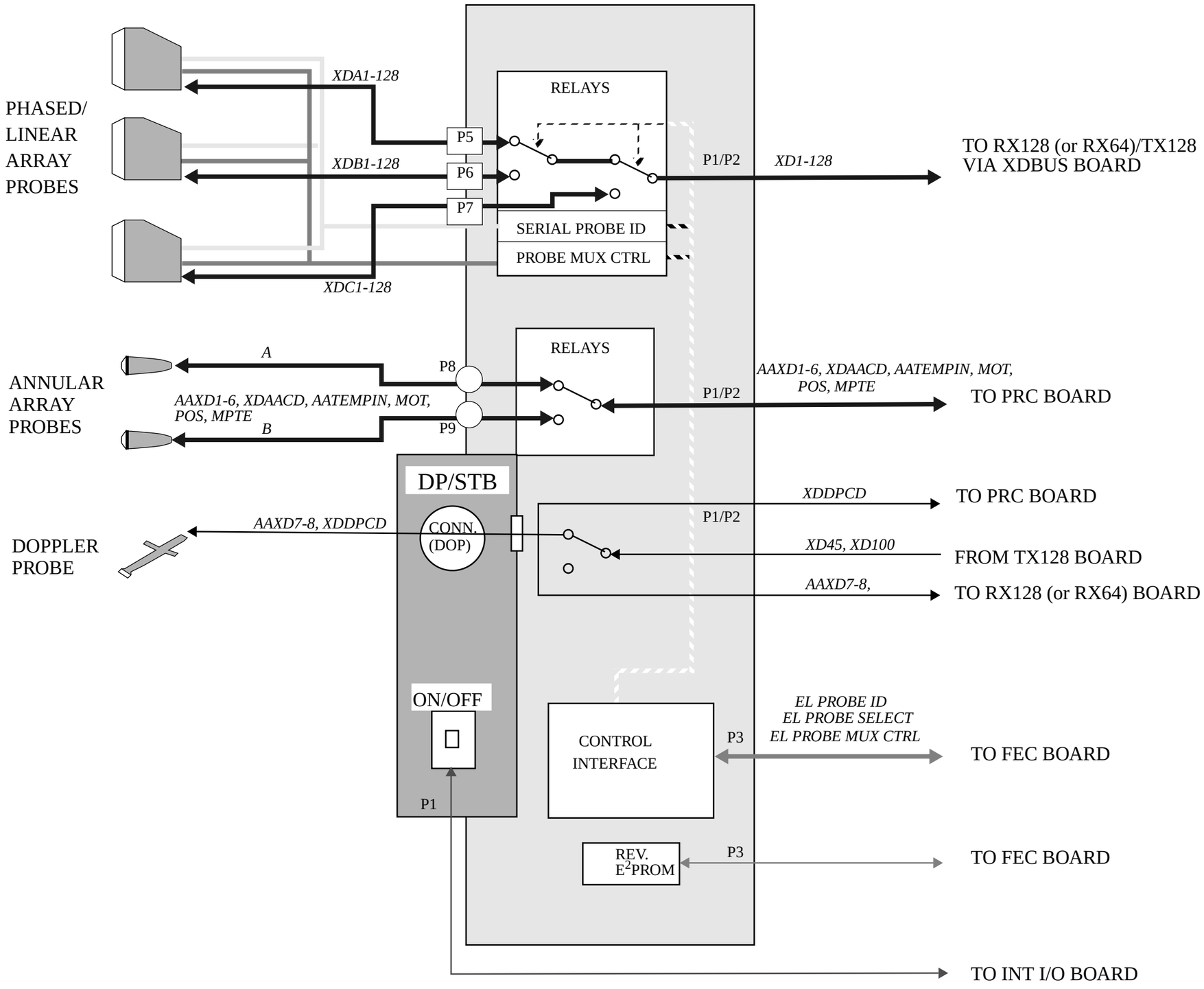
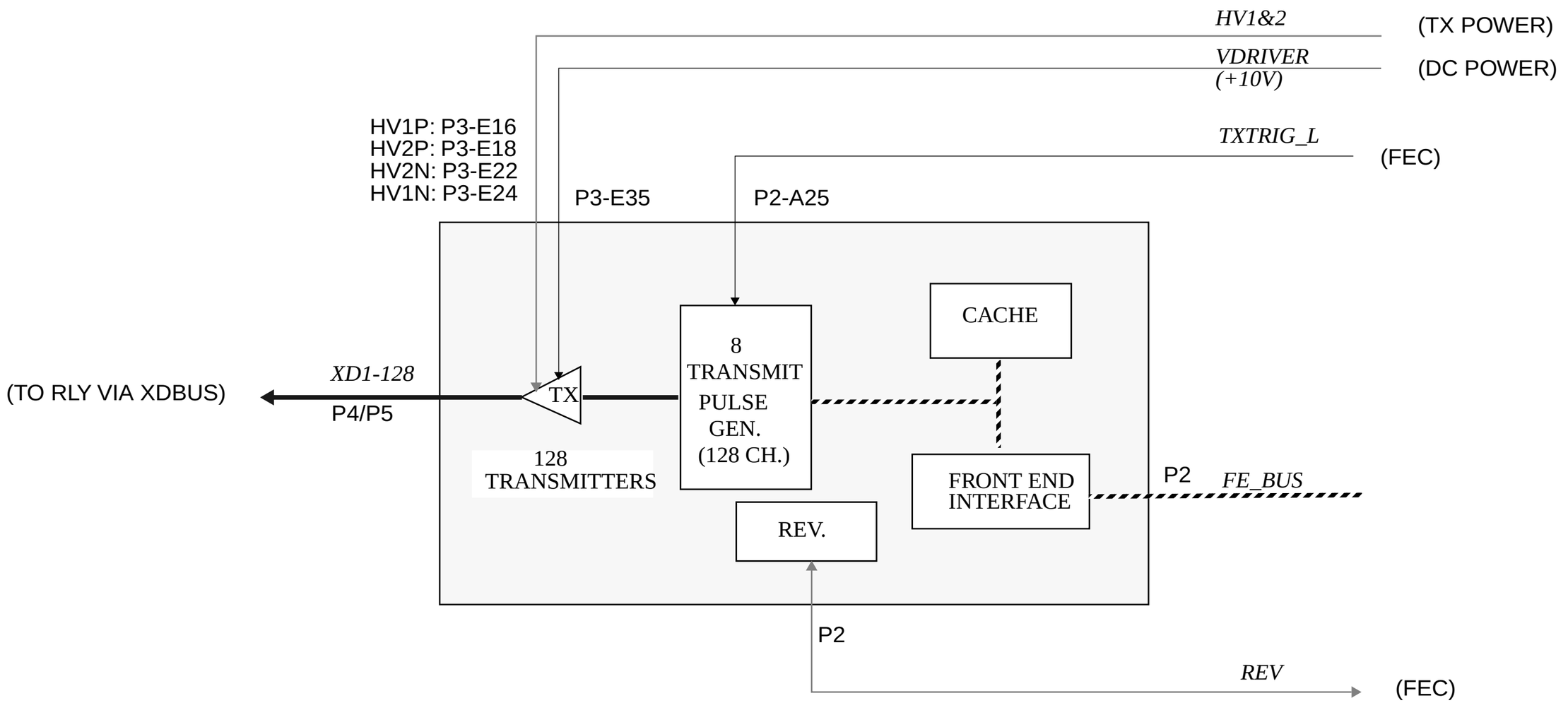
Relay Board Block Diagram – rev. 04

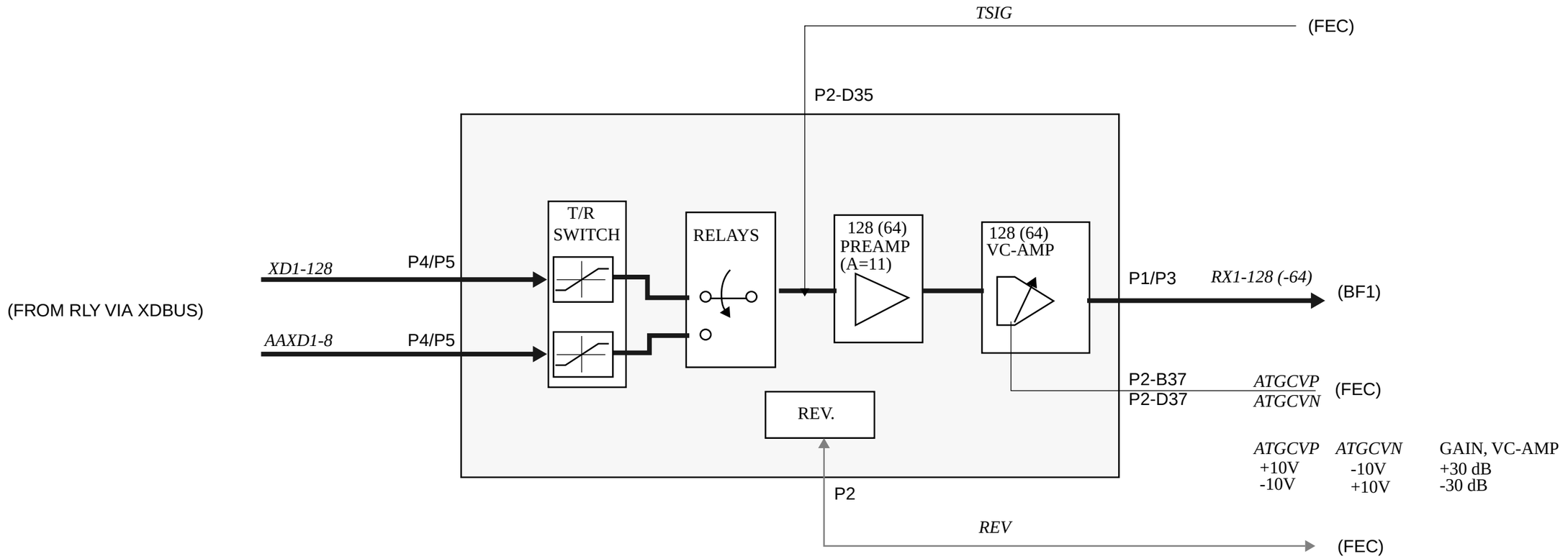


TX-128 Block Diagram – Rev. 02



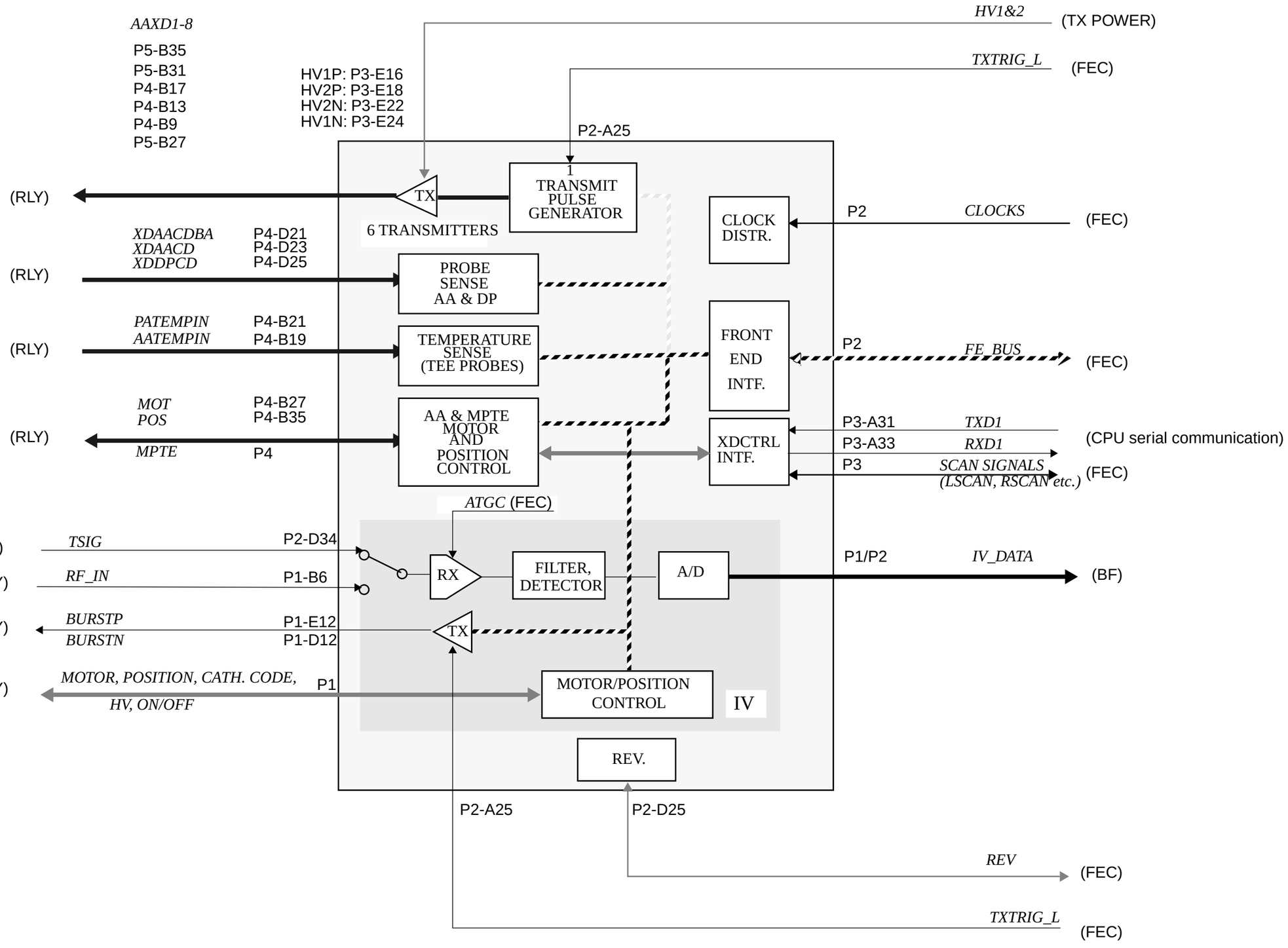
Rev. 02

RX128 (RX64) Block Diagram – Rev. 03

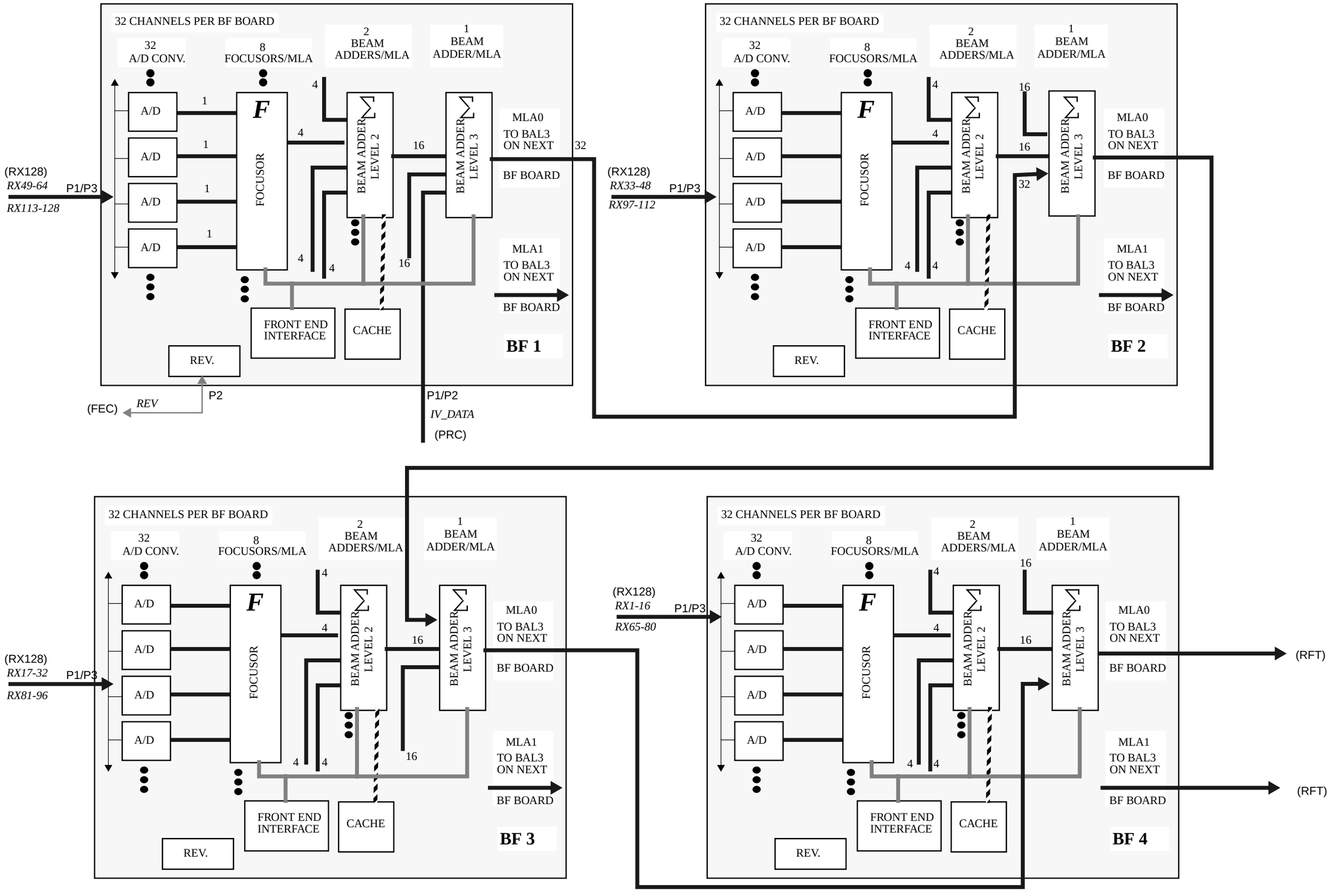


Rev. 03

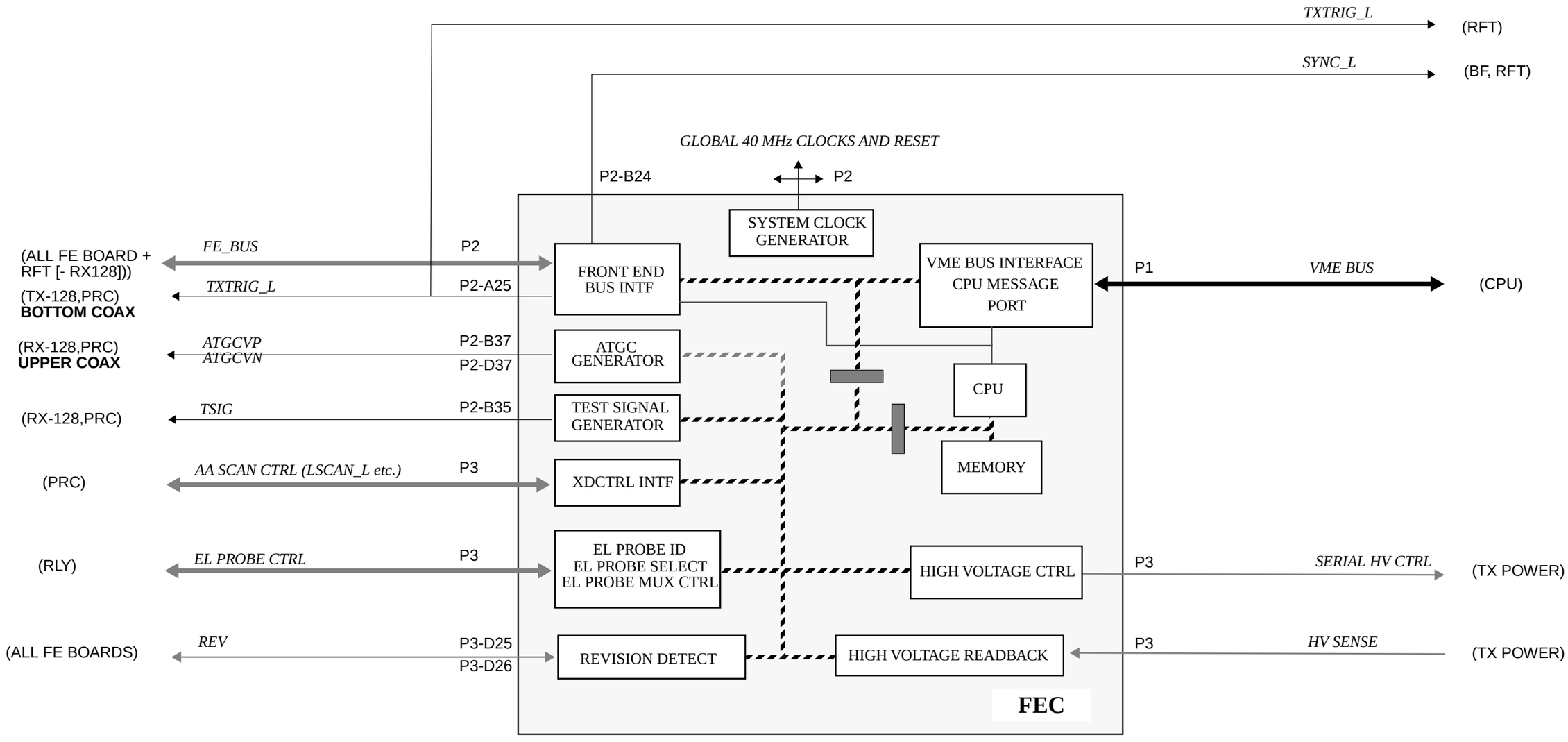
Probe Controller Block Diagram – rev. 02



Beam Former Boards Block Diagram – rev. 02

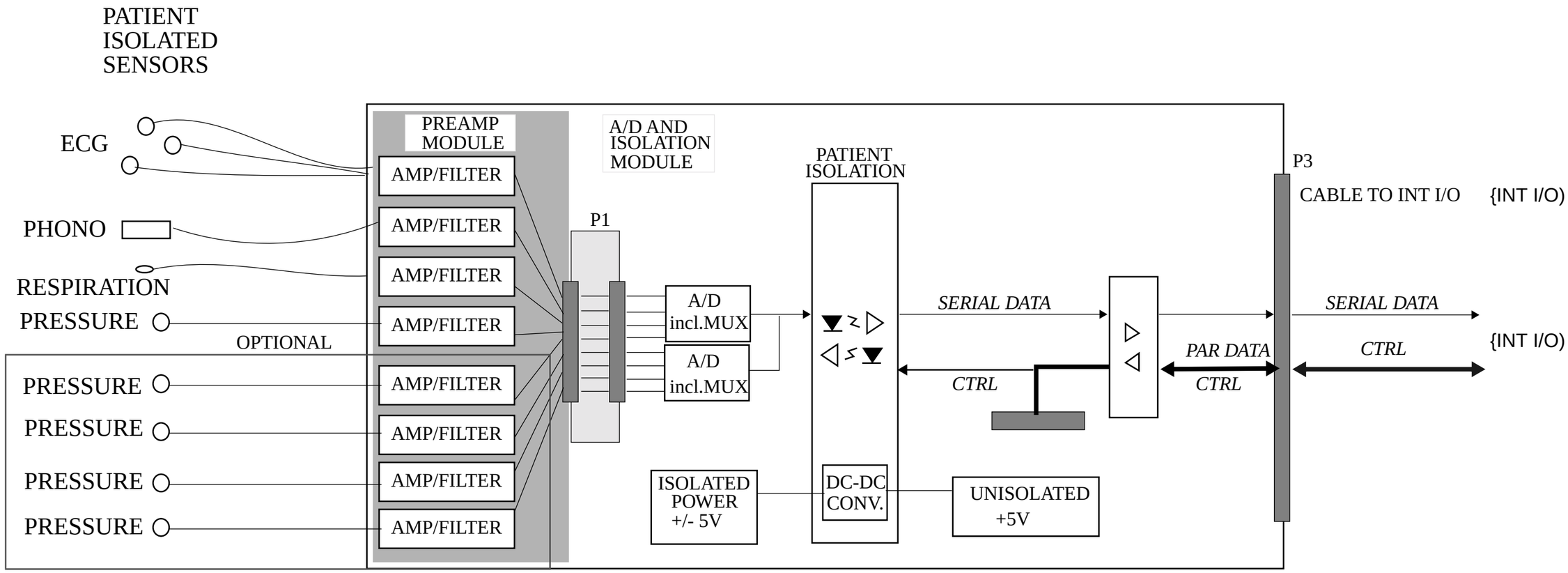


Front End Controller Board Block Diagram – rev. 02



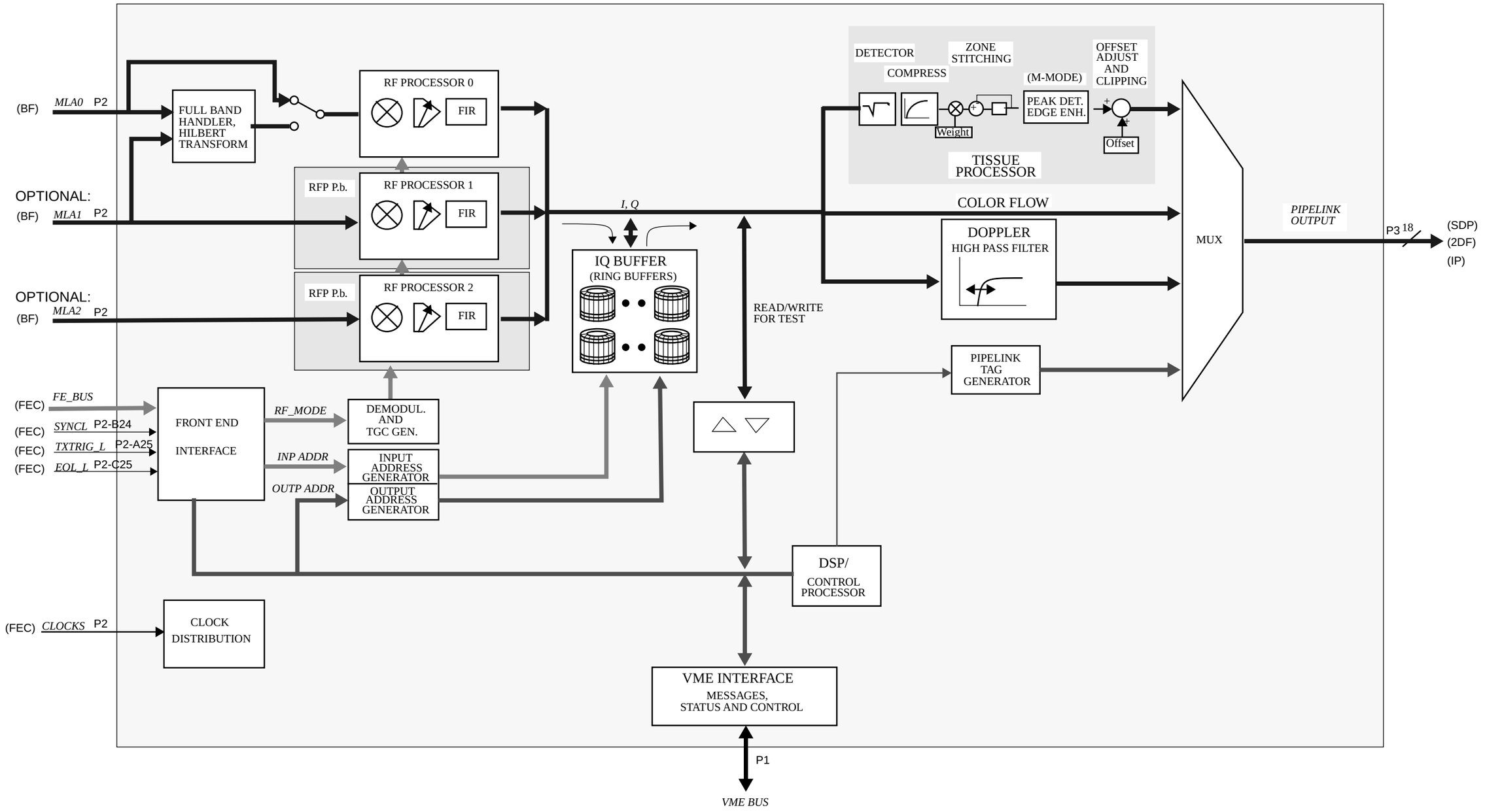
Rev. 02

Patient I/O Block Diagram – rev. 02



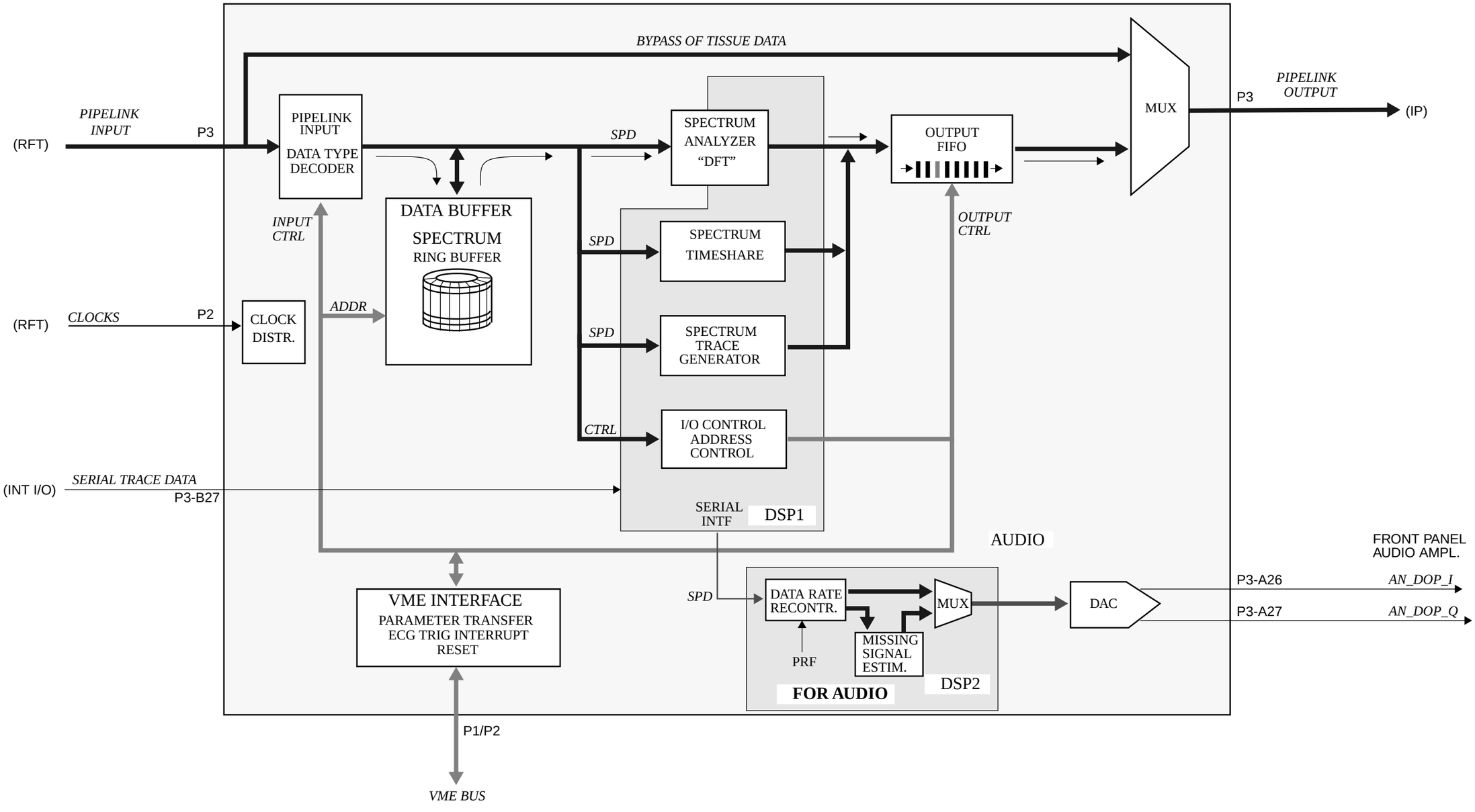
Rev. 02

RF & Tissue Proc. Block Diagram – rev. 02



Rev. 02

Spectrum Doppler Processor – rev. 02



Rev. 02

2D Flow Board Block Diagram – rev. 01

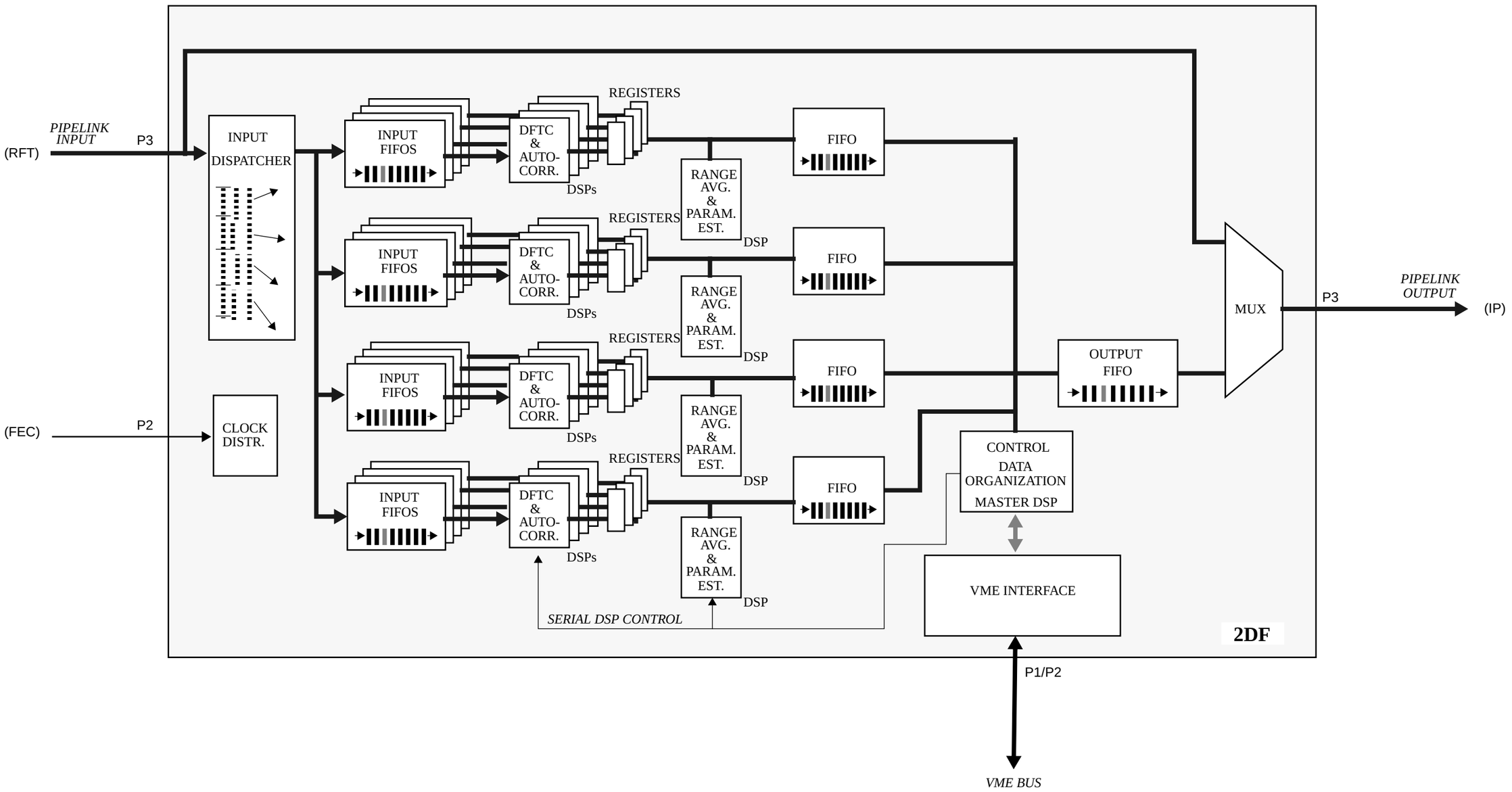


Image Port 2 Board Block Diagram - rev.01

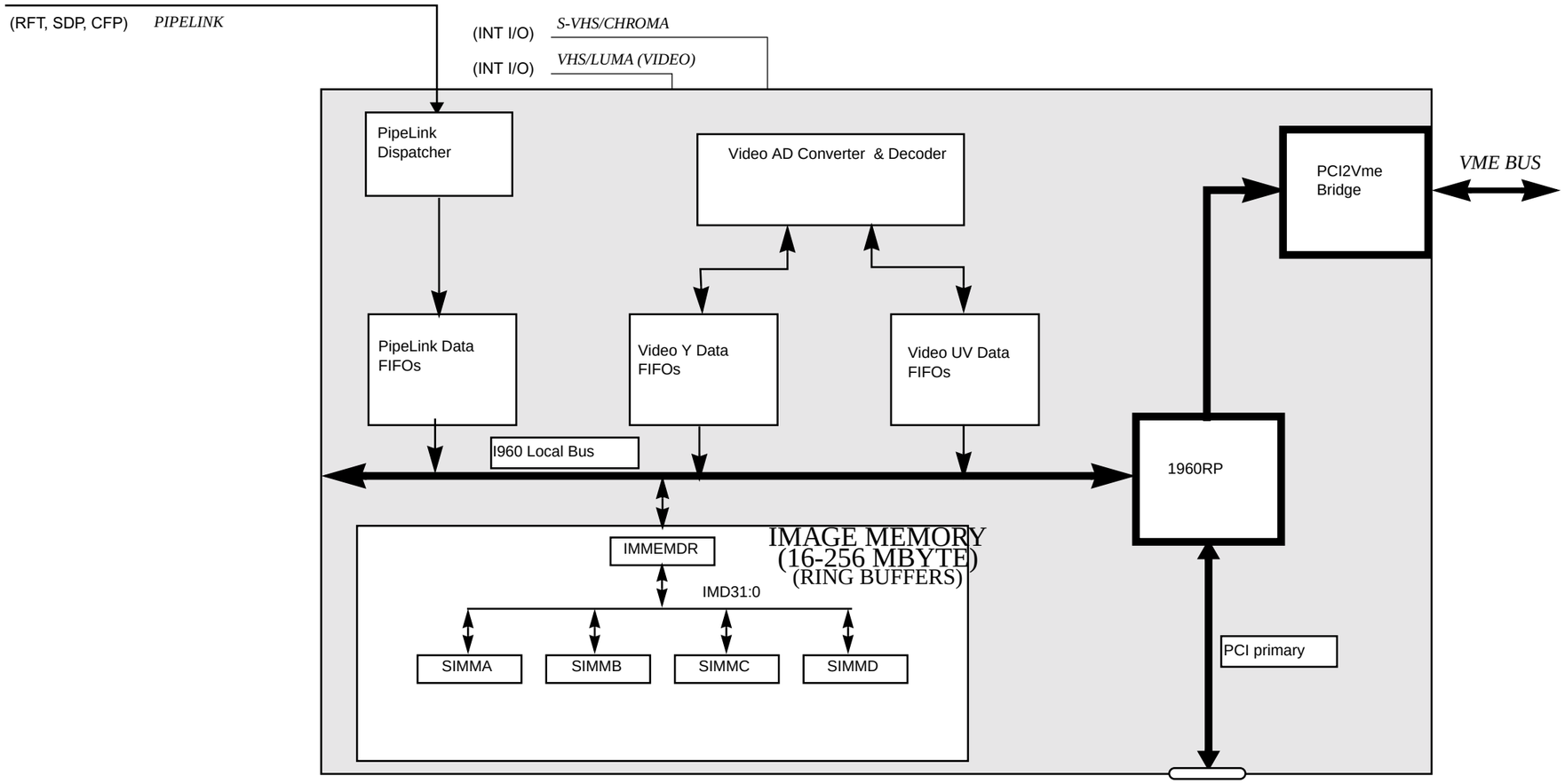
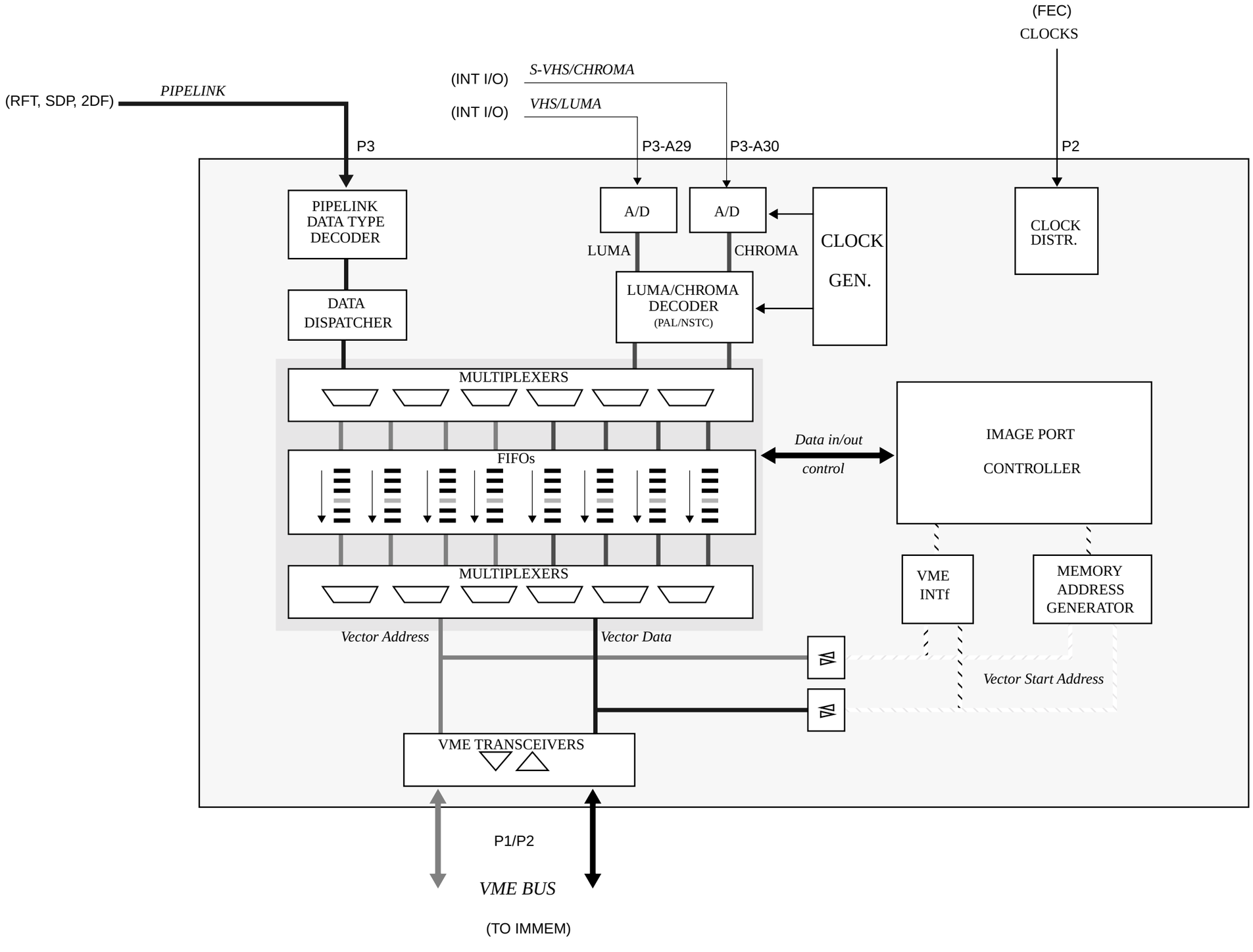


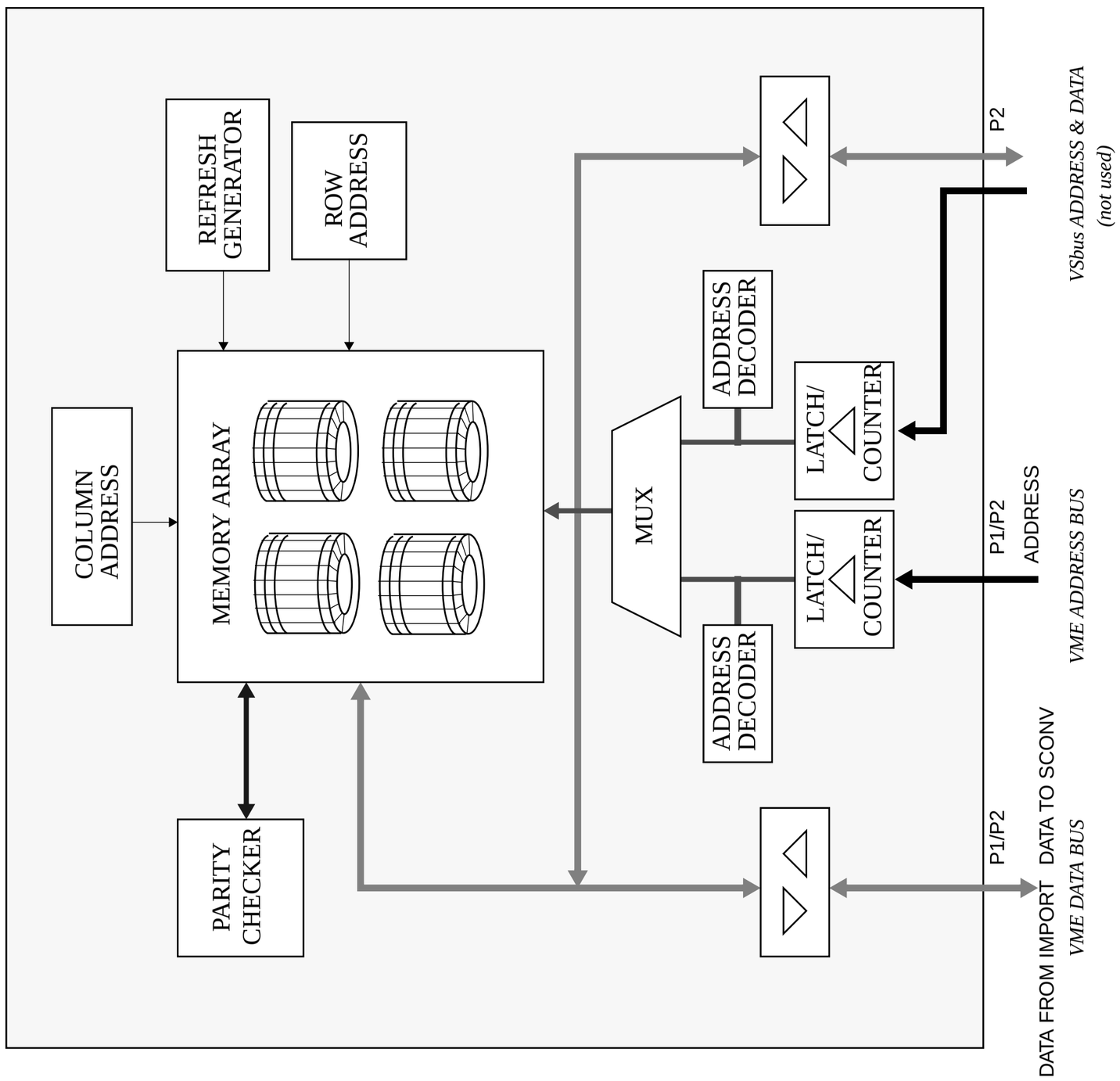
Image Port Block Diagram – rev. 01



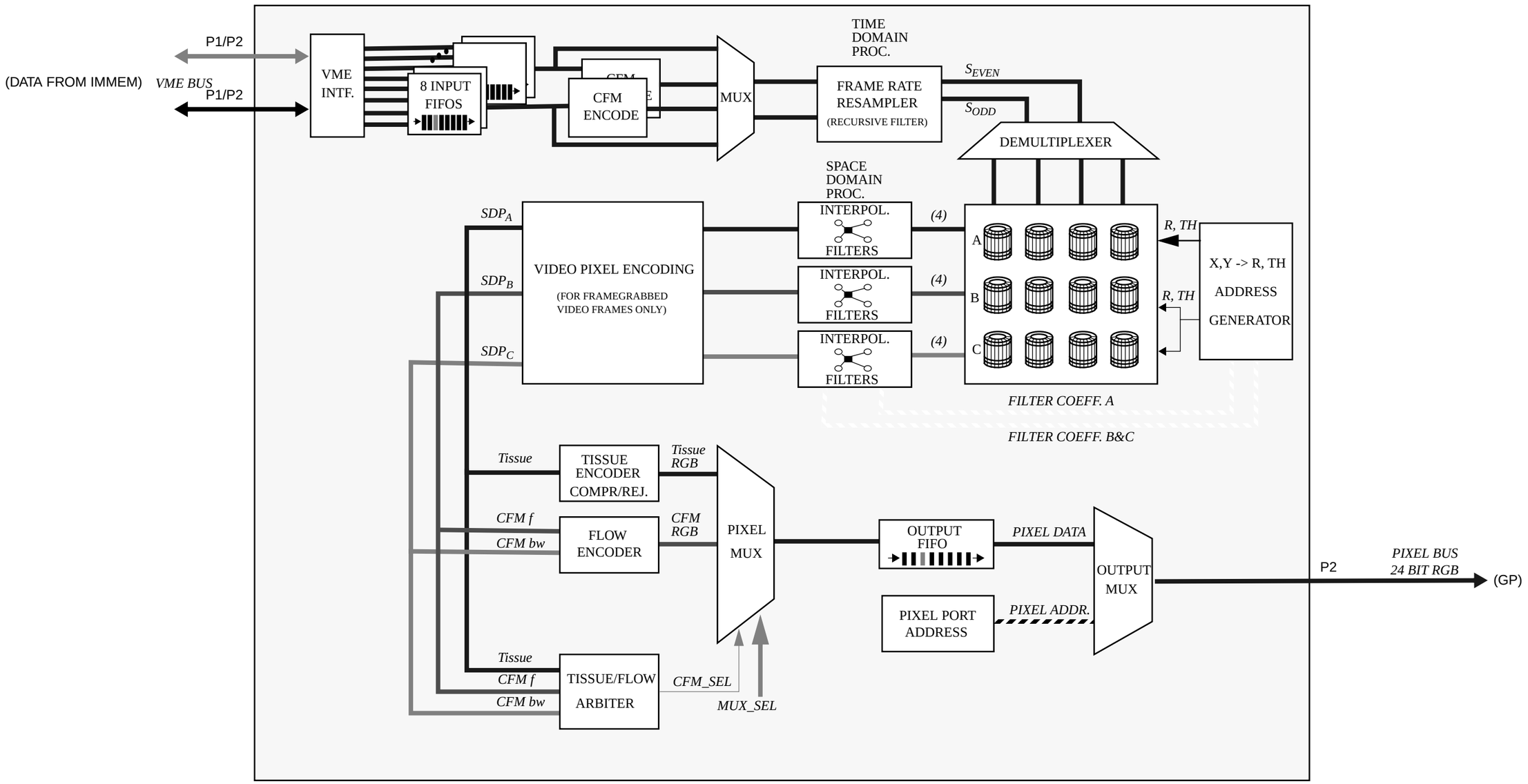
Rev. 01

Image Memory Block Diagram – rev. 01

Rev. 01

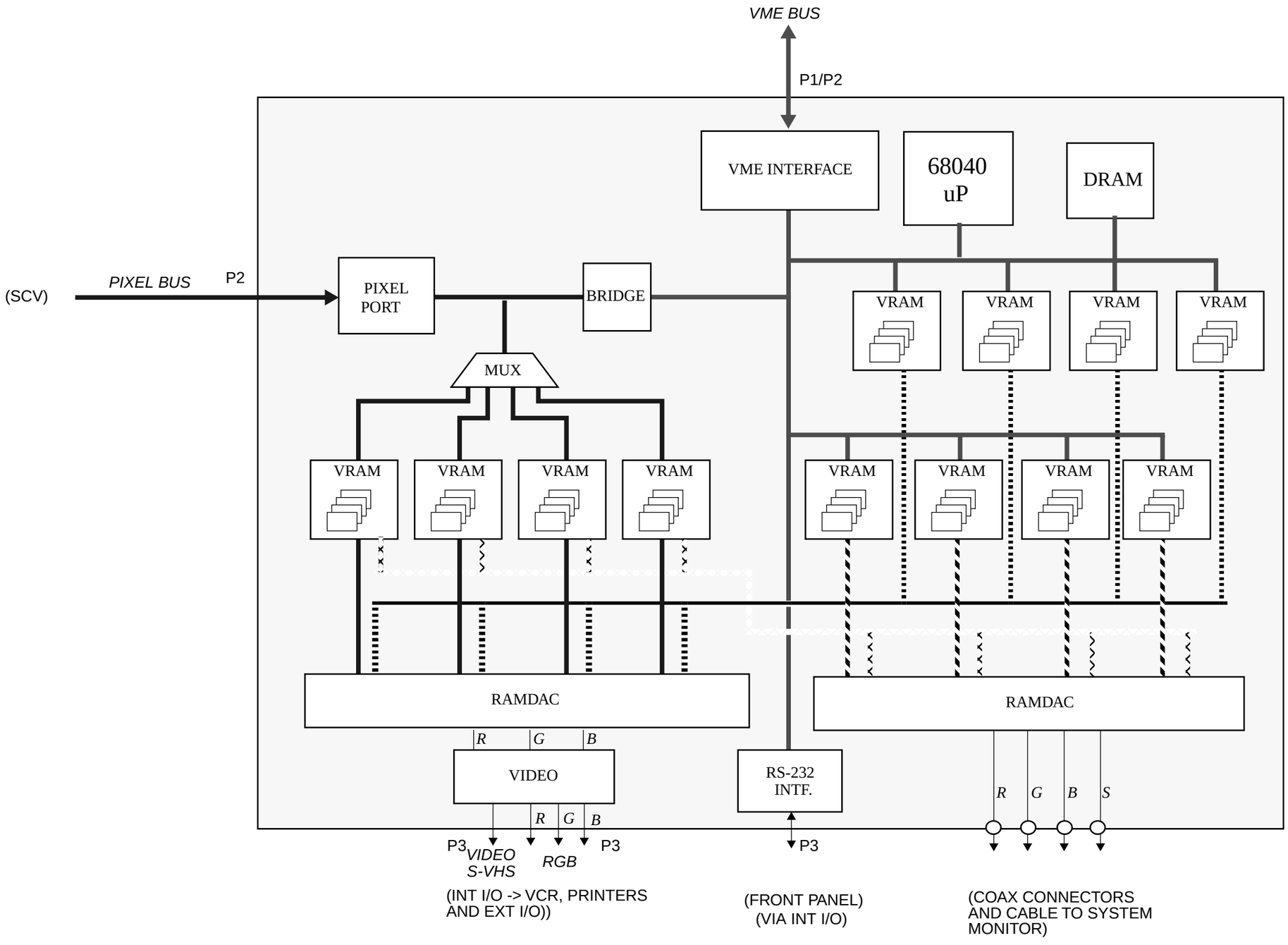


Scan Converter Block Diagram – rev. 01



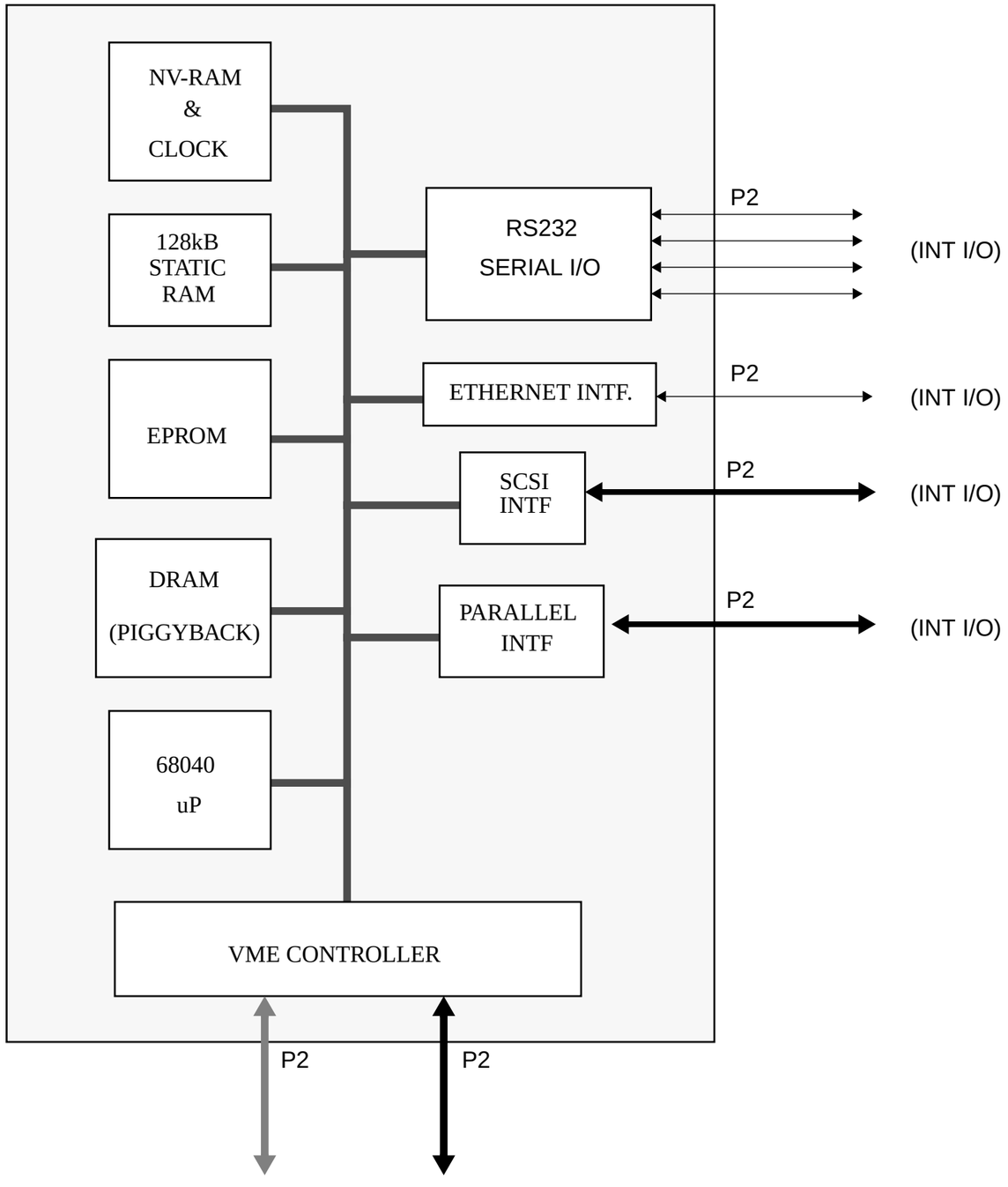
Rev. 01

Graphic µP Board Block Diagram – rev. 01



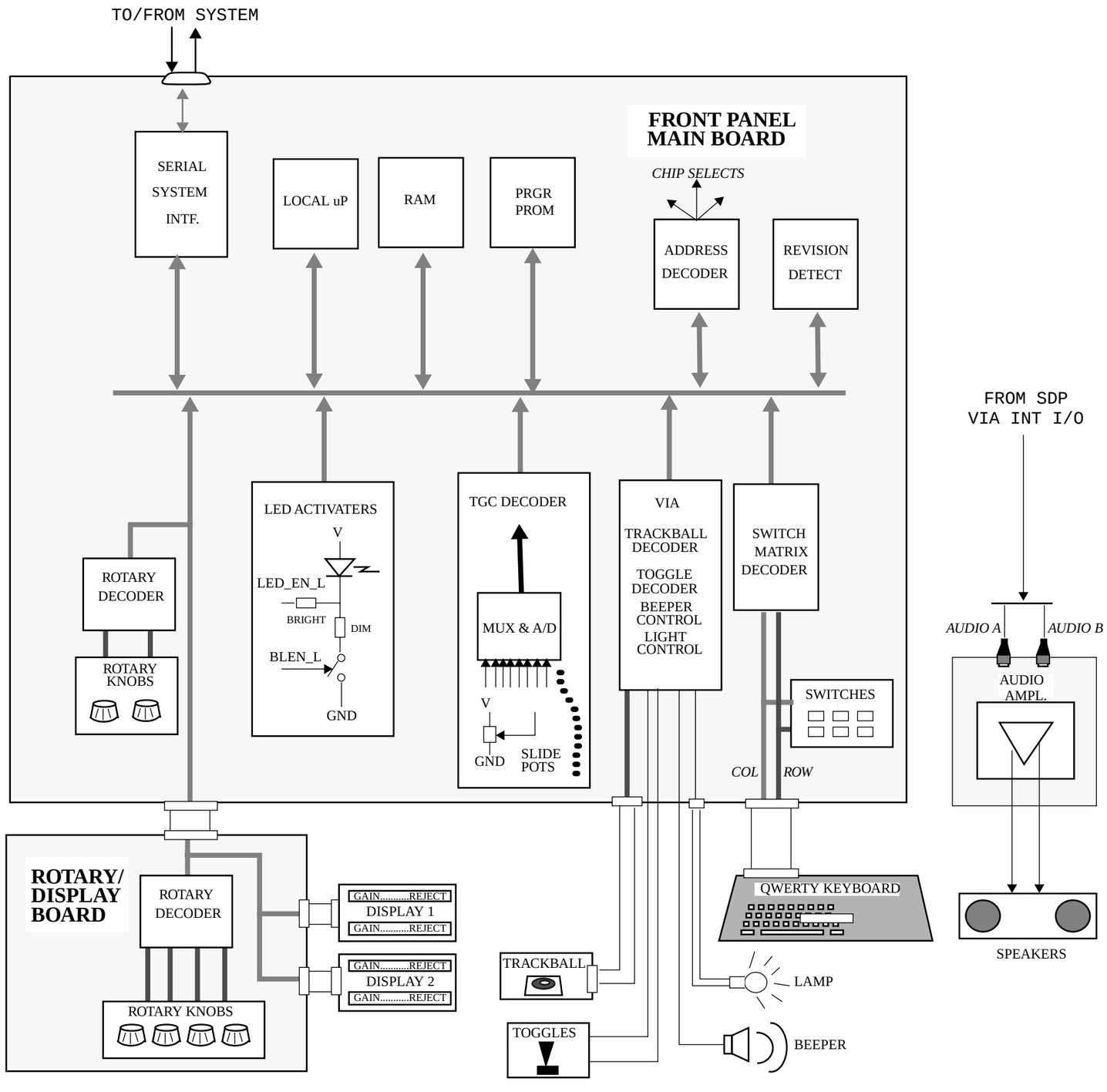
Rev. 01

CPU Block Diagram – rev. 01



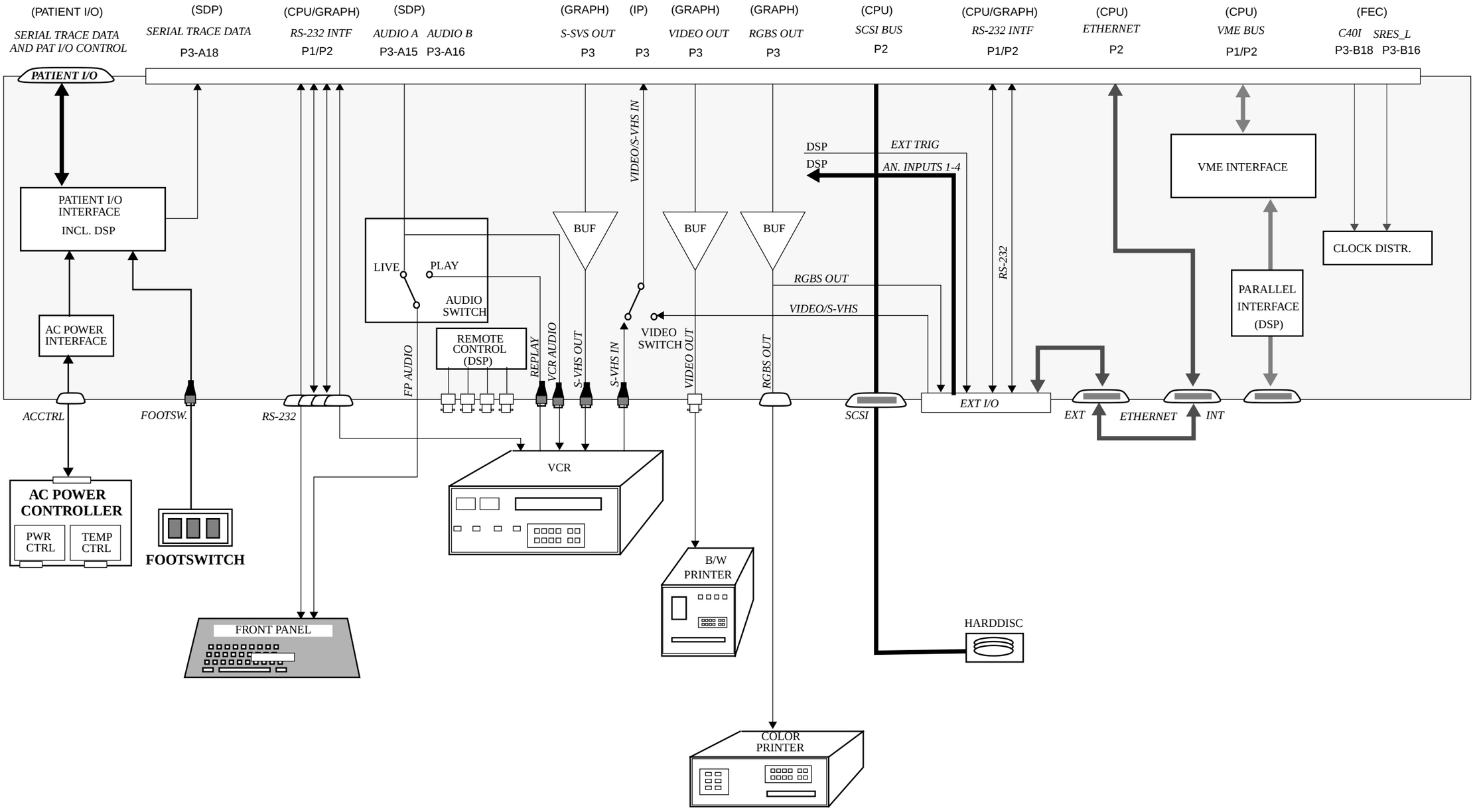
Rev. 01

Front Panel Block Diagram – rev. 01



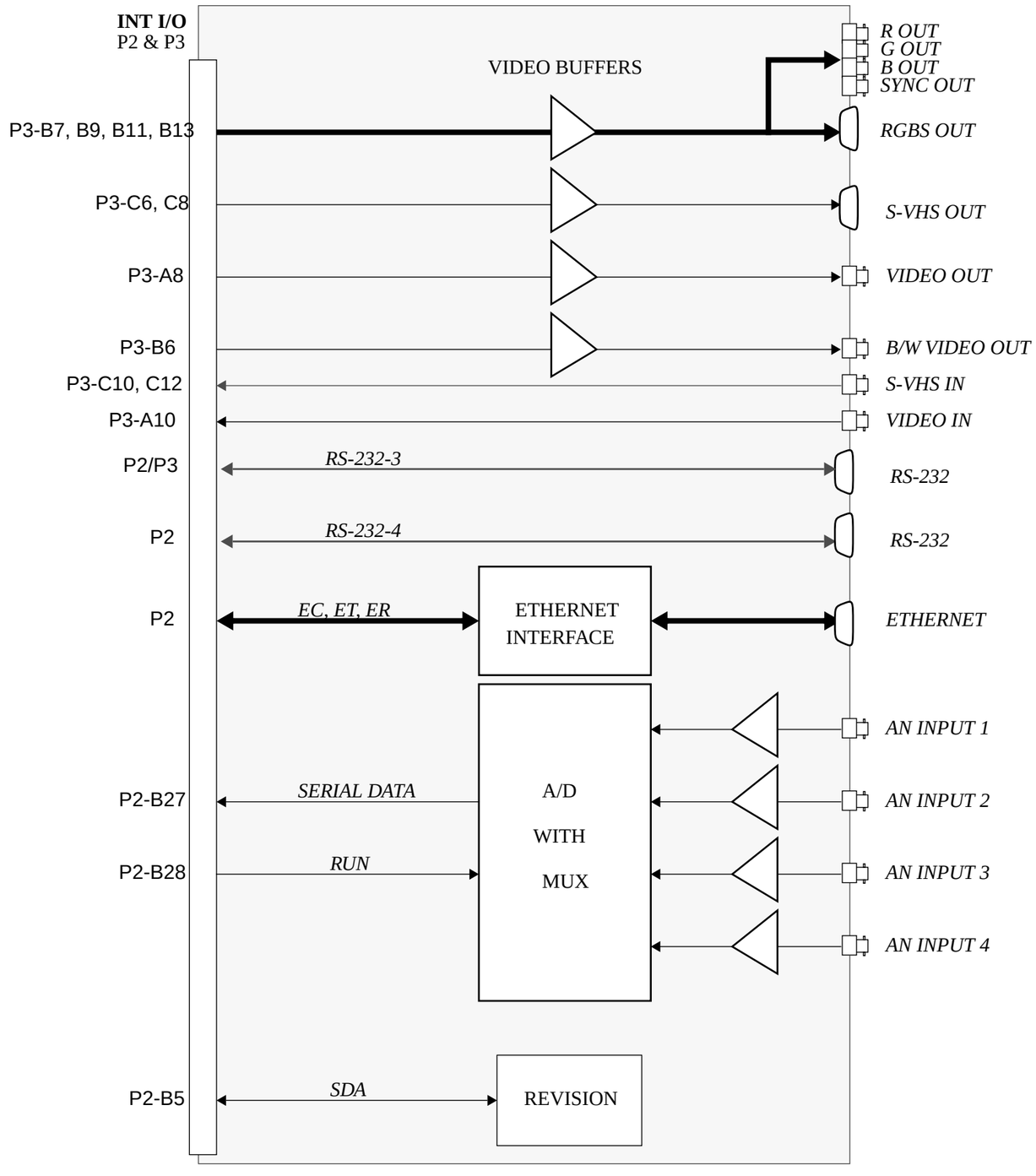
Rev. 01

Internal I/O Block Diagram – rev. 01



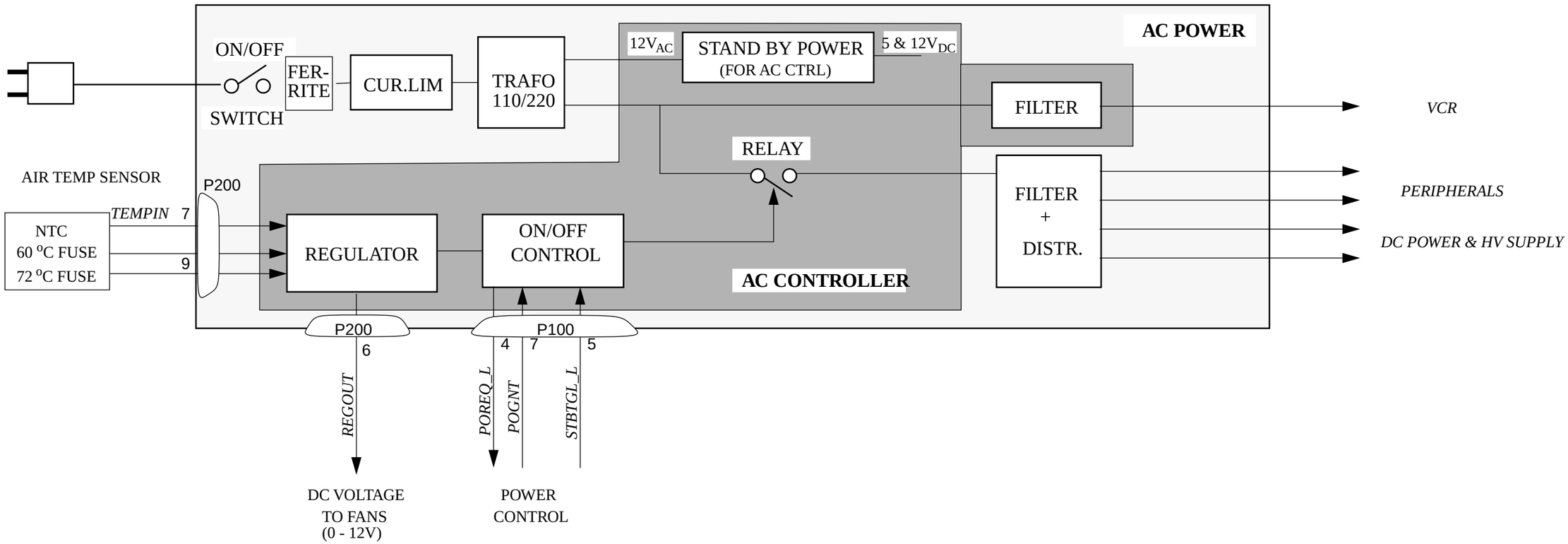
Rev. 01

External I/O Block Diagram – rev. 02



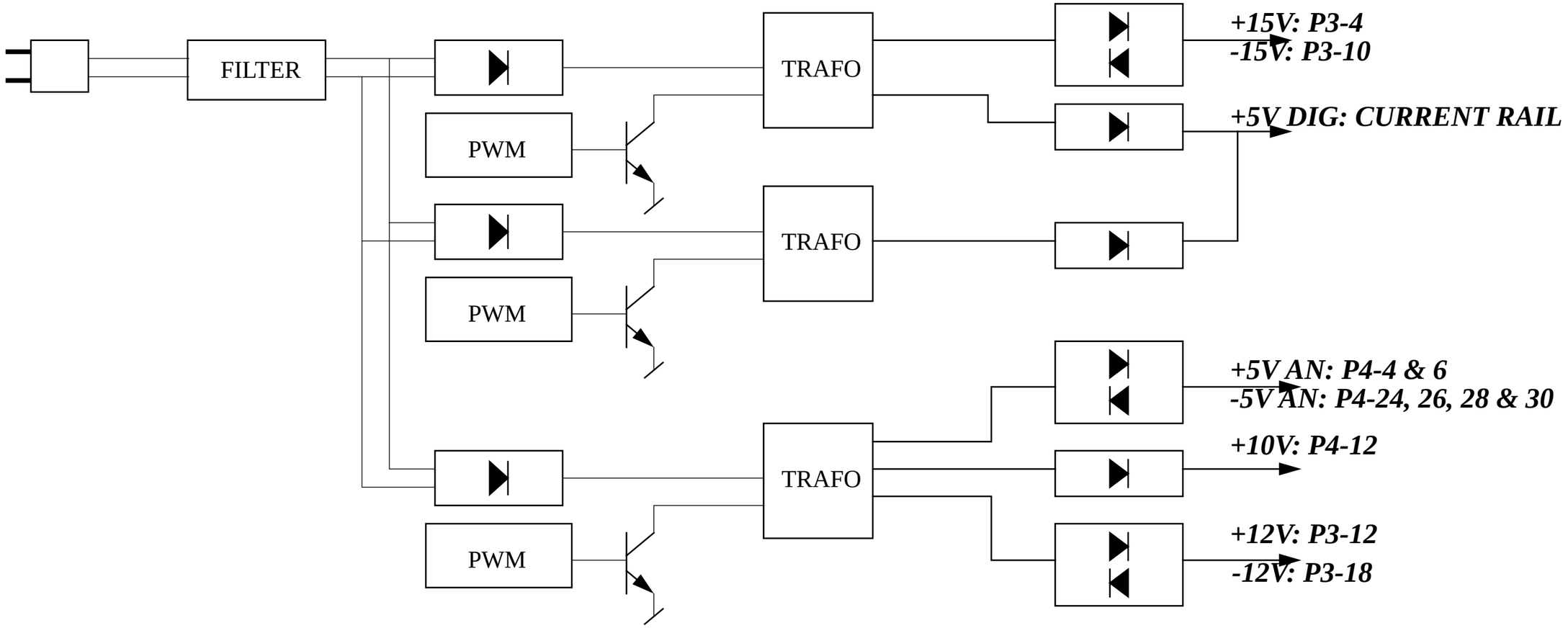
Rev. 02

AC Power Block Diagram – rev. 02



Rev. 02

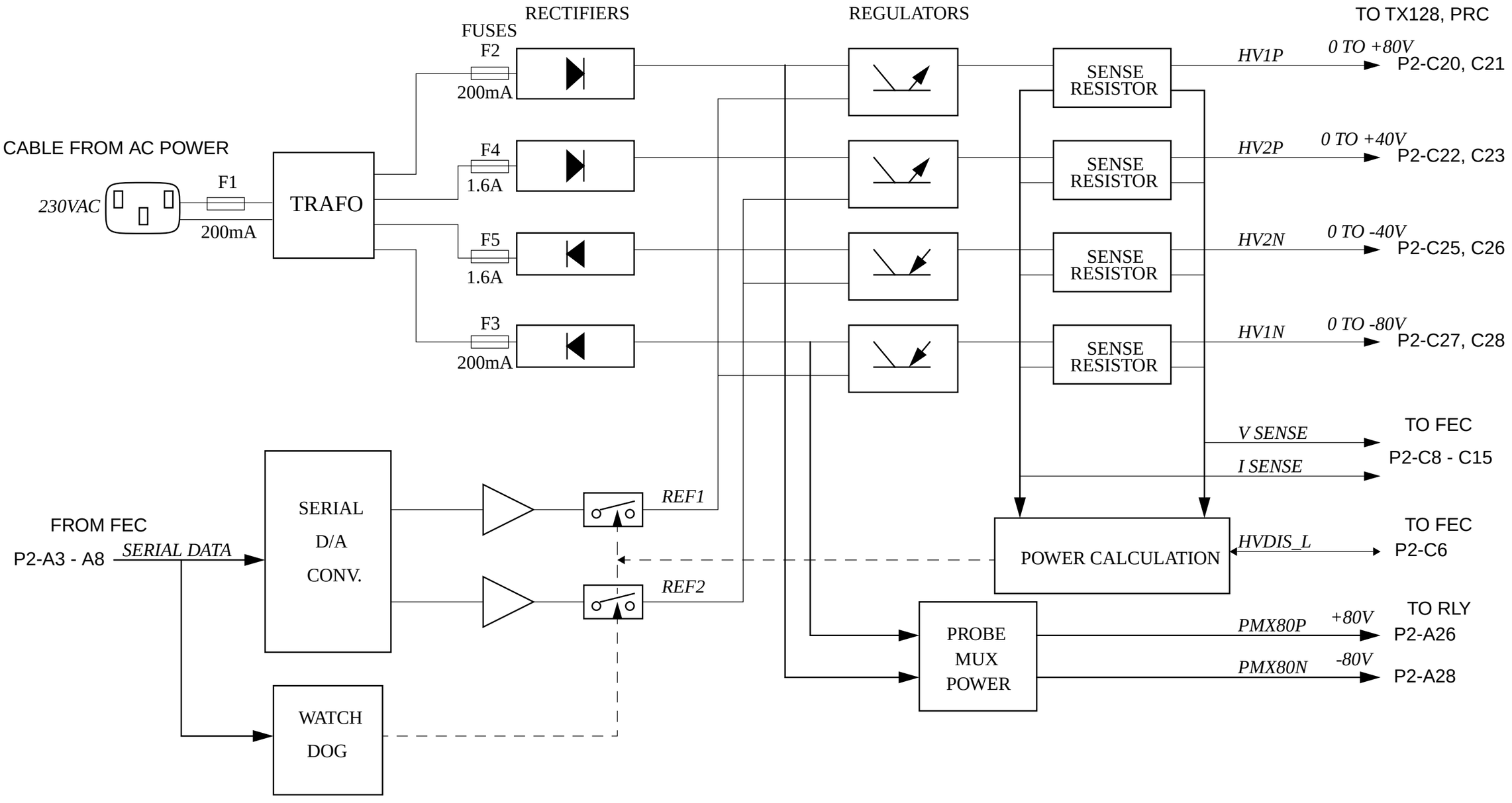
DC Power Supply Block Diagram – rev. 02



Drawing by GJ.

Rev. 02

High Voltage Power Supply Block Diagram – rev. 02



Drawing by G.J.

Rev. 02

SYSTEM FIVE Block Diagrams

Overview

Introduction

This part of the Service Manual holds the block diagrams for SYSTEM FIVE .

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
Clock Distribution — rev. 01	B3 - 3
Control and Data Flow – rev. 01	B3 - 4
System FiVe Data Flow Schematic – rev. 05	B3 - 5
Motherboard with Major “Buses” — rev. 02	B3 - 6
System FiVe Overall Power Distribution – rev. 05	B3 - 7

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:B3_01_Innh.03.
Printed: December 5, 2000.

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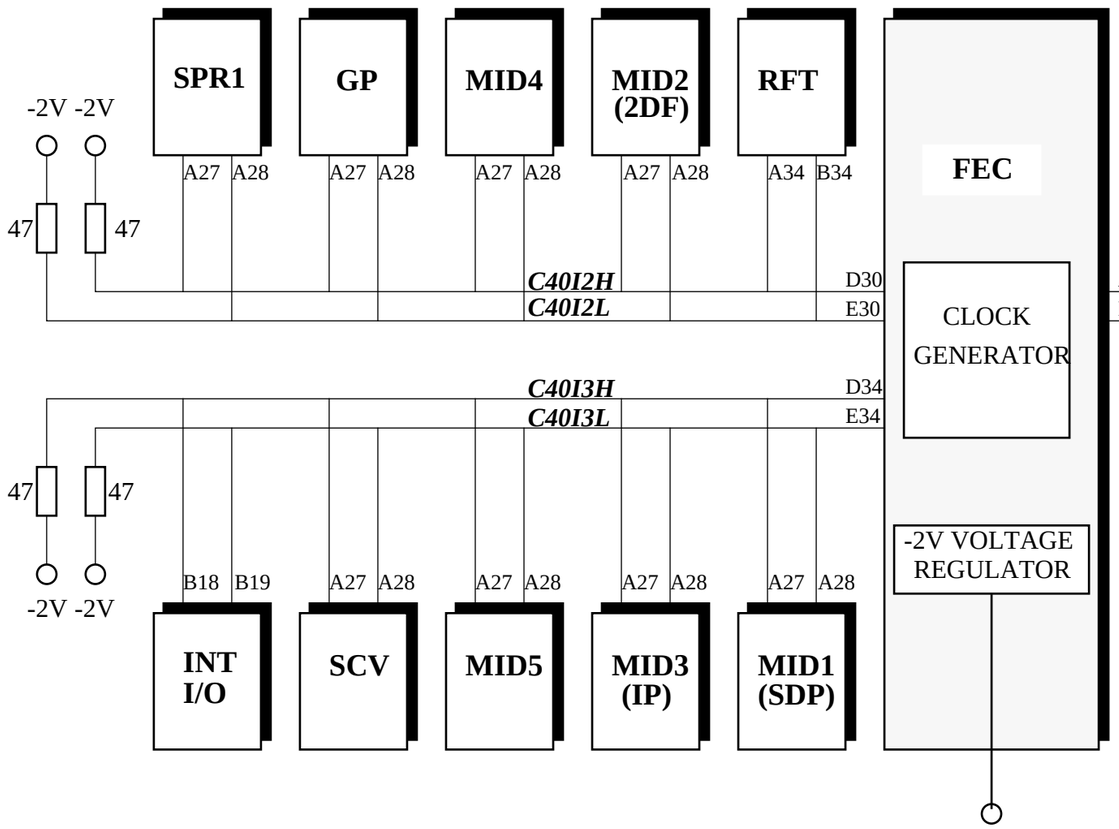
1 Clock Distribution — rev. 01

Only I-phase shown



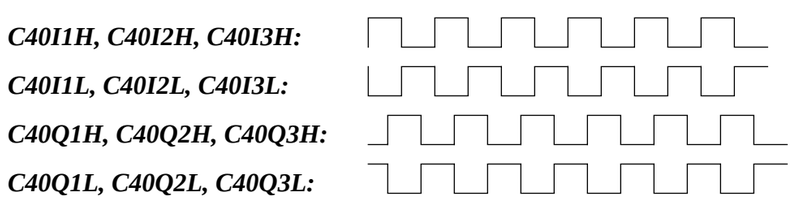
Comments:

All clocks are distributed on the P2 connector, except to INT I/O which uses P3.

In addition to the clocks, a sync. reset signal, ***SRESnH*** and ***SRESnL*** (n = 1,2,3) is also distributed in the same way.

All clocks and reset signals are at ECL level: Typically between -0.9V (high) and -1.8V (low).

40 MHz I & Q Clocks



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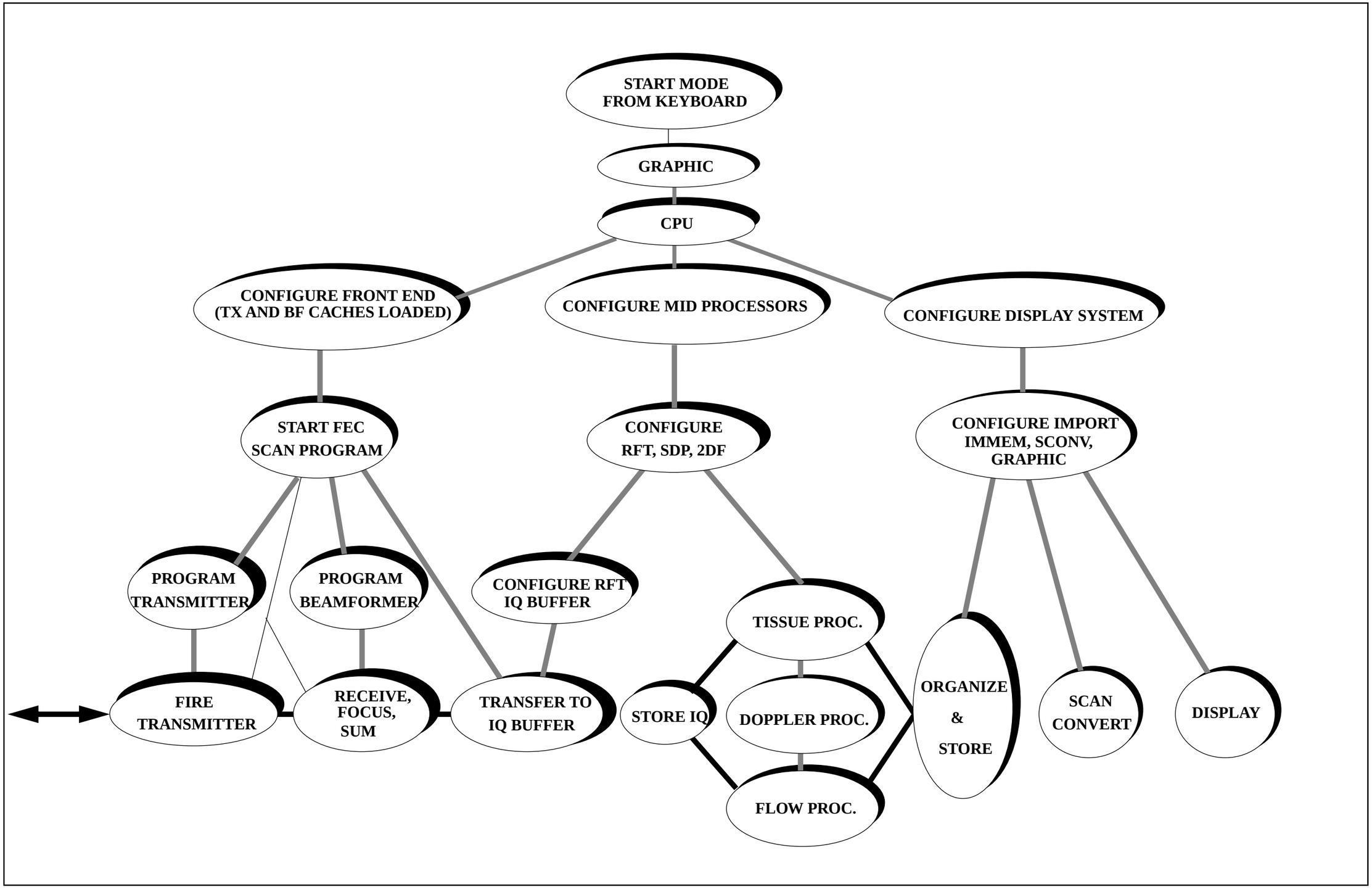
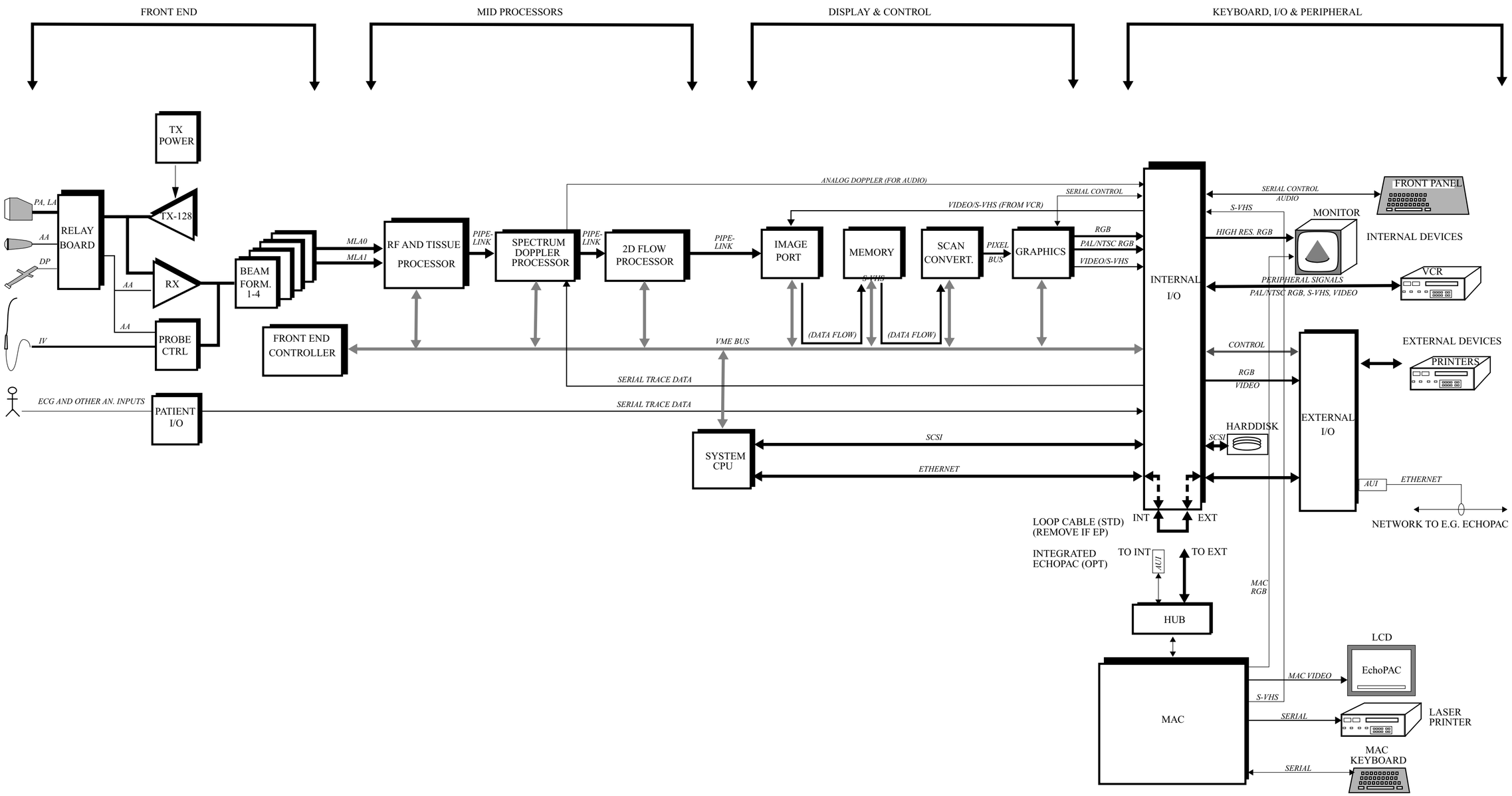
Printed: December 5, 2000.

2 Control and Data Flow – rev. 01



Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:B3_03_ctrl_seq.
Printed: December 5, 2000.

System FiVe Data Flow Schematic – rev. 05



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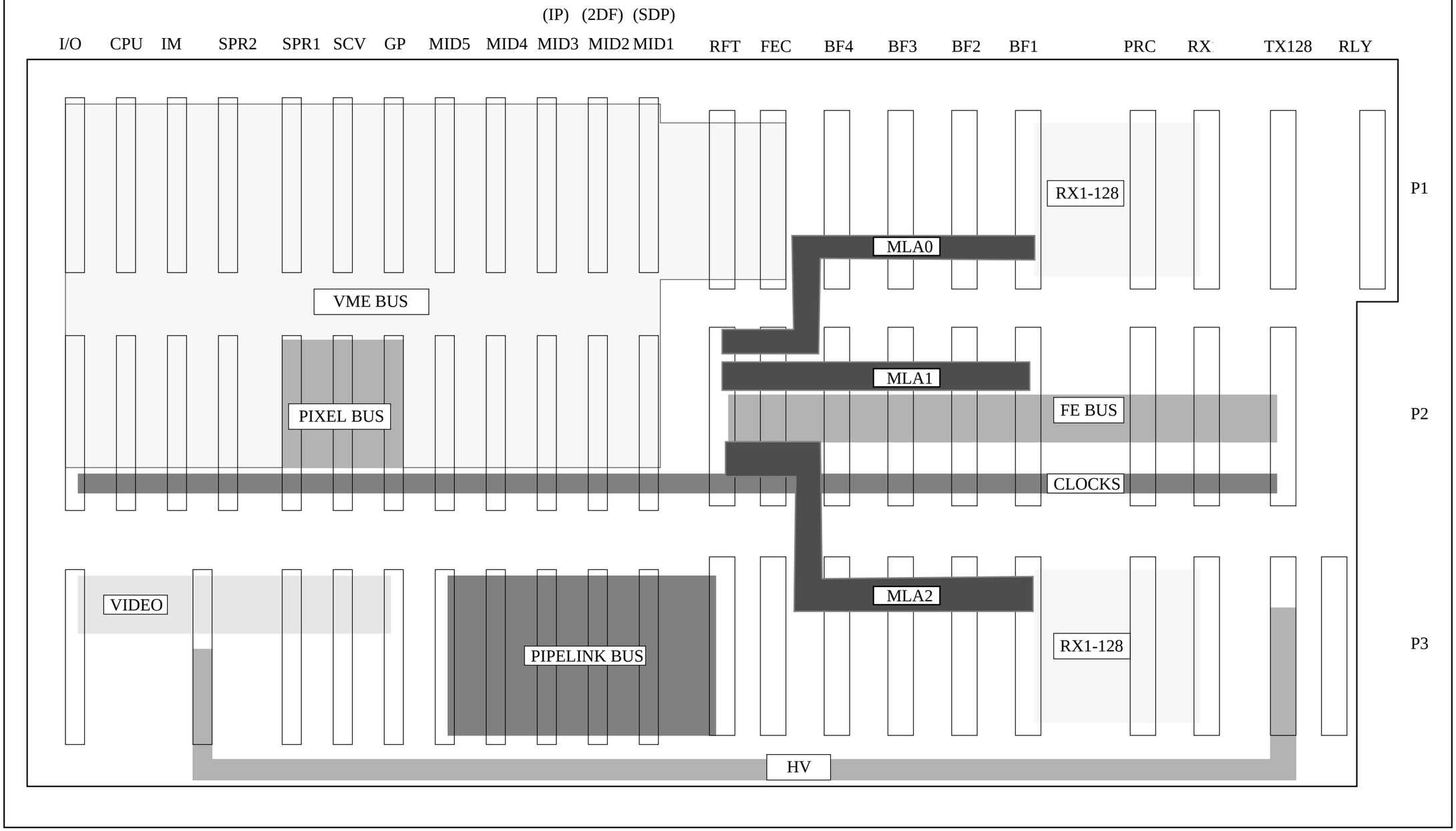
Printed: December 5, 2000.

Motherboard with Major “Buses” — rev. 02



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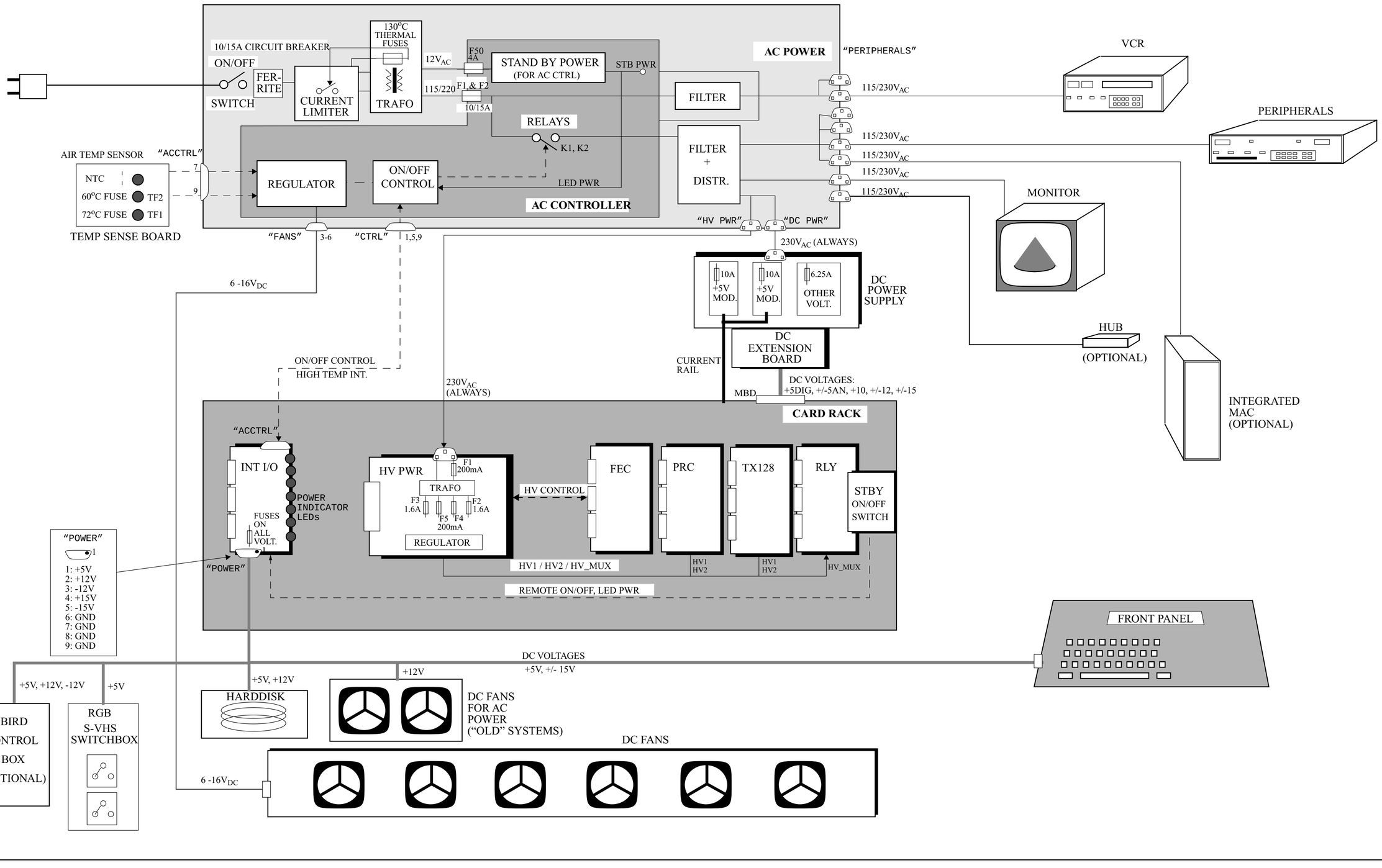
Printed: December 5, 2000.

5 System FiVe Overall Power Distribution – rev. 05



SYSTEM FIVE Cables

Overview

Introduction

This part of the Service Manual describes the cables in SYSTEM FIVE .

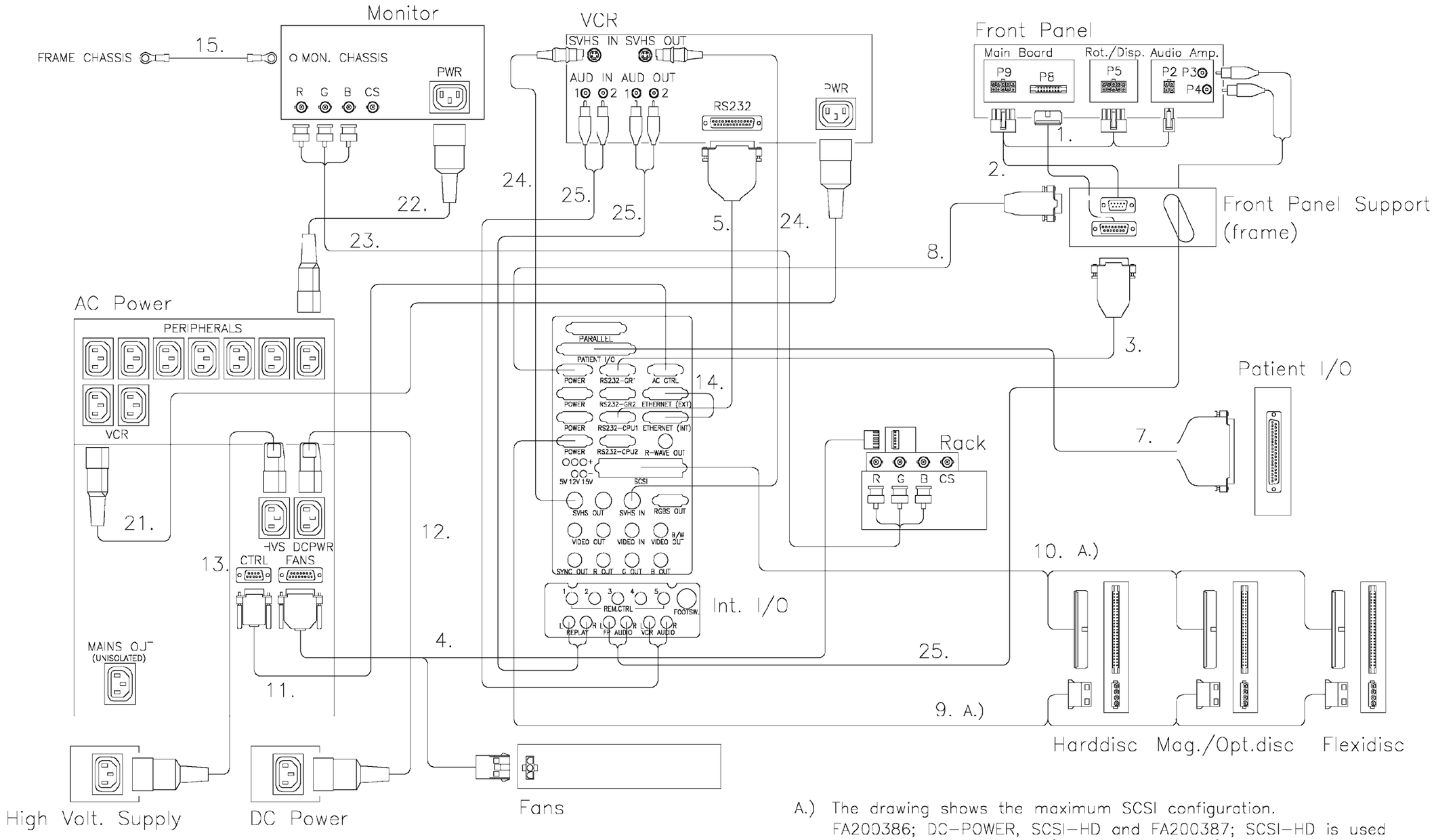
Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
Internal Cable Harness – rev. E	C1-2
Cable Harness - MAC – rev. B	C1-3
Cable Harness - MAC Elite, FA204727 rev. C	C1-4
Cable Harness - MAC Elite, FA204864 rev. A	C1-5
S5-EchoPAC Transfer Kit – rev. A	C1-6

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:C1_01_Cables.02.
Printed: December 5, 2000.

1 Internal Cable Harness – rev. E



1. FA200078; FP Ctrl, Internal.
2. FA200079; FP Power, Internal.
3. FA200081; FP Ctrl, External.
4. FA200147; Temp.Sense & Fan.
5. FA200155; VCR Control.
7. FA200634; Patient I/O Ctrl.
8. FA200282; FP Power, External.
9. FA200297; DC–Power, SCSI–discs. A.)
10. FA200298; SCSI – discs. A.)
11. FA200312; AC–Ctrl.
12. FA200313; Power, DC–Power.
13. FA200318; Power, HV–Supply.
14. FA200370; Ethernet Jumper
15. FA200507; Monitor GND.

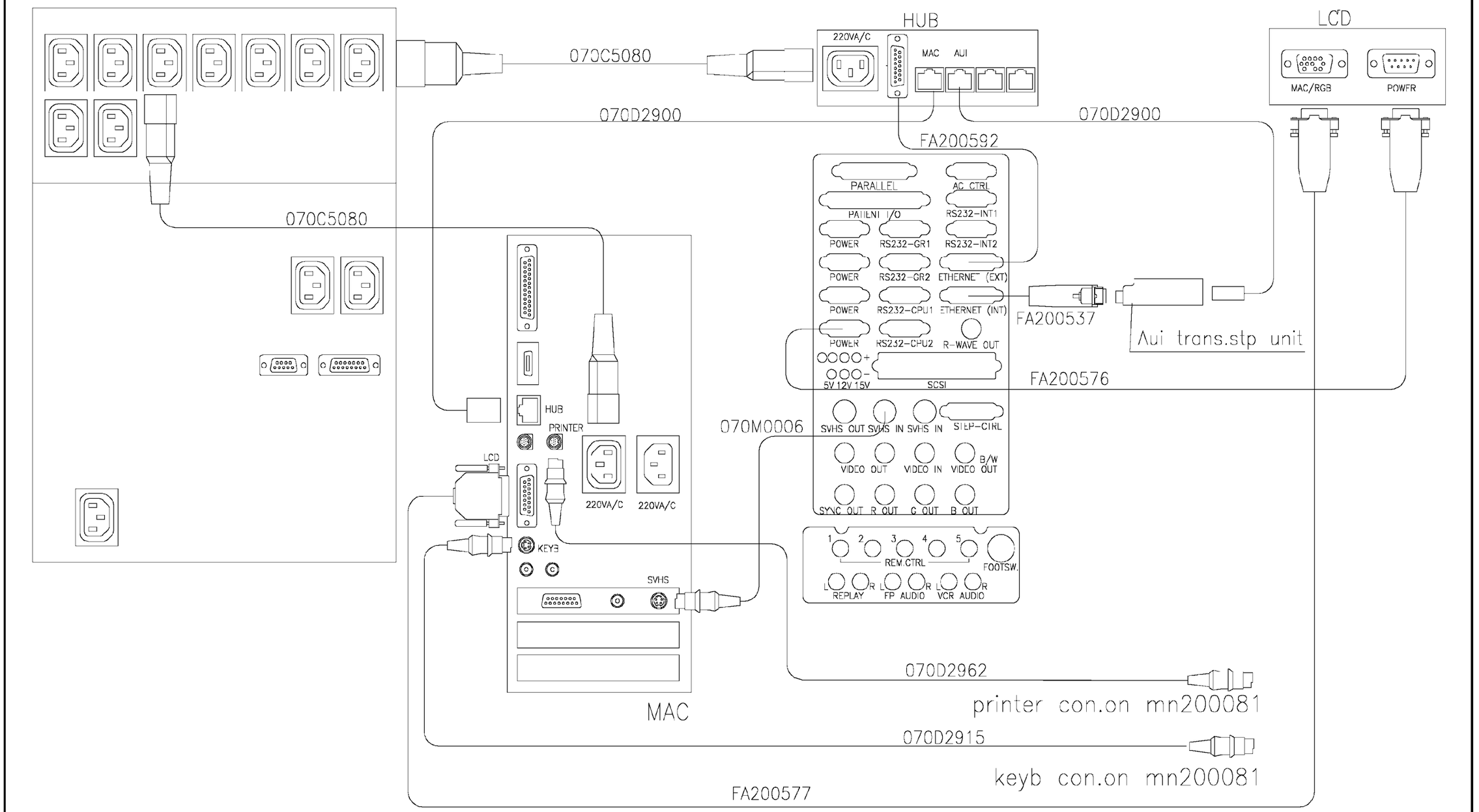
21. C70C5140; Mains, Shielded, 1.40m.
22. C70C5205; Mains, Shielded, 2.05m.
23. C70M0005; Signal, RGB
24. C70M0006; Signal, Shielded, Video.
25. C70M0007; Shielded w/Phono Conn.

A.) The drawing shows the maximum SCSI configuration. FA200386; DC–POWER, SCSI–HD and FA200387; SCSI–HD is used as standard configuration.(Single SCSI–device.)

VINGMED SOUND			MODULE NAME: CABLE HARNESS, INT.	
BY ØT	DATE 21.Mai.97	SIGN On File	TYPE OF DOC. WIR. DIAGR.	CLASSIF CATION
CHECKED SØ	DATE On File	SIGN On File	MODULE NO. FA201160	REV. E
APPROVED KB	DATE On File	SIGN On File		
TOLERANCE		SCALE	FILE FA160_E.DWG	SHEET 1 OF 1

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:C1_02_Cabl_Harn.02.
Printed: December 5, 2000.

2 Cable Harness - MAC – rev. B



REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
B	Mac. computer changed to modell 7300.		3.Nov.97	SØ
A	First rev s5 supervision		On File	ØT

VINGMED SOUND

BY SØ	DATE 3.Nov.97	SIGN On File
CHECKED KAB	DATE On File	SIGN On File
APPROVED KB	DATE On File	SIGN On File
TOLERANCE		SCALE

MODULE NAME: CABLE HARNESS, MAC

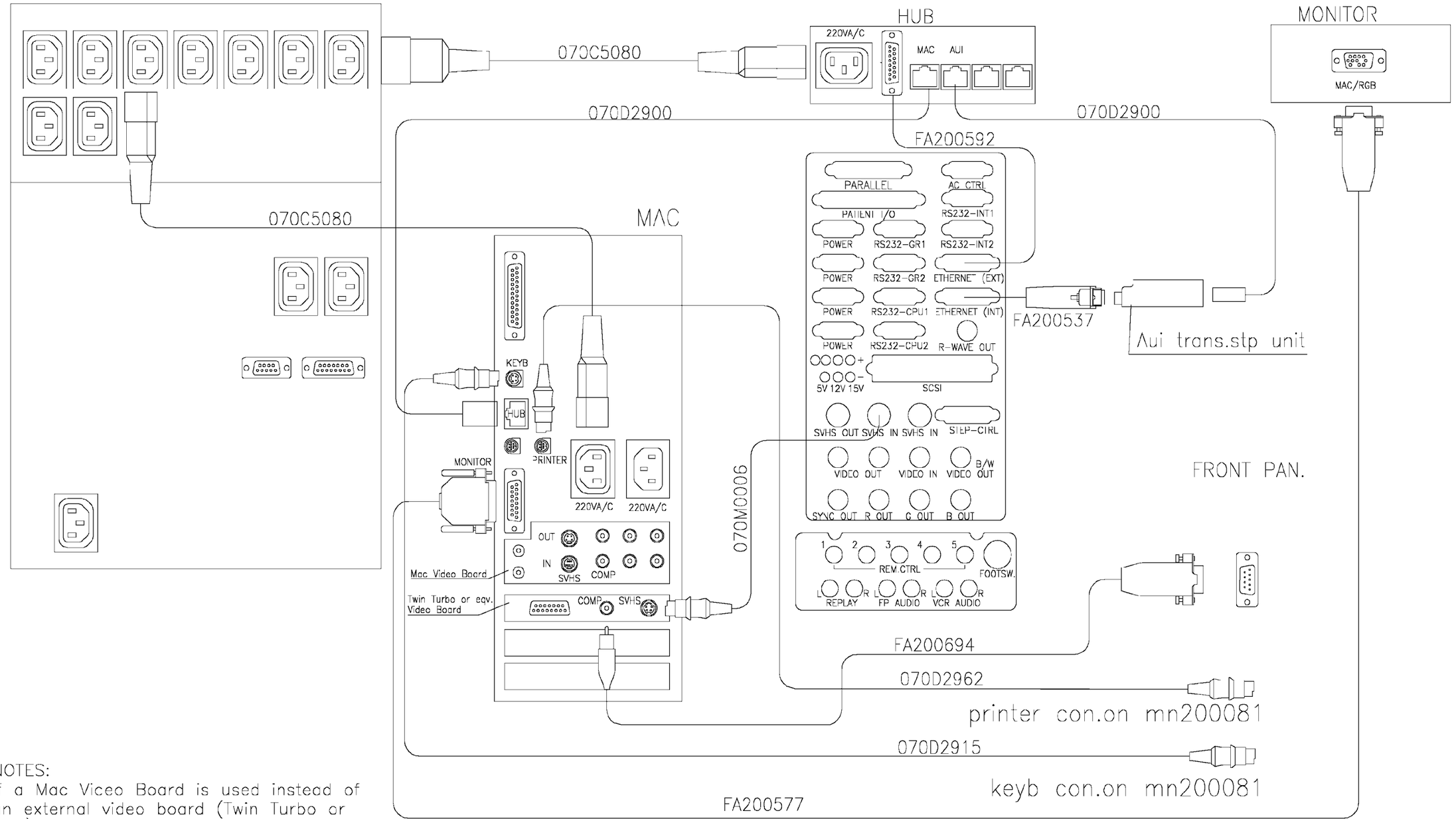
TYPE OF DOC.: WIR. DIAGR. | CLASSIFICATION:

MODULE NO.: FA204609 | REV.: B

FILE: FA609_B.DWG | SHEET 1 OF 1

Macintosh HD:User:James:@-arb:Service:S5_ServiceMan:S5_serv_files:C1_03_Cabl_H_MAC.01.
Printed: December 5, 2000.

Cable Harness - MAC Elite, FA204727 rev. C



NOTES:
If a Mac Viceo Board is used instead of an external video board (Twin Turbo or eqv.), cable A. and B. has to be connected to COMP– and SVHS–OUT on the Mac board.

REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
C	Mac. computer changed to modell G3.		6.Feb.98	SØ
B	Mac. computer changed to modell 7300.		3.Nov.97	SØ
A	First rev s5 supervision		On File	ØT

VINGMED SOUND

BY SØ	DATE 3.Nov.97	SIGN On File	
CHECKED KAB	DATE On File	SIGN On File	
APPROVED KB	DATE On File	SIGN On File	
TOLERANCE		SCALE	

MODULE NAME: CABLE HARNESS, MAC ELITE

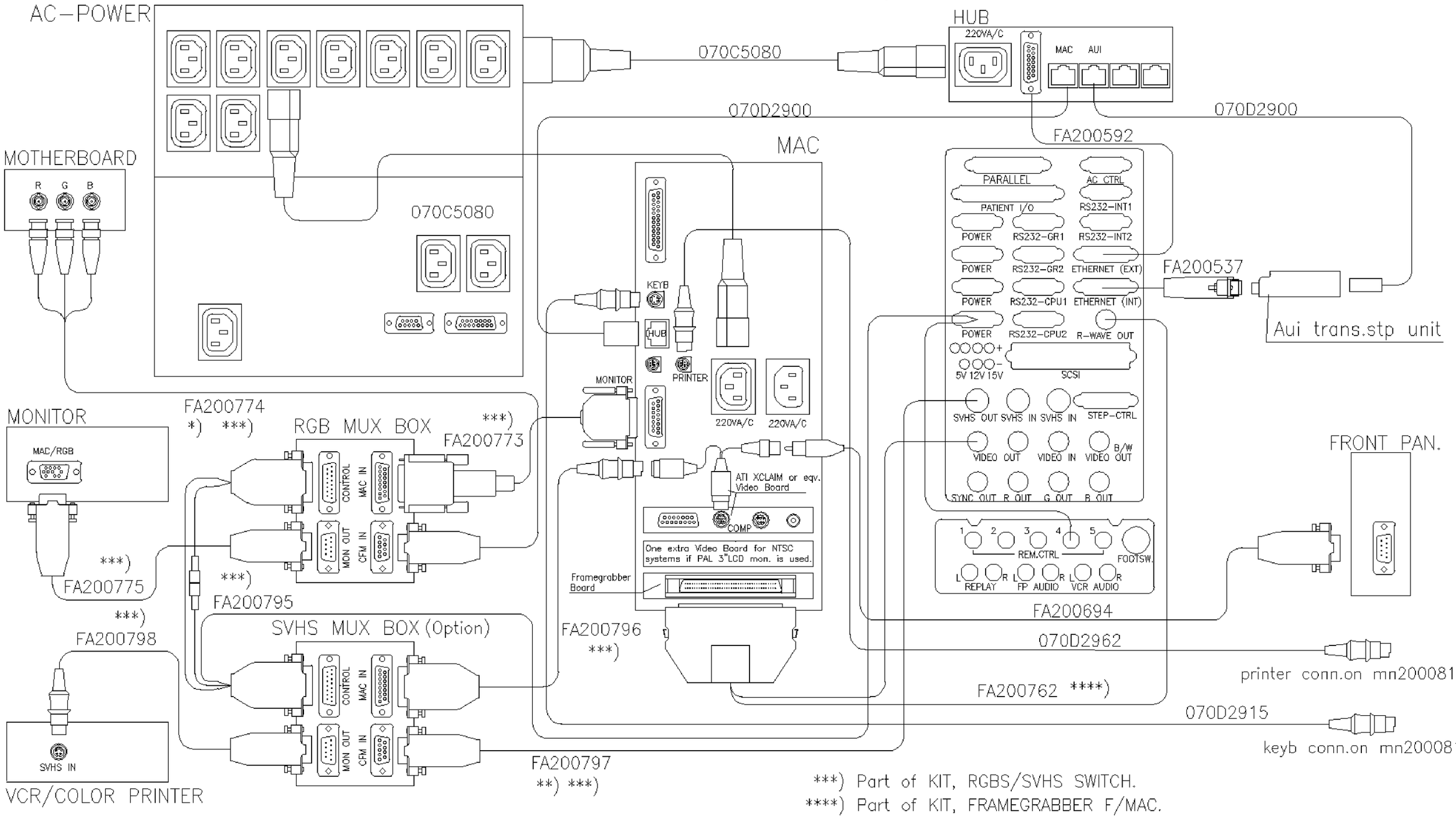
TYPE OF DOC.: WIR. DIAGR. | CLASSIFICATION:

MODULE NO.: FA204727 | REV.: C

FILE: FA727_C.DWG | SHEET 1 OF 1

Macintosh HD:User:James:@i-ash:Service:S5_ServiceMan:S5_serv_files:C1_04_Cabl_H_MAC_Elit.01.
Printed: December 5, 2000.

Cable Harness - MAC Elite, FA204864 rev. A



***) Part of KIT, RGBS/SVHS SWITCH.
****) Part of KIT, FRAMEGRABBER F/MAC.

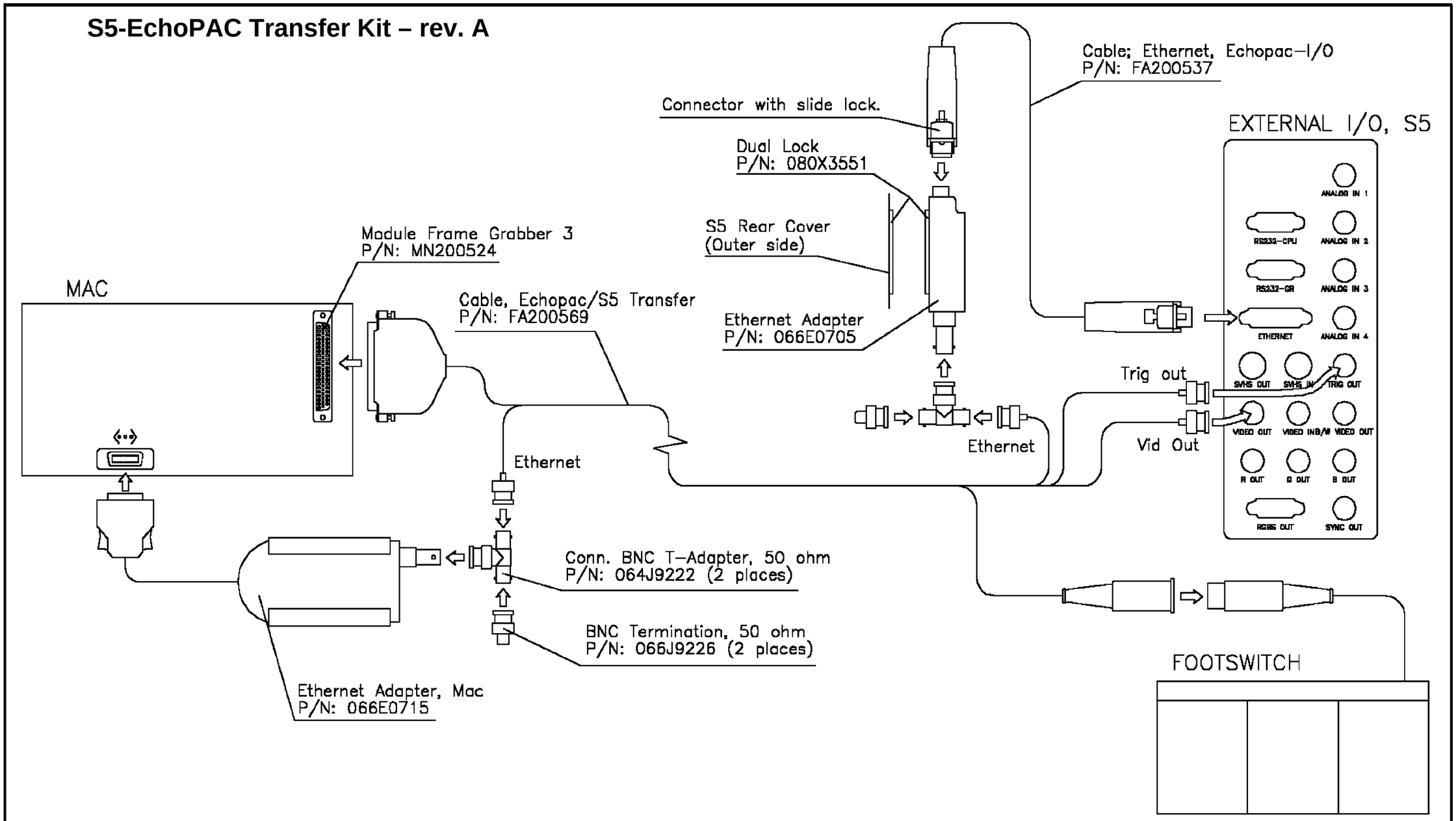
*) FA200774 will replace the RGB cable between MBD. and MON. in S5 Cable Harness.
**) FA200797 will replace the SVHS cable between I/Oout and VCRin in S5 Cable Harness.

REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
A	New P/N for cable harn. RGB/SVHS Mux and Framegrabber impl.		18sep98	SØ

VINGMED SOUND			MODULE NAME: CABLE HARNESS, MAC ELITE
BY: SØ	DATE: 18sep98	SIGN: On File	TYPE OF DOC.: WIR. DIAGR. / CLASSIFICATION:
CHECKED: KAB	DATE: On File	SIGN: On File	MODULE NO.: FA204864 / REV.: A
APPROVED: KB	DATE: On File	SIGN: On File	
TOLERANCE		SCALE	FILE: FA864_A.DWG / SHEET 1 OF 1

Macintosh HD:User James:@i-art:Service:S5_serv_files:C1_045_Cabl_H_MAC_Elite.01.
Printed: December 5, 2000.

S5-EchoPAC Transfer Kit – rev. A



VINGMED SOUND			MODULE NAME ECHOPAC/S5 TRANSFER KIT	
BY KAM	DATE 26Mai97	SIGN On file	TYPE OF DOC. WIR. DIAGR.	CLASSIFICATION
CHECKED KAB	DATE On file	SIGN On file	MODULE NO. FA204621	REV. A
APPROVED	DATE On file	SIGN On file		
TOLERANCE		SCALE	FILE FA621_A.dwg	SHEET 1 OF 1

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:C1_05_S5_EP_Trnsfer.fk 01.
Printed: December 5, 2000.

SYSTEM FIVE Power

Overview

Introduction

This part of the Service Manual describes the cables in SYSTEM FIVE .

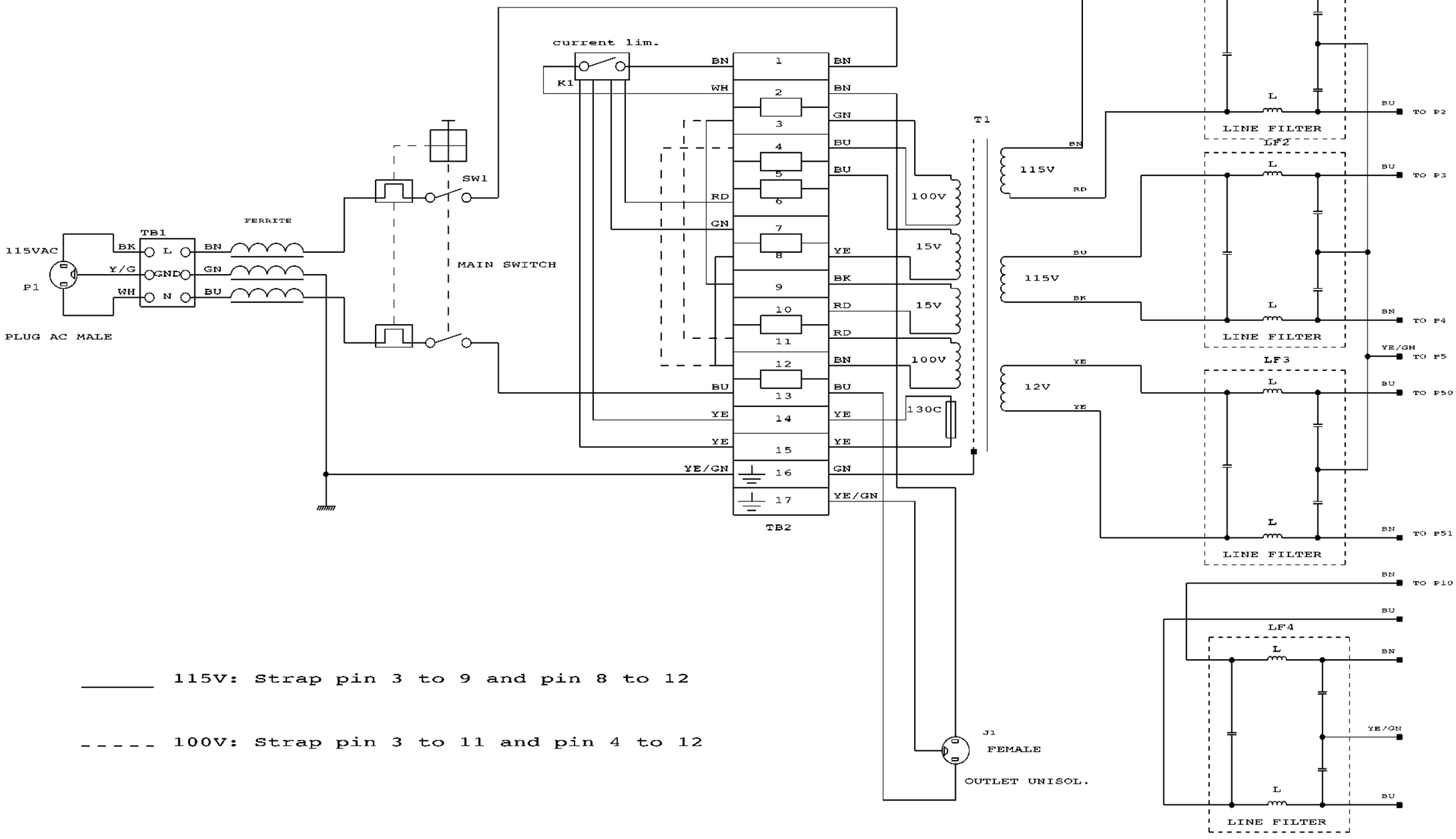
Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
AC Power, 115VAC – rev. 01	C2-2
AC Power, 230VAC – rev. 03	C2-3
Current Limiter & Temperature Switch – rev. B	C2-4

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:C2_00_Power.
Printed: December 5, 2000.

1 AC Power, 115VAC – rev. 01



_____ 115V: Strap pin 3 to 9 and pin 8 to 12

_ _ _ _ _ 100V: Strap pin 3 to 11 and pin 4 to 12

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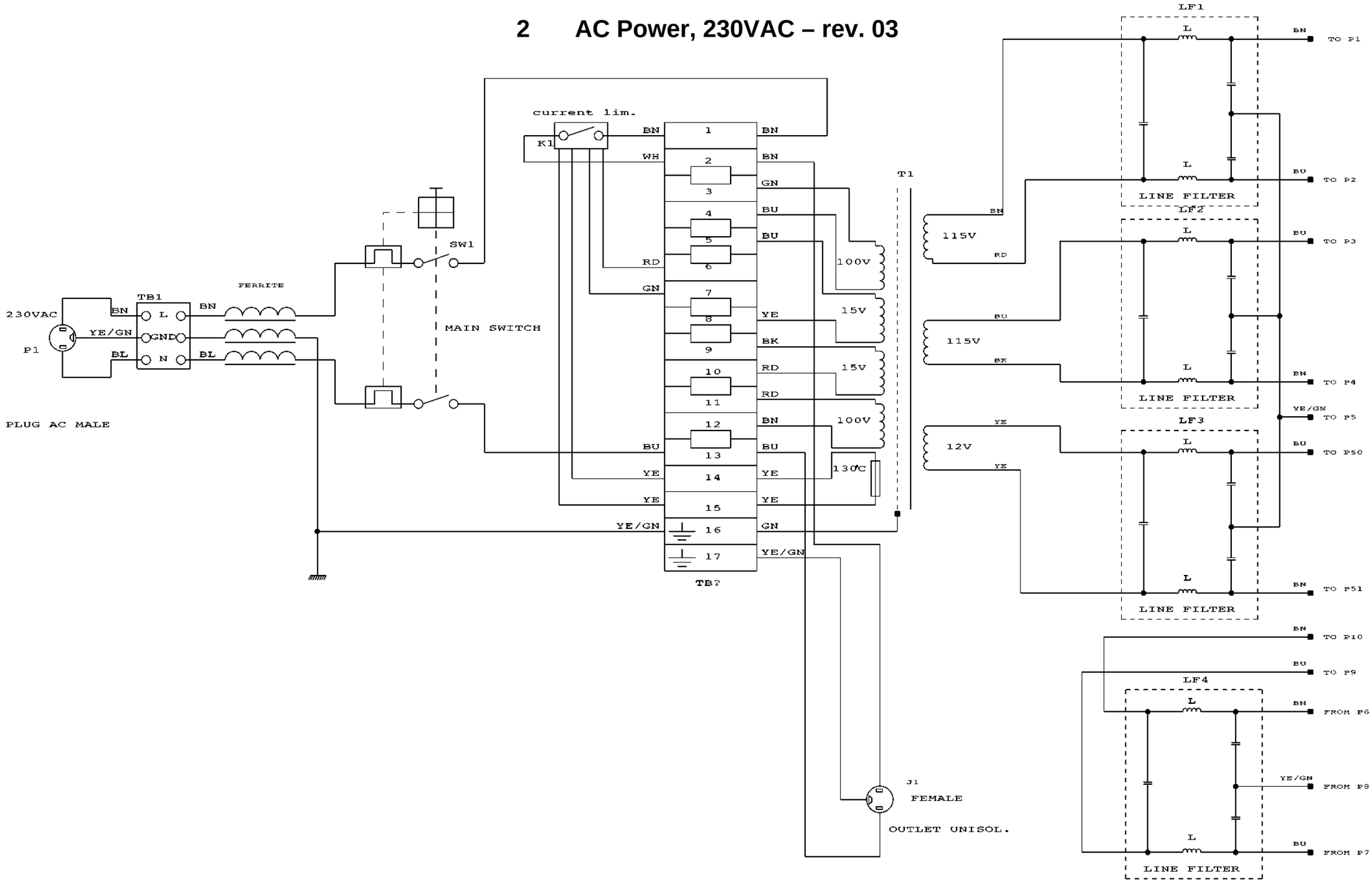
VINGMED Sound			MODULE ACPOWER 115V		PROJECT SYSTEM 5
DESIGNER GRT.	DATE 7 JAN. 97	SIGN	TYPE OF DOC CD	CLASSIFICATION QA	
CHECKED GRT.	DATE ON FILE	SIGN	PART NUMBER FA201231		REV 1
APPROVED KB	DATE ON FILE	SIGN			
SCALE	FILE /AC115_01.1				SHEET 1 OF 1

Macintosh HD:User:James:@-arb:Service:5S_ServiceMan:5S_serv_files:C2_01_AC_Pwr_115.02.
Printed: December 5, 2000.

2 AC Power, 230VAC – rev. 03



VINGMED sound			MODULE ACPOWER 230V	PROJECT SYSTEM 5
DESIGNER GJ	DATE 7 JAN. 92	SIGN	TYPE OF DOC CD	CLASSIFICATION
CHECKED GRL	DATE ON FILE	SIGN	PART NUMBER FA201040	REV 03
APPROVED KB	DATE ON FILE	SIGN		
SCALE	FILE -/AC230_03.1			SHEET 1 OF 1

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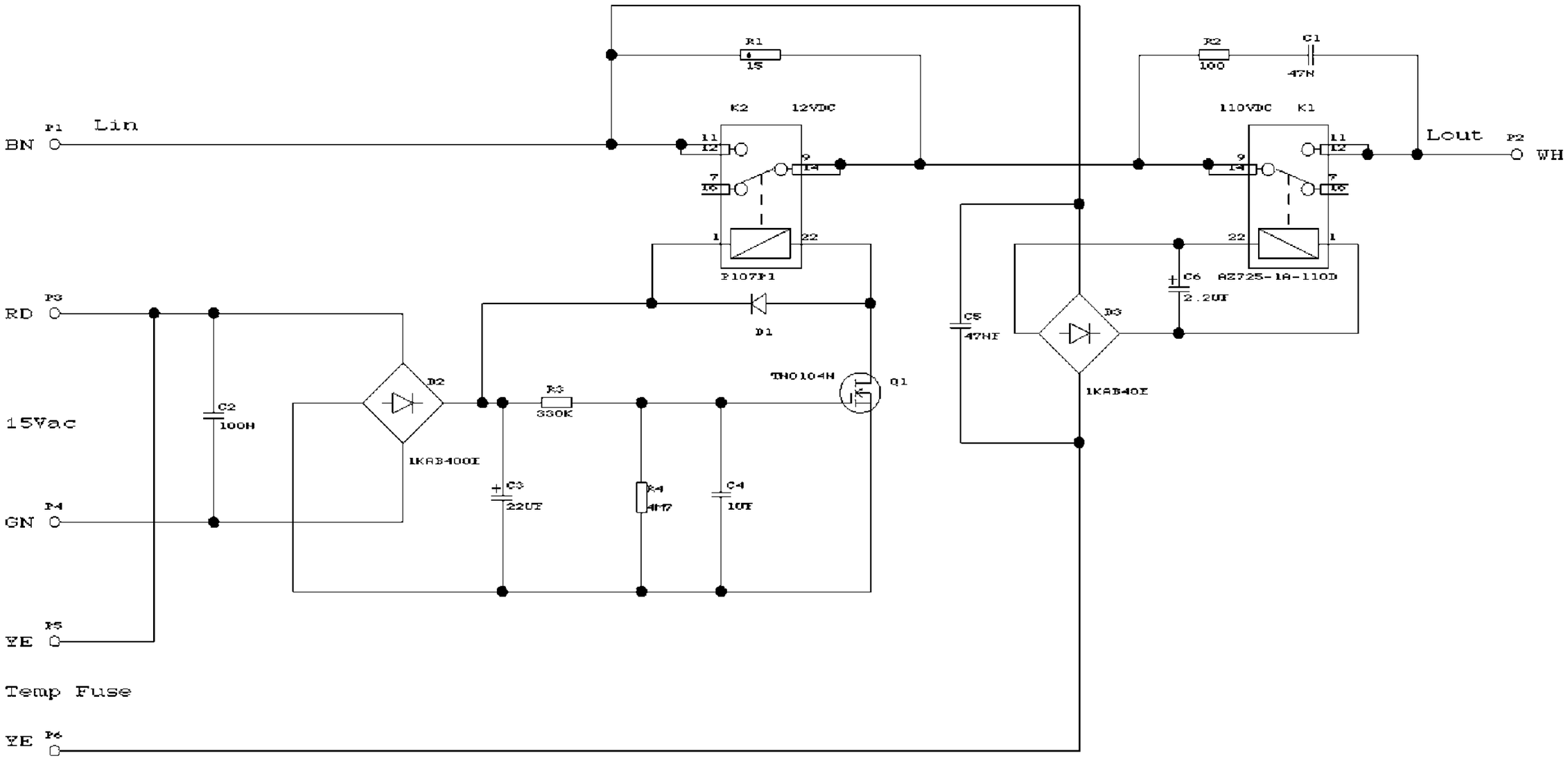
Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:C2_02_AC_Pwr_230.02.
Printed: December 5, 2000.

3 Current Limiter & Temperature Switch – rev. B



VINGMED sound			MODULE: CURRENT LIMITER & TEMP. SWITCH		PROJECT: SYSTEM 5
DESIGNER: GJ	DATE: 24 JUNE 1996	SIGN	TYPE OF DOC: CD	CLASSIFICATION	
CHECKED: GRL	DATE: ON FILE	SIGN	PART NUMBER: FA201558		REV: B
APPROVED: KF	DATE: ON FILE	SIGN			
SCALE	FILE: CURRLIM_B.1				SHEET: 1 or 1

Macintosh HD:User:James:@:ram:Service:SS_ServiceMan:SS_serv_files:C2_03_Cur_Lim.02.
Printed: December 5, 2000.

SYSTEM FIVE Mechanics

Overview

Introduction

This part of the Service Manual describes the Mechanics in SYSTEM FIVE .

Table of Contents

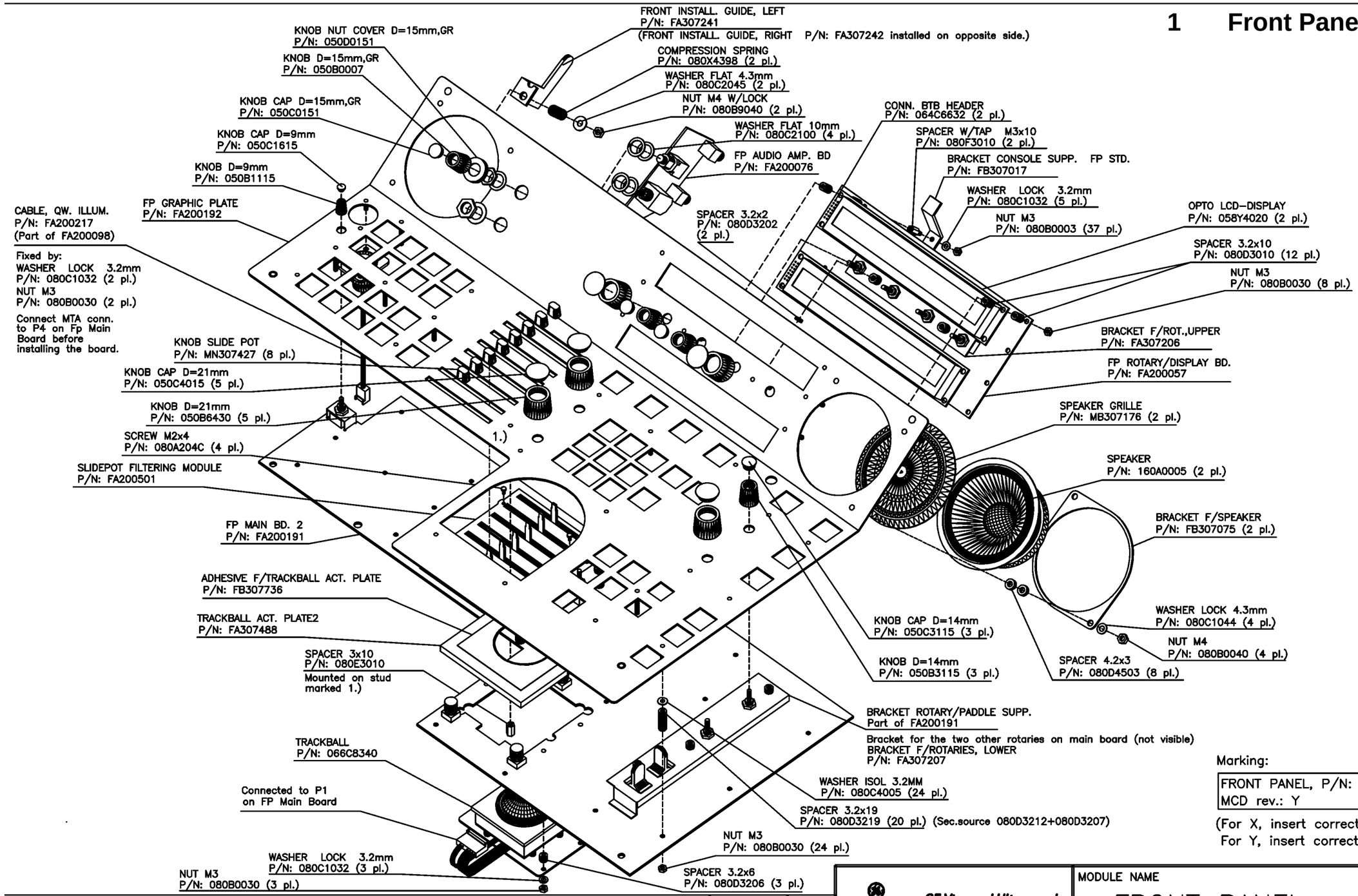
This table gives you an overview for this part of the Service Manual:

Contents	Page
Front Panel	D-3
Front Panel w/LCD display	D-4
Keyboard Subassembly - rev. A	D-5
Internal I/O Subassembly - rev. A	D-6
Extern I/O Subassembly - rev. A	D-7

Macintosh HD:User:James:@i-arts:Service:S5_ServiceMan:S5_serv_files:D_01_Mechanics.
Printed: December 5, 2000.

Empty page.

1 Front Panel



Marking:

FRONT PANEL, P/N: FA200045-X
MCD rev.: Y

(For X, insert correct language index.
For Y, insert correct MCD rev.)

REV.	REVISION DESCRIPTION	DATE	DRAFT BY
0	Adhesive for trackball plate added. Updating of drawing.	3.July00	SØ
N	Mounting instruction for speaker brackets changed due to new bracket version.	5.June00	SØ
M	Change of trackball (new p/n: 066C8340).	27.Apr.00	SØ
L	Moved spacer (mounted on stud marked 1).	6.Dec.99	CM

GE Vingmed Ultrasound

BY SØ	DATE 3.July00	SIGN
CHECKED ØT	DATE 3.July00	SIGN
APPROVED KB	DATE 3.July00	SIGN
TOLERANCE		SCALE

MODULE NAME: FRONT PANEL

TYPE OF DOC.: AP/A3

CLASSIFICATION:

MODULE NO.: FA209045

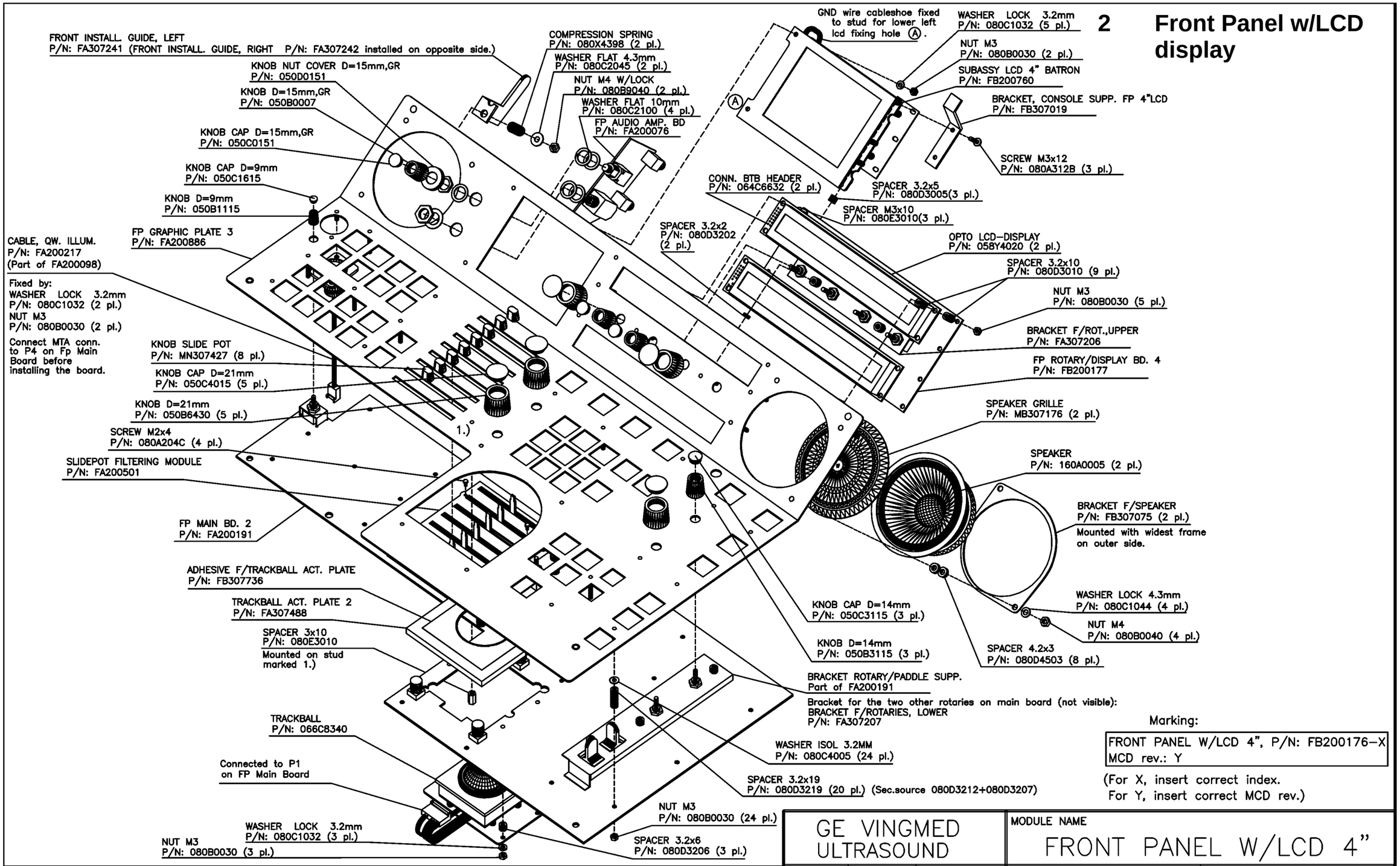
REV.: 0

FILE: fa045_o.dwg

SHEET 1 OF 1

Macintosh HD:User:James:@k-arb:Service:S5_service:Main:S5_serv_files:D_02_Front_Panel:03.
Printed: December 5, 2000.

2 Front Panel w/LCD display



Marking:

FRONT PANEL W/LCD 4", P/N: FB200176-X
MCD rev.: Y

(For X, insert correct index.
For Y, insert correct MCD rev.)

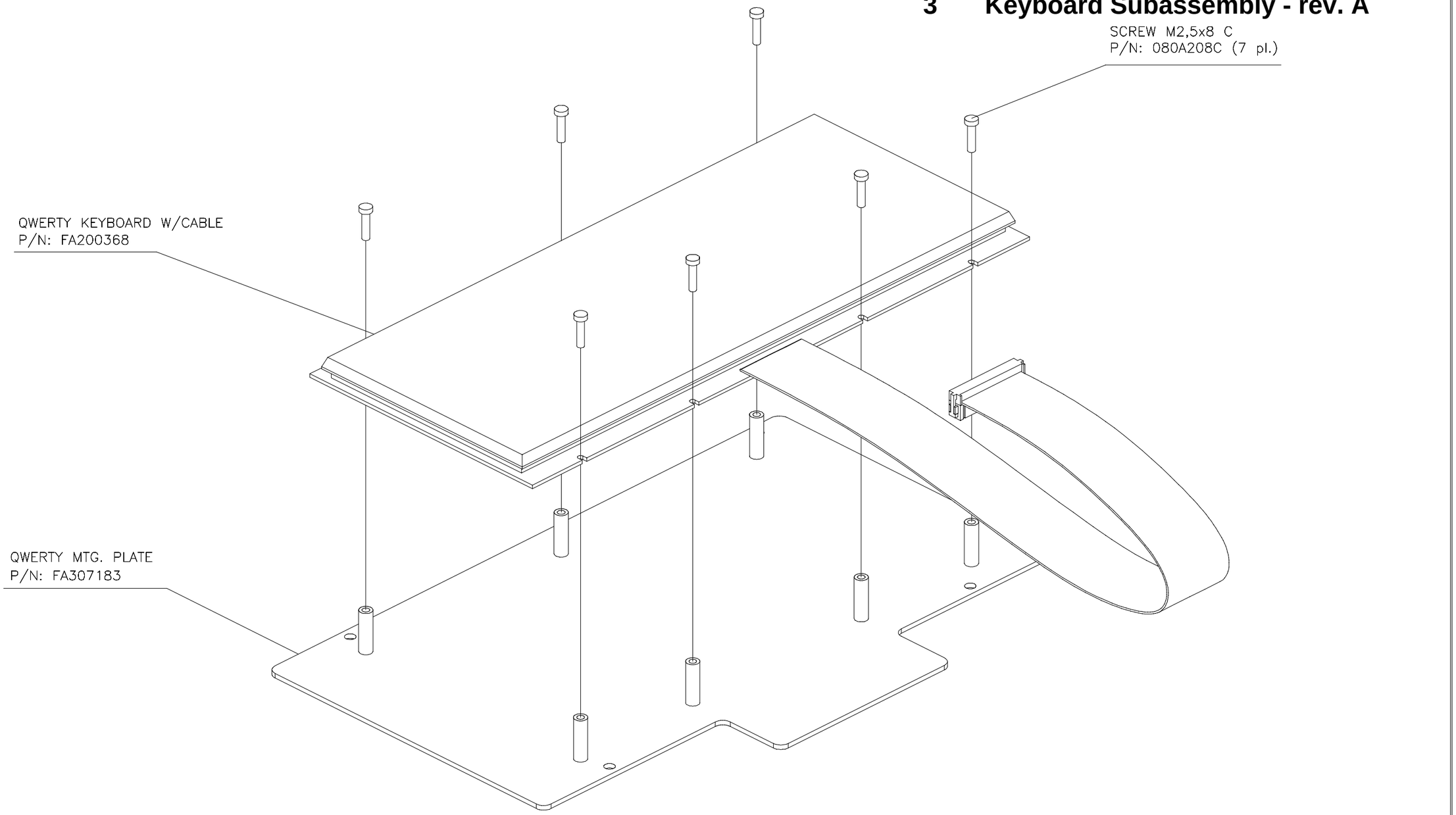
REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
D	Change LCD 4" to new type (Batron).		23aug00	SØ
C	Adhesive for trackball plate introduced. Drawing updated.		3July00	SØ
B	Change of trackball (new p/n: 066C8340).		28Apr00	SØ

GE VINGMED ULTRASOUND			
BY SØ	DATE 23aug00	SIGN	
CHECKED JTT	DATE 24aug00	SIGN	
APPROVED KB	DATE 24aug00	SIGN	
TOLERANCE		SCALE	

MODULE NAME	FRONT PANEL W/LCD 4"
TYPE OF DOC. ASSEMBLY PROC.	CLASSIFICATION
MODULE NO. FB209176	REV. D
FILE fb176_d.dwg	SHEET 1 OF 1

Macintosh HD:User:James:@:earb:Service:SS_ServiceMan:SS_serv_files:D_03_Keyboard.01.
Printed: December 5, 2000.

3 Keyboard Subassembly - rev. A



REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
B	New keyboard from CHERRY implemented.			SØ
A	First revision.			SØ

VINGMED SOUND

BY	DATE	SIGN
SØ	26APR.95	ON FILE
CHECKED MH	DATE ON FILE	SIGN ON FILE
APPROVED KB	DATE ON FILE	SIGN ON FILE
TOLERANCE		SCALE

MODULE NAME: QWERTY KEYBD. SUBASSY.

TYPE OF DOC.: ASSY PROC.

CLASSIFICATION:

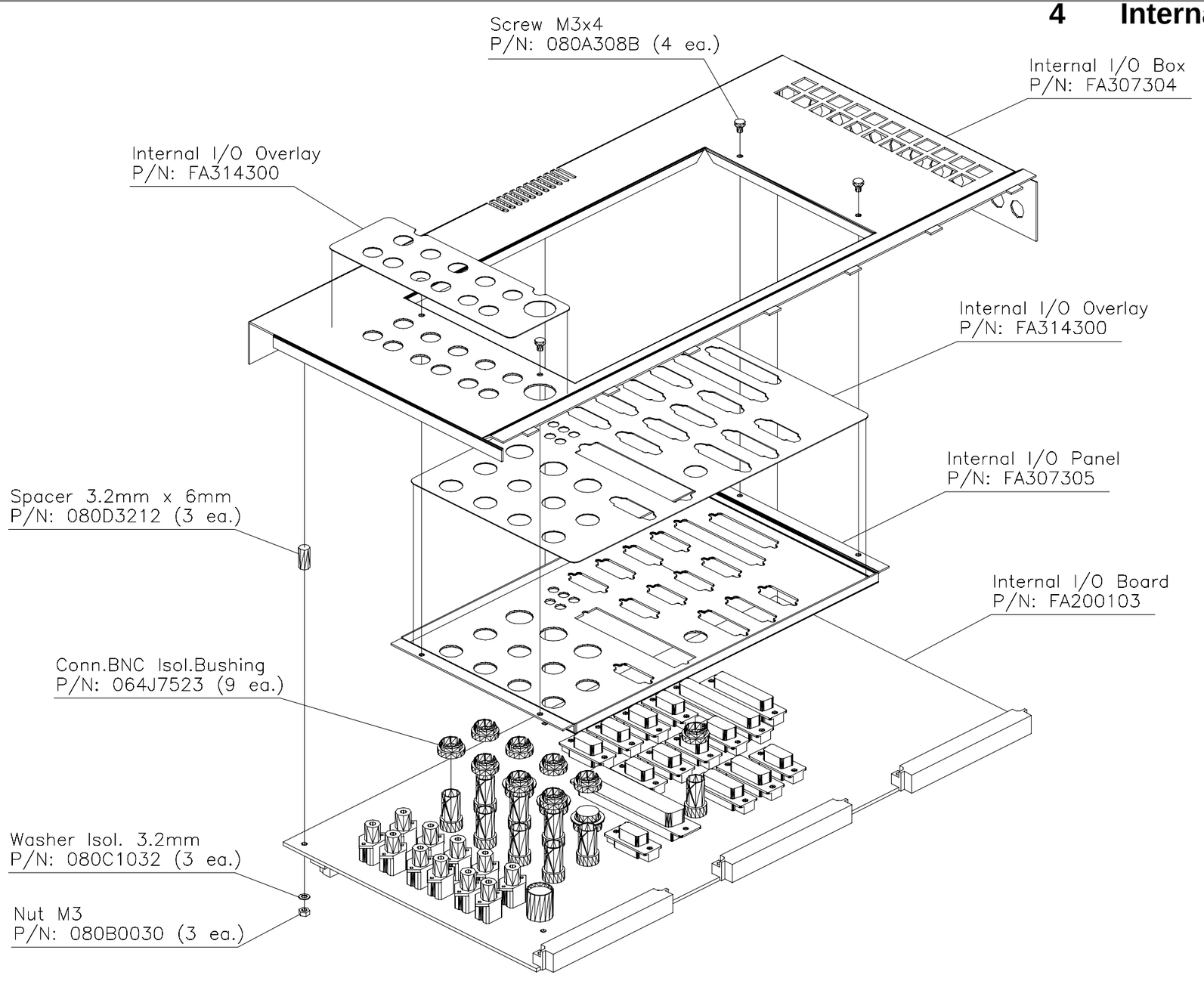
MODULE NO.: 330 FA209360

REV.: B

FILE: FA360_B.DWG

SHEET 1 OF 1

4 Internal I/O Subassembly - rev. A

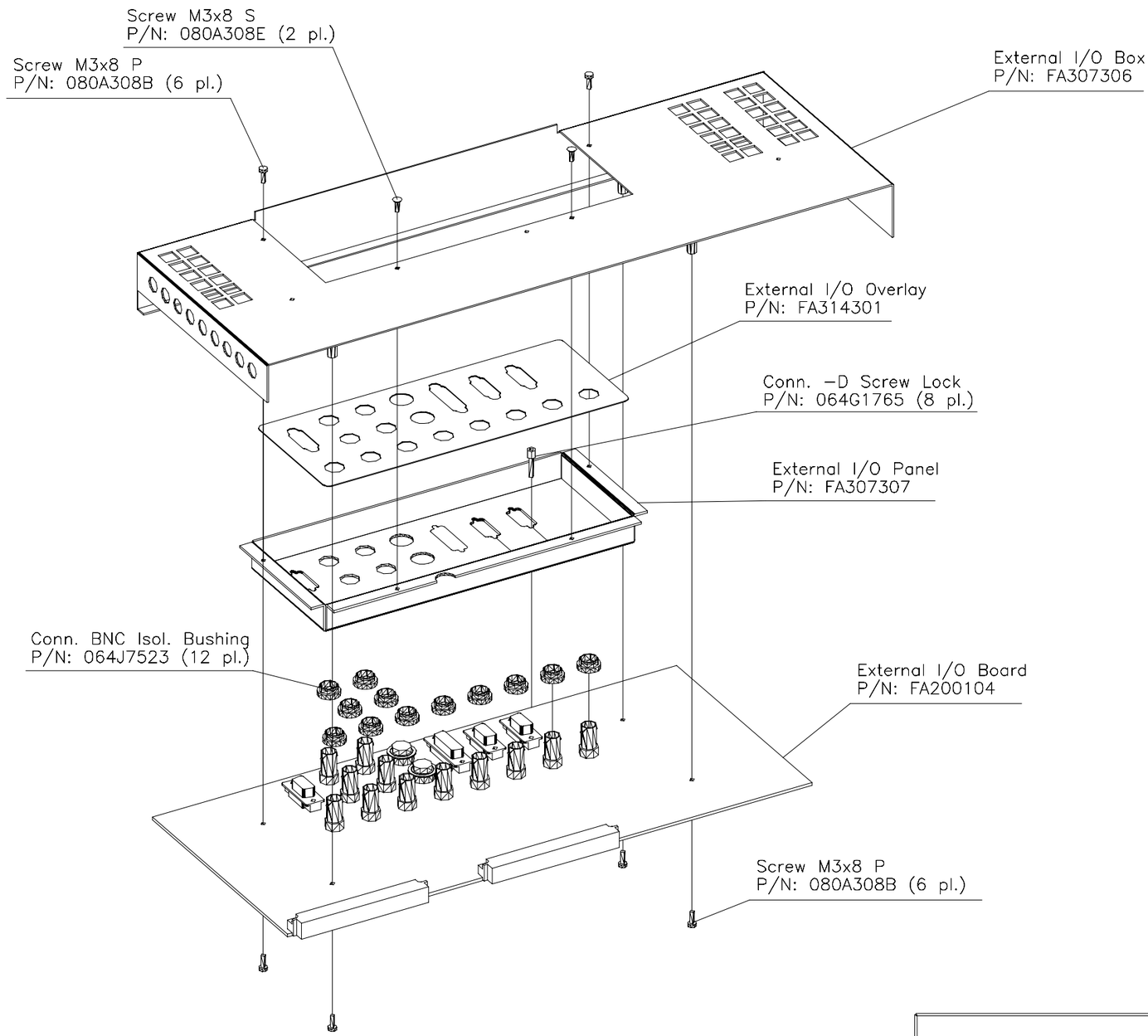


REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
A	Doc. release.			SØ

VINGMED SOUND			MODULE NAME: INTERNAL I/O SUBASSY
BY: SØ	DATE: 5apr.95	SIGN:	TYPE OF DOC.: ASSY PROC. / CLASSIFICATION:
CHECKED: GJ	DATE:	SIGN:	MODULE NO.: 330 FA209115 / REV.: A
APPROVED: KB	DATE:	SIGN:	
TOLERANCE:		SCALE:	FILE: FA115_A.DWG / SHEET 1 OF 1

Macintosh HD:User:James:@i-ath:Service:S5_ServiceMan:S5_serv_files:D_04_Intern_IO.01.
Printed: December 5, 2000.

5 Extern I/O Subassembly - rev. A



REV.	REVISION DESCRIPTION	AP"D BY	DATE	DRAFT BY
A	First Revision.		21.FEB95	SO

VINGMED SOUND

BY	DATE	SIGN
SO	21.FEB95	
CHECKED	DATE	SIGN
APPROVED	DATE	SIGN
TOLERANCE		SCALE

MODULE NAME: EXTERNAL I/O SUBASSY

TYPE OF DOC.: ASSY. PROC.

CLASSIFICATION:

MODULE NO.: 330 FA209116

REV.: A

FILE:

SHEET 1 OF 1

Macintosh HD:User:James:@i-arb:Service:SS_ServiceMan:SS_serv_files:D_05_Extern_IO.01.
Printed: December 5, 2000.

SYSTEM FIVE Probes

Overview

Introduction

This part of the Service Manual describes probes for use on SYSTEM FIVE.

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
• Mechanical Steered Probes • Annular Phased Array Transducer (APAT) • Electronically Steered Probes • Doppler Probes	E1-2 E1-2 E1-3 E1-5

• Probes
• Probe Support List – rev. 13
  • Flat Phased Array (FPA) Probes:
  • Flat Linear Array (FLA) Probes:
  • Curved Linear Array (CLA) Probes:
  • TV Probes:
  • FPA MPTE Probes:
  • APA Probes:
  • Doppler Probes:
	E2-1
	E2-1
	E2-3
	E2-3
	E2-3
	E2-3
	E2-4
	E2-4
	E2-4

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:E0_01_Innh.04.
Printed: December 5, 2000.

Your Notes:

Probes - rev. 05

1 Overview

1.1 Abstract

This document describes the probes that can be used on the SYSTEM FIVE.

2 Document History

Table 1: Document History.

Revision	Date	By	Description
01	21 Mar 1994	ALO	Initial release.
02	10 Oct 1996	HH/lhs	Updated layout, corrected spelling/ typing errors, removed unsupported probes, added new probes.
03	11 Oct 1996	LHS	Updated
04	9. Sep 1999	EAT/HH/ lhs	Updated contents per v.1.8 release (Added several probes)
05	14. Dec. 1999	LHS	Added one probe, KW100004 per v.1.9 release.
06	02.Nov.00	JB	Changed Probe frequency from 5 to 8

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:E1_02_Probes.05.
Printed: December 5, 2000.

3 Mechanical Steered Probes

3.1 Annular Phased Array Transducer (APAT)

Part Number, Frequency and Color Code on the APAT probes used on SYSTEM FIVE are listed below.

Table 2: APAT probes

P/N	Name	ID Resistor	Color Code
TG100102	2.5 MHz	2k2	Red
TK100104	3.25MHz	6k8	Blue
TN100119	5 MHz	10k	Black
TT100101	7.5MHz	15k	Orange

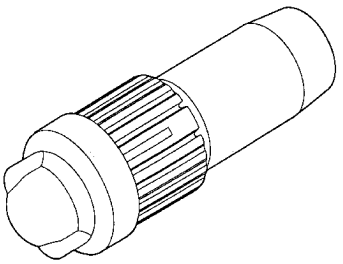


Fig. 3.1 APAT probe.

3.2 PV Probe

Table 3: PV probe

P/N	Name	ID Resistor
TT100109	7.5 MHz PV	33k

3.3 Transvaginal Probe

Table 4: Transvaginal probe

P/N	Name	ID Resistor
TN100124	5 MHz TV	1k5

3.4 Transesophageal Probes (TEE)

Table 5: TEE probes

P/N	Name	Tip	Endoscop	ID Resistor
TN100047	5MHz Adult/ Monoplane	15.5 mm	ACMI PUR	100k
TN100053	5MHz Adult/ Multiplane	15.5 mm	ACMI PUR	220k
TN100065	PMPTE	10.5 mm	ACMI PUR	560k

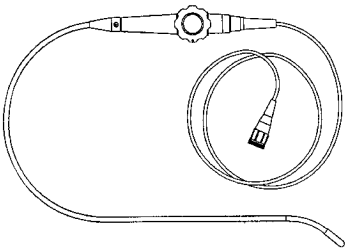


Fig. 3.2 TEE probe

4 Electronically Steered Probes

4.1 Phased Array

Table 6: Phased Array Probes

P/N	Frequency	# Elements	Footprint
KG100001	2.5 MHz	64	21*17
KK100001	3.5 MHz	96	21*17
KK100005	3.5 MHz	96	21*17
KN100001	5.0 MHz	128	21*17
KN100002	5.0 MHz	96	21*15
KW100002	10 MHz	96	14*10

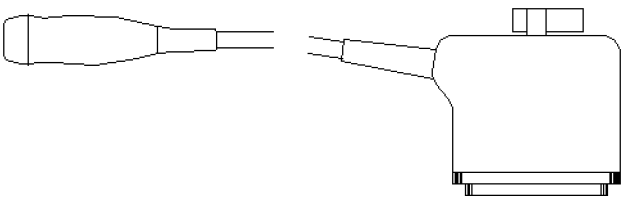


Fig. 4.1 Phased Array probe

4.2 Linear Array

Table 7: Linear Array Probes

P/N	Frequency	# Elements	Footprint
KN100003	5.0 MHz	192	60*17
KT100001	7.5 MHz	192	50*17
KW100001	10.0 MHz	192	50*17
KW100004	10.0 MHz	192	50*17

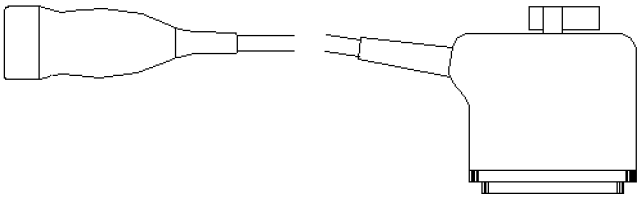


Fig. 4.2 Linear Array probe

4.3 Curved Linear Array

Table 8: Curved Linear Array Probes

P/N	Frequency	Radius of curvature	Field of view	# Elements
KK100004	3.5 MHz	40	85°	192
KN100008	5.0 MHz	40	68°	192

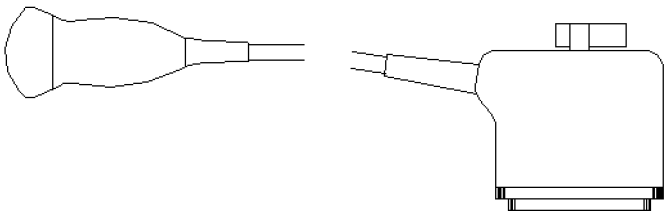


Fig. 4.3 Curved Linear Array Probe.

4.4 Transvaginal Probe

Table 9: Transvaginal Probe

P/N	Frequency	Radius of curvature	Field of view	# Elements
KQ100002	6.5 MHz	9	124°	128

4.5 Phased Array TE Probes

Table 10: Phased Array TE Probes

P/N	Frequency	# Elements	Tip	Endoscop
KN100006	5.0 MHz	64	14 mm	Storz
KN100007	5.0 MHz	64	14 mm	ACMI PUR
KN100010	8.0 MHz	48	10.7 mm	ACMI

4.6 Doppler Probes

Table 11: Doppler Probes

P/N	Name	Shape	ID Resis-tor
KE100001	2 MHz	Straight	5k6
TE100024	2 MHz	Angled Pen	3k9
TQ100002	6 MHz	Straight	150 k

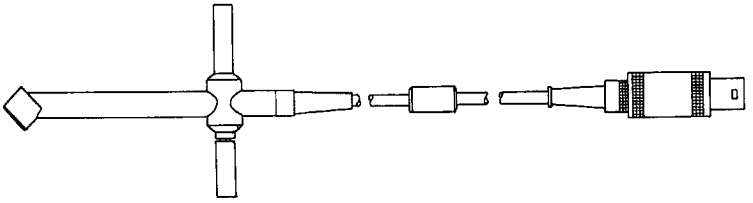


Fig. 4.4 Doppler Probe, Angled Pen.

Your Notes:

Probe Support List – rev. 13

1 Abstract

The purpose with this document is to give a listing of the probes which are supported by the different software versions:

2 Document History

Rev.	Date	By	Description
01	1 Aug 96	GRL	First version of document per V1.1 release
02	10 Oct 96	HH/LHS	Removed unsupported probes, added new probes, corrected errors
03	5 May 97	GRL	Updated per V1.2 release
04	23 Jun 97	GRL	Updated per V1.2.2 release.
05	17 Nov 97	GRL	Updated per V1.3 release.,
06	22 Dec 97	GRL	Updated per V1.3.1 release. New probes: KE100001: 2 MHz Tc probe KQ100002: 6.25 MHz TV probe KK100005: 3.5 MHz FPA (Diasonics)
07	30 Apr 98	GRL	Updated per V1.4 release. Redone the table to show probe support, history sorted by software level.
08	14 Oct 98	GRL	Updated per V1.5 and V1.5.1 release. Support for KN100006 PAMPTE probe.
09	21 Dec.98	GRL	Updated per V1.5.2 release. PAMPTE support on Membership
10	11 Jan 99	JK	Updated per V1.6 release. V1.6 has the same probe support as V1.5 and V1.5.1.
11	19.Aug.1999	JK	Updated per V1.7 release. Support for KW100002, Pediatric FPA probe
12	6. Sep. 1999	EAT/HH/lhs	Updated per v.1.8 release
13	3. Dec. 1999	LHS	Updated per v.1.9 release
14	02Nov.00	JB	Changed probe frequency from 5 to 8MHz

3 Probes

The table starting on Page E2-3 lists the available probes for System FiVe.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:E2_03_prb_list_a.13.
Printed: December 5, 2000.

Your Notes:

Probe Part number	Rev	ID	Probe Type and Description	v1.7/1.7.1	v1.8	v1.9
				Apr. 1999	Sep. 1999	Dec. 1999
Flat Phased Array (FPA) Probes:						
KG100001	A	2	2.5 MHz, 64 el.	P	P	P
KG100001	B	22	2.5 MHz, 64 el. (improved shielding, new mapping)	P,M,A	P,M,A	P,M,A
KG100001	C	49	2.5 MHz, 64 el. (new tuning)	P,M,A	P,M,A	P,M,A
KK100001	A	3	3.5 MHz, 96 el. Echo	P	P	P
KK100001	B C	35	3.5 MHz, 96 el. (new Xtal, new mapping), Echo	P,M,A	P,M,A	P,M,A
KK100005	A	34	3.5 MHz, 96 el., Diasonics	P,M,A	P,M,A	P,M,A
KN100001	A	5	5.0 MHz, 128 el.	P	P	P
KN100002	A	4	5.0 MHz, 96 el. (small)	P (not US)	P (not US)	P (not US)
KN100002	B	28	5.0 MHz, 96 el. (small, new mapping)	P,M	P,M	P,M
KW100002	A		10 MHz, 96 el.	P,M,Pe,A	P,M,Pe,A	P,M,Pe,A
Flat Linear Array (FLA) Probes:						
KN100003	A	9	5.0 MHz, 192 el	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
KT100001	A	10	7.5 MHz, 192 el.	Pe,P,M,A (not US)	Pe,P,M,A (not US)	Pe,P,M,A (not US)
KW100001	A	23	10 MHz, 192 el.	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
KW100004	A	59	10 MHz, 192 el.	NO	NO	Pe,P,M,A
Curved Linear Array (CLA) Probes:						
KK100004	A	17	3.5 MHz, 192 el.	Pe,P,M, A:Option	Pe,P,M, A:Option	Pe,P,M, A:Option
KN100008	A	18	5.0 MHz, 192 el.	Pe,P,M, A:Option	Pe,P,M, A:Option	Pe,P,M, A:Option
TV Probes:						
KQ100002	A	30	6.25 MHz, 128 el.	Pe,P,M, A:Option	Pe,P,M, A:Option	Pe,P,M, A:Option

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:E2_04_prb_list_b14.
Printed: December 5, 2000.

Probe Part number	Rev	ID	Probe Type and Description	v1.7/1.7.1	v1.8	v1.9
				Apr. 1999	Sep. 1999	Dec. 1999
FPA MPTE Probes:						
KN100006		13	5.0 MHz PAMPTE, Vingmed, 64 el.	P,M,A:Option	P,M,A:Option	P,M,A:Option
KN100007	A	14	5.0 MHz, Oldelft MTEE, 64 el.	Pe,P (not US)	Pe,P (not US)	Pe,P (not US)
KN100007	B	25	5.0 MHz, Oldelft MPTE, 64 el. (new orientation, new mapping)	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
KN100010	A	53	8.0 MHz, Oldelft Ped PAMPTE, 48 el.	NO	Pe,P,M,A	Pe,P,M,A
APA Probes:						
TG100102	-	6	2.25 MHz, APAT, 5el.	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
TK100104	-	12	3.25 MHz, APAT, 4 el.	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
TN100119	-	14	5.0 MHz, APAT, 4 el.	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
TT100101	-	16	7.5 MHz, APAT, 4 el.	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
APA TE Probes:						
TN100047	-	26	5 MHz adult TEE	Pe,P,M,A (not US)	Pe,P,M,A (not US)	Pe,P,M,A (not US)
TN100053	-	30	5 MHz, adult MTEE	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
TN100065	-	22	7.5 MHz, ped. MPTE	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
Doppler Probes:						
TE100024	-	8/9	2 MHz “Pedof” probe	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A
KE100001	-	10/11	2 MHz Trans Cranial probe (PW)	Pe,P,M (not US)	Pe,P,M (not US)	Pe,P,M (not US)
TQ100001	-	17/28	6 MHz Pencil probe	Pe,P,M,A	Pe,P,M,A	Pe,P,M,A

Explanation of probe support table

P ..... : means that the probe is supported on the Premium (256 channel) systems.
Pe ..... : means that the probe is supported on the Performance (256 channel) systems.
M ..... : means that the probe is supported on the Membership (128 channel) systems.
A ..... : means that the probe is supported on the Advantage (128 channel) systems.
APA..... : probes and APA TE probes are optional and support will depend on software type (aa or not).
US ..... : United States support (i.e. FDA approval)
NO ..... : means no support.

SYSTEM FIVE I/O signals

Overview

Introduction

This part of the Service Manual describes the peripherals and I/O signals in SYSTEM FIVE.

Table of Contents

This table gives you an overview for this part of the Service Manual:

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Printed: December 5, 2000.

Notes:

I/O Signals

1 Introduction

1.1 Abstract

This is a description of the input - and output connectors in System 5.

1.2 Document History

Rev.	Date	Sign.	Description
01	29 Aug 94	GRL	First version of document
02	28 Apr 95	GRL	Added voltages on conn. and drwg. of INT I/O & EXT I/O
03	9 Apr 96	GRL	Corrected INT I/O power connector voltages.
04	9 Aug 96	GRL	Made cross reference to Internal Cable Harness wiring diagram
05	30 Mar 99	LHS	Added updated illustration for the Int. I/O
06	June 00 Nove.00	LHS/ JB	Updated-Corrected Error. Removed IV Data

1.3 References

Wiring Diagram of Internal Cable Harness – rev. E on *page C1-2*.

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2 Patient I/O

2.1 ECG connector

Type of connector: 6 pin circular AMP.
Use: A 3-lead ECG cable can be connected to this input.

ECG Connector	
Pin	**Signal**
A	ELECTRODE_RA (right arm)
B	ELECTRODE_LA (left arm)
C	ELECTRODE_LL (left leg)
D	
E	
F	SHIELD

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Parameter	Min.	Typ.	Max.	Units
Gain	40.0	40.5	41.0	dB
Input Range	-25		25	mV
Bandwidth		1600		Hz
Input Impedance		2 * 33		MΩ
Input Noise Voltage (100 Hz)		30		nV/$\sqrt{Hz}$
Input Noise Current (100 Hz)		16		fA/$\sqrt{Hz}$
Common Mode Rejection (100 Hz)		100		dB

2.2 Phono connector:

Type of connector: 6.3 mm phono.

Use: A heart microphone can be connected to this input.

See Patient I/O assembly drawing for physical location of pins.

Phono Connector	
Pin	**Signal**
SLV	Sleeve: PHONO_GND
T	Tip: PHONO_HOT (non-inverting input)
T/S	PHONO_COLD (inverting input)
R	

2.3 Respiration connector:

Parameter	Min.	Typ.	Max.	Units
Gain	40.0	40.5	41.0	dB
Input Range	-25		25	mV
Bandwidth		1600		Hz
Input Impedance		2 * 3.3		MΩ
Input Noise Voltage (100 Hz)		12		nV/$\sqrt{Hz}$
Input Noise Current (100 Hz)		110		fA/$\sqrt{Hz}$
Common Mode Rejection (100 Hz)		120		dB

Type of connector: 6.3 mm phono.

Use: A respiration transducer can be connected to this input.

See Patient I/O assembly drawing for physical location of pins.

Respiration Connector	
Pin	**Signal**
SLV	Sleeve: Thermistor (high pot.)
T	Tip: Thermistor (low pot.)
T/S	
R	

Parameter	Min.	Typ.	Max.	Units
Nominal Bridge Resistance		10		kΩ
Bridge Sensitivity		250		µV/Ω
Bandwidth		160		Hz

2.4 Pressure connector:

Type of connector: 6.3 mm phono.

Use: A pressure transducer can be connected to this input.

See Patient I/O assembly drawing for physical location of pins.

Pressure Connector	
Pin	**Signal**
SLV	Sleeve: Shield
T	Tip: Pressure sensor input, non-inverting
T/S	Pressure sensor input, inverting
R	

Parameter	Min.	Typ.	Max.	Units
Gain	15.0	15.5	16.0	dB
Input Range	-420		+420	mV
Bandwidth		160		Hz
Input Impedance		2 * 100		MΩ
Input Noise Voltage (100 Hz)		30		nV/$\sqrt{Hz}$
Input Noise Current (100 Hz)		9		fA/$\sqrt{Hz}$
Common Mode Rejection (100 Hz)		100		dB

3 Probe Connector Panel

3.1 Doppler connector:

Type of connector: 10 pin LEMO.

Use: A Vingmed Stand-alone Doppler probe is connected to this input.

See IV & DP Board assembly drawing for physical location of pins.

Table 1: Doppler Connector Signal Description

Pin #	Signal	Description
1	GND	Ground from RLY board
2	AAXD7P	RX/TX signal (RX in CW)
3	AAXD7N	Ground reference for RX/TX signal above
4	GND	Ground from RLY board
5	XDDPCD	Resistor code signal
6	AAXD8P	RX/TX signal (TX in CW)
7	AAXD8N	Ground reference for RX/TX signal above
8	GND	Ground reference for resistor code signal
9	GND	Ground from RLY board
10	GND	Ground from RLY board

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3.2 PA/LA probe connectors (3):

Type of connectors: 260 pin Cannon DL.

Use: For use of phased array-, linear array- and curved linear array probes.

See Relay Board assembly drawing for physical location of pins.

(Connector 1 shown)

	Signal									
	1	2	3	4	5	6	7	8	9	10
A	XD1_1	XD2_1	XD17_1	XD18_1	XD33_1	XD34_1	XD49_1	XD50_1		
B	AGND1	XD3_1	AGND1	XD19_1	AGND1	XD35_1	AGND1	XD51_1		
C	XD4_1	XD5_1	XD20_1	XD21_1	XD36_1	XD37_1	XD52_1	XD53_1		
D	XD6_1	AGND1	XD22_1	AGND1	XD38_1	AGND1	XD54_1	AGND1		
E	XD7_1	XD8_1	XD23_1	XD24_1	XD39_1	XD40_1	XD55_1	XD56_1		
F	XD9_1	XD10_1	XD25_1	XD26_1	XD41_1	XD42_1	XD57_1	XD58_1		
G	AGND1	AGND1	AGND1	AGND1	AGND1	AGND1	AGND1	AGND1		AGND1
H	XD11_1	XD12_1	XD27_1	XD28_1	XD43_1	XD44_1	XD59_1	XD60_1		VRO-TA
J	XD13_1	XD14_1	XD29_1	XD30_1	XD45_1	XD46_1	XD61_1	XD62_1		AGND1
K	XD15_1	AGND1	XD31_1	AGND1	XD47_1	AGND1	XD63_1	AGND1		LROT
L	XD16_1		XD32_1		XD48_1		XD64_1	TEMP1		AGND1
M										RROT
N										
P	XD65_1	XD66_1	XD81_1	XD82_1	XD97_1	XD98_1	XD113_1	XD114_1	MUX_SDA1	MUX_SDA2
R	AGND2	XD67_1	AGND2	XD83_1	AGND2	XD99_1	AGND2	XD115_1	MUX_SDA3	MUX_SDA4
S	XD68_1	XD69_1	XD84_1	XD85_1	XD100_1	XD101_1	XD116_1	XD117_1	MUX_SDA5	MUX_SDA6
T	XD70_1	AGND2	XD86_1	AGND2	XD102_1	AGND2	XD118_1	AGND2	MUX_SDA7	MUX_SDA8
U	XD71_1	XD72_1	XD87_1	XD88_1	XD103_1	XD104_1	XD119_1	XD120_1	MUX_SCL	
V	XD73_1	XD74_1	XD89_1	XD90_1	XD105_1	XD106_1	XD121_1	XD122_1	MUX_LE_L	AVDD
W	AGND2	AGND2	AGND2	AGND2	AGND2	AGND2	AGND2	AGND2	AGND2	AGND2
X	XD75_1	XD76_1	XD91_1	XD92_1	XD107_1	XD108_1	XD123_1	XD124_1	A0	MUX_VPP
Y	XD77_1	XD78_1	XD93_1	XD94_1	XD109_1	XD110_1	XD125_1	XD126_1	PR_ACT1	GND
Z	XD79_1	AGND2	XD95_1	AGND2	XD111_1	AGND2	XD127_1	AGND2	A1	MUX_VNN

	Signal									
	1	2	3	4	5	6	7	8	9	10
a	XD80_1		XD96_1		XD112_1		XD128_1		GND	PR_PRES
b									PCF_SCL	PCF_SDA
c									VDD	GND

PA Transducer Signals

Signal Name	Type	Description
XD*n*_1	IO	Transducer *n* of 128, PA probe 1
XD*n*_2	IO	Transducer *n* of 128, PA probe 2
XD*n*_3	IO	Transducer *n* of 128, PA probe 3

PA Control and Sense Signals

Signal Name	Type	Description
PR_PRES*(n)*	IO	PA Probe *n* present (TTL)
PR_ACT*n*	O	Probe *n* active (TTL)
MUX_SCL	I	Probe multiplexer clock (TTL)
MUX_SDA*n*	I	Probe multiplexer serial data *n* of 8 (TTL)
MUX_LE	I	Probe multiplexer latch enable (TTL)
MUX_SCL*(n)*	O	Probe multiplexer clock, probe *n (TTL)*
MUX_SDA*n*	O	Probe multiplexer serial data *n* of 8 (TTL)
MUX_LE*(n)*_L	O	Probe multiplexer latch enable, probe *n (TTL)*
TEMP	IO	Phased array TEE temperature sense signal
PCF_SCL	O	Probe configuration PROM clock (TTL)
PCF_SDA	IO	Probe configuration PROM data (TTL)
A0	I/O	Address for EEPROM (conn. dependant) (0 or 5V)
A1	I/O	Address for EEPROM (conn. dependant) (0 or 5V)
VROTA	IO	Scan plane 2 position for MPTE probe
LROT	IO	Rotate left control for MPTE probe (TTL)
RROT	IO	Rotate right control for MPTE probe (TTL)
MUX_VPP	O	+80 V for multiplexers
MUX_VNN	O	-80 V for multiplexers

3.3 AA Connectors (2):

Type of connectors: 30 pin circular Burndy.

Use: For use of mechanical APAT and TEE probes.

See Relay Board assembly drawing for physical location of pins.

(Connector B shown).

	Signal
1	AGND1
2	AAVSS
3	LROTB
4	AGND1
5	AAVDD
6	AGND1
7	AGND1
8	AGND1
9	AGND1
10	POSBN
11	AGND1
12	AGND1
13	AGND1
14	AGND1
15	AGND1
16	AGND1
17	to P23
18	RROTB
19	MOTBP
20	MOTBN
21	TEMOTBN
22	to P24
23	POSBP
24	
25	VROTAB
26	XDAACDB
27	to P19
28	to P20
29	to P21
30	to P22

AA Element Signals

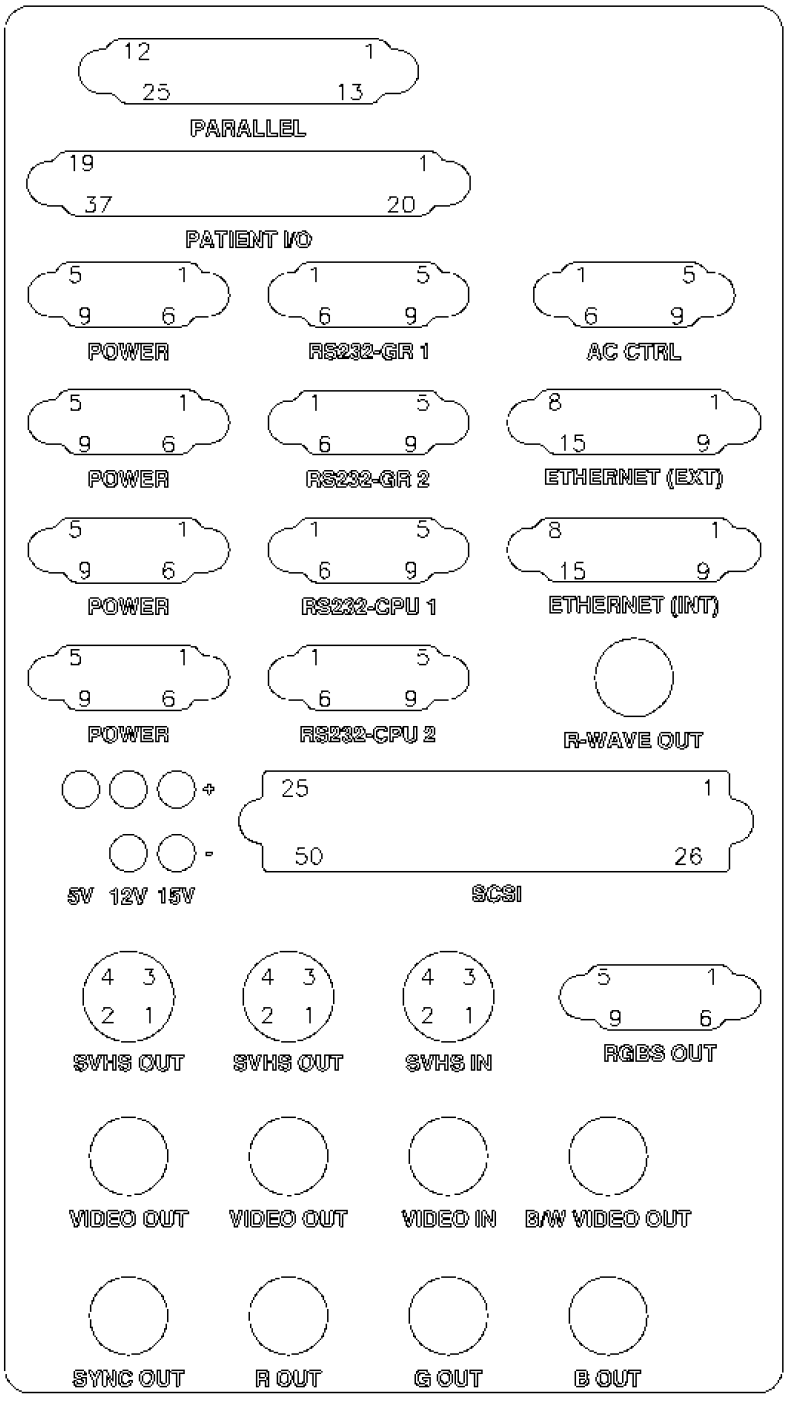
Signal Name	Type	Description
P19-P24	IO	6 AA transducer channels, coax to RLY bd.

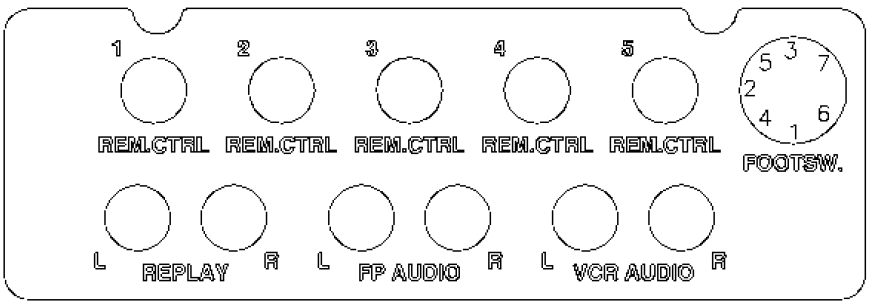
AA Control and Sense Signals

Signal Name	Type	Description
MOTBP	O	AA positive motor drive
MOTBN	O	AA negative motor drive (max +/- 12V)
TEMOTBN	O	TE probe negative motor drive (max +/- 12V)
POSBP	I	AA positive position sense (500 kHz signal)
POSBN	I	AA negative position sense (ground)
VROTAB	I	Scan plane 2 pos. for MPTE probe B (0-10V_{DC})
LROTB	O	Rotate left control for MPTE probe (TTL)
RROTB	O	Rotate right control for MPTE probe (TTL)
AAVSS	O	+15V (for TE endoscope house)
XDAACDB	I/O	Probe Code signal (0 - 12V_{DC})

4 Internal I/O without PosDet and PAMPTE support

The drawing below shows the different connectors and pin numbers.

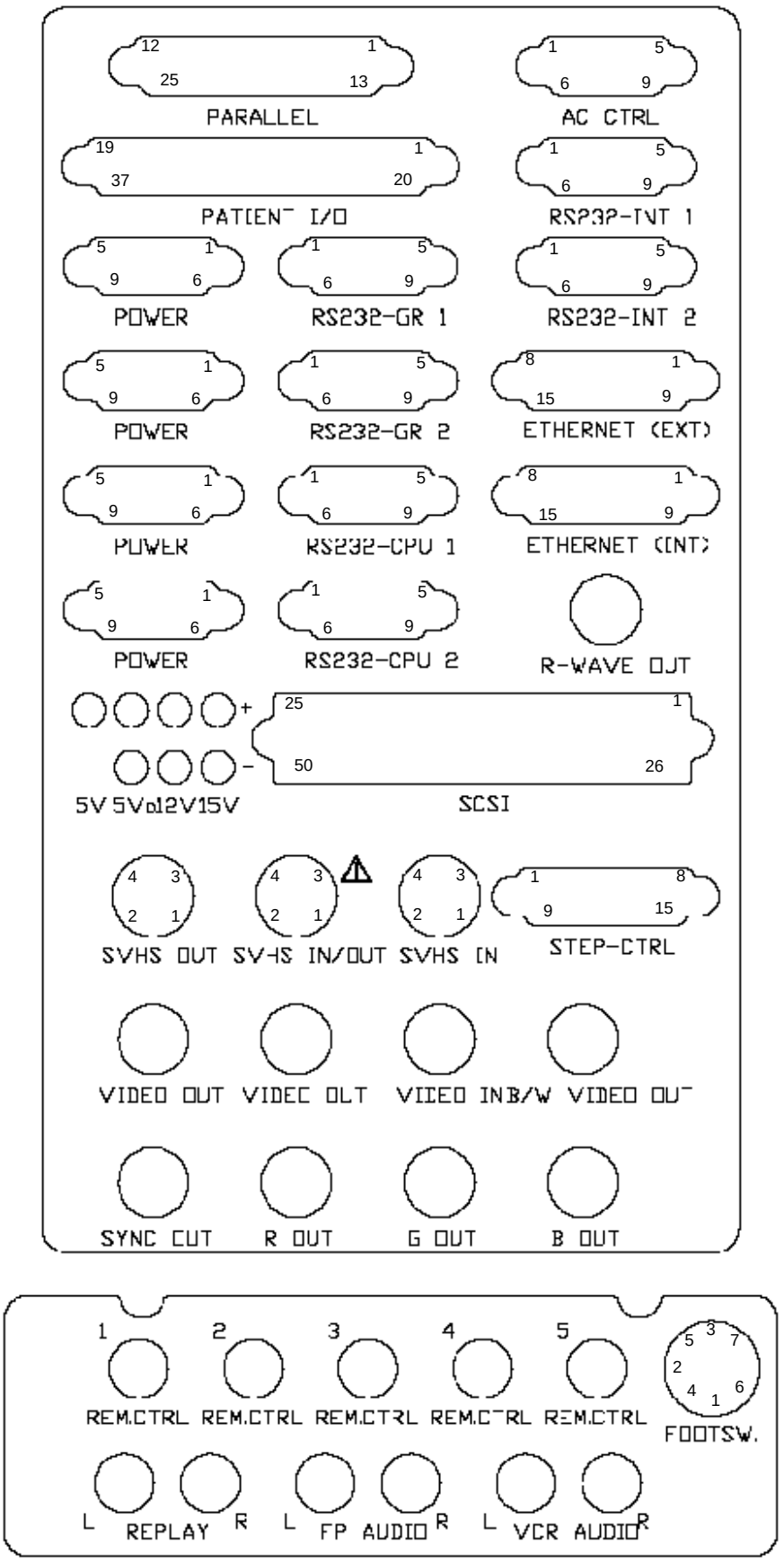




Macintosh HD:User:James@i-arb:Service:S5_ServiceMan:S5_serv_files:F1_04_io_sig.05.
Printed: December 5, 2000.

5 Internal I/O with PosDet and PAMPTE support

The drawing below shows the different connectors and pin numbers.



5.1 Parallel connector:

Type of connector: 25 pin DSUB, female.

Use: Image and text printing on parallel printers. Data transfer to post prosessing unit (e.g. MAC).

Pin number	Signal	In/out	Level
1	Strobe	output	TTL
2	D 0	in/out	TTL
3	D 1	in/out	TTL
4	D 2	in/out	TTL
5	D 3	in/out	TTL
6	D 4	in/out	TTL
7	D 5	in/out	TTL
8	D 6	in/out	TTL
9	D 7	in/out	TTL
10	ACK	input	TTL
11	BUSY	input	TTL
12	PE	input	TTL
13	SLCT	output	TTL
14	AUTOFEED	output	TTL
15	ERROR	input	TTL
16	INIT	output	TTL
17	SELECTIN	output	TTL
18-25	GND		

Table 2: Parallel interface, Centronics

5.2 Patient I/O connector (cable no.7):

Type of connector: 37 pin DSUB, female.

Use: Cable connected to Patient I/O module. Serial and parallel interface signals in addition to power and ground.

Pin	Name	Type	Description
1, 3, 5, 7, 16, 17, 19, 21, 23, 25, 27, 29, 31	DGND	0V	Ground

Table 3: Patient I/O Connector

Pin	Name	Type	Description
2	CLKR	TTL	Transfer clock from PAT I/O
4	DR	TTL	Serial data from PAT I/O
6	FSR	TTL	Frame Sync
8 - 15	DSP_D0-7	TTL	Configuration data from PAT I/O
22	SEL1_L	TTL	Chip select to configuration reg. 1
24	SEL2_L	TTL	Chip select to configuration reg. 2
28	PRST_L	TTL	Reset PAT I/O board.
32, 33	+5V	+5V	+5V

Table 3: Patient I/O Connector

5.3 Power connectors (cables no. 8 and no. 9):

Type of connector: 9 pin DSUB, female.

Use: Power distribution to front panel and harddisk.

Power: (note that each output is protected with a recovery fuse).

Pin	Voltage	Color Code	Current (max)
1	+5V	Red	2 A
2	+12V	Yellow	1A
3	-12V		1A
4	+15V	Orange	1A
5	-15V	Violet	1A
6	GND	Black	
7	GND	“	
8	GND	“	
9	nc		

Table 4: Power Connectors 1- 4

5.4 RS232 connectors (a.o. cable no.3: FP serial ctrl):

Type of connector: 9 pin DSUB, male.

Use:

RS232-GR 1: Serial communication between Graphics board and the Front Panel.

RS232-GR 2: spare

RS232-CPU 1: Serial communication between CPU board and VCR.

RS232-CPU 2 : spare

RS232-INT 1: Bird (only available on boards with support for PAMPTE support)

RS232-INT 2: Bird (only available on boards with support for PAMPTE support)

Signals of interest:

Signal	Pin	In/out	Baud rate
DCD	1		
RD	2	input	300-38.400
TD	3	output	300-38.400
DTR	4	input	
GND	5		
DSR	6		
RTS	7	output	
CTS	8	input	
	9		

Table 5: RS-232

5.5 AC CTRL connector (cable no. 11):

Type of connector: 9 pin DSUB, male.

Use: A power remote control line (STBTGL_L) from the IV, DP and STBY Board to the AC power is implemented. The AC power remote control interface detects tthis signal and gives an interupt (PODREQ) to the CPU which prepares power-down. The AC power will not switch off until a grant signal (POFGNT) from the CPU is activated.

The LEDs on the power STBY board are activated by the thre signals, LEDPWR (+5V), STBLED_L and ONLED_L.

HITEMP_L is a signal generated by the ACCTRL board when a hifg temperature condition is detected.

Signals of interest:

Pin	Name	Description
1	LEDPWR	+5V
2	STBLED_L	Led drive
3	ONLED_L	Led drive
4	POFREQ	Power off request
5	STBTGL_L	From remote switch
6	GND	
7	POFGNT	Power off grant
8	GND	
9	HITEMP_L	High temp (>60°) warning

Table 6: AC Power Remote Control

6 ETHERNET connectors (INT and EXT):

Type of connector: 15 pin DSUB, female.

Use: The Ethernet signals from the system CPU are looped through the Internal I/O board before routed to the External I/O board.

Pin	Name	Description
2	EC+	Collision Input, diff. pos.
3	ET+	Transmit Output, diff. pos.
5	ER+	Receive Input, diff. pos.
6	GND	Ground
9	EC-	Collision Input, diff. neg.
10	ET-	Transmit Output, diff. neg.
12	ER-	Receive Input, diff. neg.
13	+12V	+12V for AUI unit.

Table 7: Ethernet connector

6.1 R-WAVE OUT connector:

Type of connector: BNC, female.

Use: This R-WAVE OUT signal is used for ECG triggering, e.g. when transferring cinellops to a MAC.

Level: TTL

6.2 SCSI cable (no 10):

Type of connector: 50 pins CHAMP, male.

Use: For communication with floppy disk, hard disk, optical disc and e.g. a SONY D7000 printer.

Pin number	Signal	In/out	Description
1-12	GND		
13	nc		
14-25	GND		
26	DB0	in/out	Data
27	DB1	in/out	"
28	DB2	in/out	"
29	DB3	in/out	"
30	DB4	in/out	"
31	DB5	in/out	"
32	DB6	in/out	"
33	DB7	in/out	"
34	DBP	in/out	Parity
35	GND		
36	GND		
37	GND		
38	TERMPWR	output	Terminator Power
39	GND		
40	GND		
41	ATN	in/out	Attention
42	GND		
43	BSY	in/out	Busy
44	ACK	in/out	Acknowledge
45	RST	in/out	Reset
46	MSG	in/out	Message
47	SEL	in/out	Select
48	C/D	in/out	Control/Data
49	REQ	in/out	Request
50	I/O	in/out	Input/output

Table 8: SCSI-2 Fast Connector

6.3 SVHS OUT connectors:

Type of connector: 4 pin MINI DIN, female.

Use: Super VHS outputs (luma and chroma) to VCR and printers.

Signals of interest:

Signal	Pin	Voltage	Imped-ance	Band-width
GND-Y	1			
GND-C	2			
SVHS Y	3	714 mV	75 ohm	5 0MHz
SVHS C	4	300 mV	75 ohm	5 0MHz

Table 9: SVHS Outputs

6.4 SVHS IN connector:

Type of connector: 4 pin MINI DIN, female.

Use: Super VHS outputs (luma and chroma) from VCR.

Signals of interest: Same as above.

6.5 RGBS OUT connector:

(Only available on boards without support for PosDet and PAMPTE)

Type of connectors: 9 pin DSUB, female, and BNCs, female.

Use: R, G, B and SYNC (NTSC or PAL) to color printers and cameras.

Signals of interest:

Signal	Voltage	Imped-ance	Band-width
R, G, B	714 mV	75 ohm	50 MHz
SYNC	300 mV	75 ohm	1 MHz

Table 10: RGB and SYNC outputs

6.6 STEP-CTRL connector:

(Only available on boards with support for PosDet and PAMPTE)

6.7 VIDEO OUT connectors:

Type of connectors: BNC, female.

Use: Composite video (NTSC or PAL) to VCR and printers.

Signals of interest:

Signal	Voltage	Imped-ance	Band-width
Comp Video	1 V	75 ohm	15 MHz
Comp sync	300 mV	75 ohm	1 MHz

Table 11: Composite video

6.8 VIDEO IN connector:

Type of connector: BNC, female.

Use: Composite video (NTSC or PAL) from VCR.

Signals of interest: same levels as above.

6.9 B/W VIDEO OUT connector:

Type of connector: BNC, female.

Use: Black and White video (NTSC or PAL) to B/W printer.

Signals of interest: same levels as above.

6.10 REM.CTRL connectors:

Type of connectors: BNC, female.

Use: Remote control 'print' signal to printers and cameras. Device and polarity must be selected in system configuration.

Signals of interest: All are TTL levels.

6.11 FOOTSW. connector

Type of connectors: 5 pin DIN, female.

Use: User selectable footswitch control (e.g. FREEZE, PAUSE etc.).

Signals of interest: TTL level signals.

SW 1: pin 1

SW 2: pin 3

SW 3: pin 4

GND: pin 2

6.12 REPLAY (L & R) connectors (cable no.23)

Type of connectors: Phono, female.

Use: Audio from VCR during playback.

Signals of interest: REPLAY_ I and REPLAY_Q: both $1V_{rms}$.

6.13 FP AUDIO (L & R) connectors (cable no.23)

Type of connectors: Phono, female.

Use: Doppler Audio to front panel audio amplifier and loudspeakers .

Signals of interest: ANDOP_ I and ANDOP_Q: both $1V_{rms}$.

6.14 VCR AUDIO (L & R) connectors (cable no.23)

Type of connectors: Phono, female.

Use: Doppler audio to VCR for recording.

Signals of interest: ANDOP_ I and ANDOP_Q: both $1V_{rms}$.

7 Card Rack

7.1 RGBS OUT connector (cable no.6):

Type of connectors: BNCs, female.

Use: R, G, B and SYNC (NTSC or PAL) to system monitor.

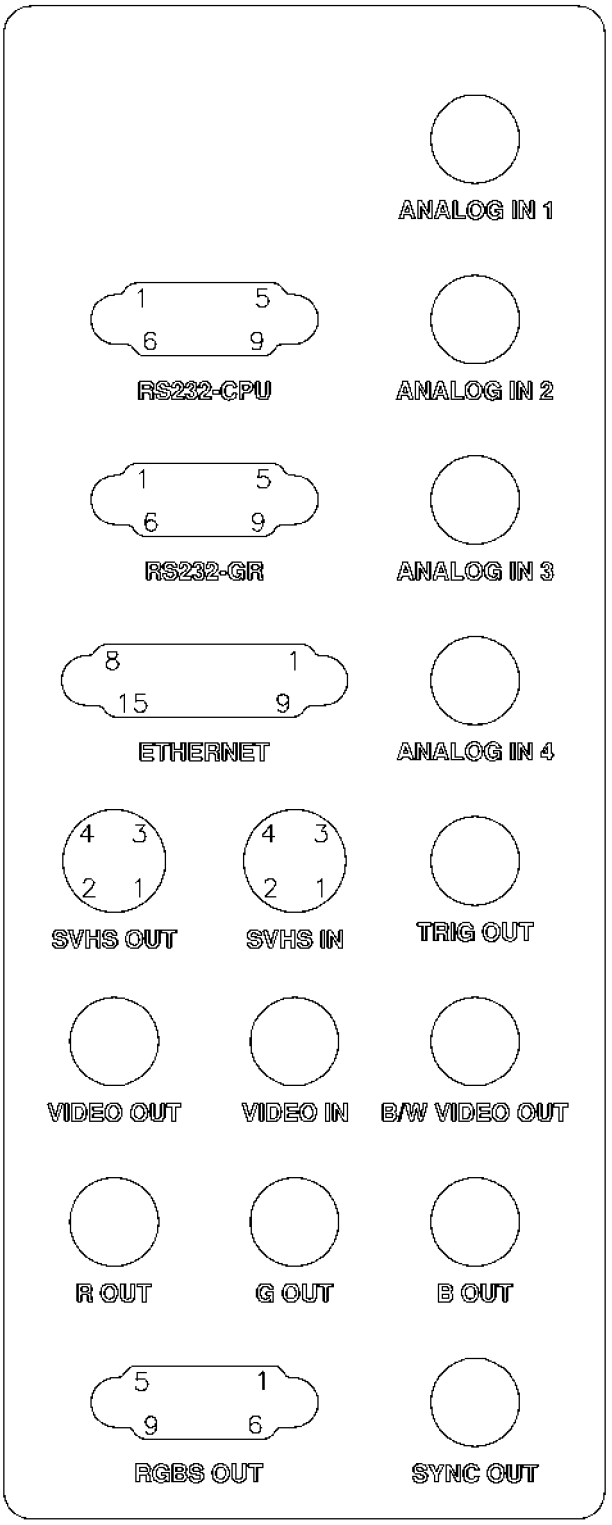
Signals of interest:

Signal	Voltage	Impedance	Bandwidth
R, G, B	714 mV	75 ohm	50 MHz
SYNC	300 mV	75 ohm	1 MHz

Table 12: RGB and SYNC outputs

8 External I/O

The drawing below shows the different connectors and pin numbers.



Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:F1_05_io_sig.05.
Printed: December 5, 2000.

8.1 RS232 connectors:

Type of connector: 9 pin DSUB, male.

Use:

RS232-CPU: serial port to CPU board.

RS232-GR: serial port to GRAPHICs board.

Signals of interest:

Signal	Pin	In/out	Baud rate
DCD	1		
RD	2	input	300-38.400
TD	3	output	300-38.400
DTR	4	input	
GND	5		
DSR	6		
RTS	7	output	
CTS	8	input	
	9		

Table 13: RS-232

8.2 ANALOG IN 1-4 connectors

Type of connectors: Phono, female.

Use: Maximum 4 analog external signals can be input to the system.

Signals of interest: ANIN1-4: Level: max $12V_{pp}$.

8.3 TRIG OUT connector:

Type of connectors: BNC, female.

Use: User selectable TRIG signal (usually ECG trigger).

Signals of interest: TRIG OUT: TTL level.

8.4 SVHS OUT connectors:

Type of connector: 4 pin MINI DIN, female.

Use: Super VHS outputs (luma and chroma) to VCR and printers.

Signals of interest:

Signal	Pin	Voltage	Imped-ance	Band-width
GND-Y	1			
GND-C	2			
SVHS Y	3	714 mV	75 ohm	5 0MHz
SVHS C	4	300 mV	75 ohm	5 0MHz

Table 14: SVHS Outputs

8.5 SVHS IN connector:

Type of connector: 4 pin MINI DIN, female.

Use: Super VHS outputs (luma and chroma) from VCR.

Signals of interest: Same as above.

8.6 VIDEO OUT connector:

Type of connector: BNC, female.

Use: Composite video (NTSC or PAL) to VCR and printers.

Signals of interest:

Signal	Voltage	Imped-ance	Band-width
Comp Video	1 V	75 ohm	15 MHz
Comp sync	300 mV	75 ohm	1 MHz

Table 15: Composite video

8.7 VIDEO IN connector:

Type of connector: BNC, female.

Use: Composite video (NTSC or PAL) from VCR.

Signals of interest: same levels as above.

8.8 B/W VIDEO OUT connector

Type of connector: BNC, female.

Use: Black and White video (NTSC or PAL) to B/W printer.

Signals of interest: same levels as above.

8.9 RGBS OUT connector:

Type of connectors: 9 pin DSUB, female, and BNC, female.

Use: R, G, B and SYNC (NTSC or PAL) to color printers and cameras.

Signals of interest:

Signal	In/out	Voltage	Imped-ance	Band-width
RGB	output	714 mV	75 ohm	50 MHz
SYNC	output	300 mV	75 ohm	1 MHz

Table 16: RGB and SYNC outputs

8.10 ETHERNET connector:

Type of connector: 15 pin DSUB, female.

Use: The Ethernet signals from the system CPU are looped through the Internal I/O board before routed to the External I/O board.

Pin	Name	Description
2	EC+	Collision Input, diff. pos.
3	ET+	Transmit Output, diff. pos.
5	ER+	Receive Input, diff. pos.
6	GND	Ground
9	EC-	Collision Input, diff. neg.
10	ET-	Transmit Output, diff. neg.
12	ER-	Receive Input, diff. neg.
13	+12V	+12V for AUI unit.

Table 17: Ethernet connector

Your Notes:

SYSTEM FIVE Maintenance Procedure

Overview

Introduction

This part of the Service Manual describes the Maintenance Procedure for use on SYSTEM FIVE .

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
Introduction	G1-3
Tool Requirements	G1-3
Description	G1-3

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:G1_01_Innh.
Printed: December 5, 2000.

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SYSTEM FIVE Maintenance Procedure - rev. 04

1 Introduction

1.1 Abstract

This procedure describes how to perform preventive maintenance, which should be done on a regular basis, e.g. twice a year.

1.2 Document History

Rev.	Date	Sign.	Description
01	28 Apr. 1995	GRL	First version of document
02	5 May 1997	GRL	Added DC offset calibration and cleaning of probe connectors
03	5 Aug 1999	LHS	Updated Tool Requirements, updated some x-refs.
04	12 Jan 2000	LHS/ JB	Corrected some x-refs.Added Installation and maintenance with cleaning instructions

Macintosh HD:User:James:@:arch:Service:S5_ServiceMan:S5_serv_files:G1_02_maintenance_proc.04.

2 Tool Requirements

- Service tool kit as described on page Intro-3
- Cleaning cloth.
- Cleaning detergent.
- Vacuumer.
- Spray can with high pressure air.

3 Description

3.1 Air Filter Cleaning

1. Loosen the 3 screws holding the main air filter cover. This cover is located on the right lower side below the lower side panel.
2. Remove the cover.
3. Pull out the main air filter.
4. Pull out the rear air filter, which is located underneath the AC- and DC power supplies.
5. The filters can be cleaned in sprinkling water, or they can be dusted with a vacuum cleaner.
6. Install the clean filters.

3.2 Probe Connector Cleaning

1. Use high-pressure air and thoroughly spray the system probe connectors to remove dust inside the connector sockets.

3.3 Mains Cable Inspection

1. Disconnect the mains plug from the wall.
2. Unscrew the plug cover/bend relief.
3. Verify that the LINE, NEUTRAL and GROUND wires are properly attached to the terminals, and that no strands may cause short-circuiting.
4. Inspect the strain relief and verify that the cable is properly secured.
5. Mount the plug cover/bend relief.
6. Inspect the mains power cable, and verify that it is free from scratches/damages that may expose any of the wires inside the collar.
7. Inspect the system strain/bend relief and verify that it secures the cable properly.

3.4 General Cleaning

1. Using warm water with a fluid detergent on a soft clothe, carefully wipe the entire system. Be careful when wiping the QWERTY keyboard (if a plastic cover is not installed).

3.5 Tests

1. Perform the DC Power Test Procedure (re. chapter K, section 4.6 on page K04-4) to verify that all DC voltages are present and within acceptable limits.
2. Perform the HV Test Procedure (re. chapter K, section 4.5 on page K04-3) to verify that all HV voltages are present and within acceptable limits.
3. Perform an Element Test (re. chapter K, section 4.7 on page K04-5) on each probe to verify that all probe elements (and system channels) are functional.
4. Perform the Automatic System Test (re. chapter K, section 9.6 on page K09-2) to verify that all boards function according to specifications.
5. Perform the Front Panel Test Procedure (re. chapter K, section 4.1 on page K04-1) to verify that all keyboard controls are functionable.
6. Perform the Front End (DC Offset) Calibration Procedure (re. chapter K, section 23 on page K16-1) to compensate for possible BF A/D converter offset drift.
7. Check the monitor, VCR and the other peripherals. If required and applicable, clean printer head(s).

3.6 Installation & Maintenance

3.7 System FiVe Shipments:

• System FiVe should be unpacked, installed and cleared for operation by an authorized service representative. Packing /Unpacking instructions are found on the outside of the transport package. System FiVe must be mains-connected to a **HOSPITAL GRADE** power source. DO NOT attempt to assemble the system or connect it to a power source until qualified approval for operation has been given.

3.8 Preventive User Maintenance

Cleaning the System

• DO NOT pour water on System FiVe or immerse any part of it, in any liquid. Avoid spilling liquids into ventilation grates.

Weekly: • The exterior surface of the System FiVe should be cleaned with a dry cloth. When more extensive cleaning is required, the unit should first be powered down and then wiped with a soft cloth that has been dampened with either water or a very mild detergent. NEVER use abrasive cleaners or steel wool.

After use: • Wipe away gel stains from the control panel and keyboard as soon as possible, because some ultrasound gels are mildly aggressive towards plastics.

3.9 Recommended Liquid Chemical Germicides

In order to provide users with options in choosing a germicide for processing their ultrasound transducer between uses, GE Medical Systems routinely reviews new medical germicides for compatibility with the materials used in the transducer enclosure, cable and lens. Although a necessary step in protecting your patients and employees from disease transmission, liquid chemical germicides must also be selected to minimize potential damage to the transducer.

For cleaning and low-level disinfection, we recommend washing the probe and cable in a warm soap and water solution (<80∞F / 27∞C), removing all visible residue by scrubbing with a soft bristle brush or gauze and using a mild, nonabrasive soap. Rinse with clean water and wipe dry with a soft towel. Check the instructions provided with each probe so as not to exceed the depth to which the probe can be safely immersed in liquid. Do not immerse the electrical connector. Use additional precautions (e.g., gloves and gown) when decontaminating an infected probe.

Low-level disinfection is intended to destroy vegetative bacteria and lipid or medium sized viruses and is somewhat effective on fungi. This is usually sufficient when scanning on intact surface skin.

For high-level disinfection, it is necessary to soak the thoroughly cleaned probe in a suitable liquid chemical germicide for an extended period. Check the instructions provided with each probe so as not to exceed the depth to which the probe can be safely immersed in liquid. Do not immerse the electrical connector. Use additional precautions (e.g., gloves and gown) when decontaminating an infected probe. The following germicides have been evaluated as being compatible only with the probe type listed:

Probe	P/N	DISINFECTANT			
		Cidex ™	Cidex PA™	Cidex OPA™	Spor ox™
FPA 2.5 -64	KG100001	YES	YES	YES	YES
FPA 3.5 -96	KK100005	YES	YES	YES	YES
FPA 5.0 -96	KN100002	YES	YES	YES	YES
FLA 5.0-192	KN100003	YES	YES	YES	YES
FPA 10.0	KW100002	YES	YES	YES	YES
FPA 5.0 - 128	KN100001	YES	No	YES	No
CLA 3.5 - 192	KK100004	YES	No	YES	No
CLA 5.0 - 192	KK100008	YES	No	YES	No
ECLA 6.5 -128	KQ100002	YES	No	No	No
FLA 10.0	KW100001	YES	No	No	No
2MHz Doppler	TE100024	YES	No	No	No
6MHz Doppler	TQ100002	YES	No	No	No
Transesophageal probes		YES	YES	YES	No

Be sure to follow the germicide manufacturer's instructions for storage, handling, preparation, time of exposure and disposal. Use only disinfectants that are approved according to local / national regulations.

High-level Disinfection destroys vegetative bacteria; lipid & non-lipid viruses, fungi and, depending highly on time of contact, is effective on bacterial spores. This is required for cavity (TV,TR,TE) scanning when in contact with mucosal membrane.

CAUTION - Improper handling can lead to early probe failure and electric shock hazards:

- DO NOT disinfect or sterilize probes by autoclaving or ethylene oxide gas process.

- DO NOT soak or wipe the probe face with methanol, ethanol, isopropanol or any other alcohol based cleaner. Doing so could result in irreversible damage to the probe’s lens.

- DO follow the specific cleaning, disinfection procedures provided with the documentation of your product, as well as the germicide manufacturer's instructions.

Failure to do so will void probe warranty.

SYSTEM FIVE Config. & Rev. Control

Overview

Introduction

This part of the Service Manual describes the Configurations and hardware revisions used in SYSTEM FIVE.

Table of Contents

This table gives you an overview for this part of the Service Manual:

Contents	Page
Compatibility Overview – rev. 15	H1-1
Board Compatibility List: • Elite, Performance and Premium Systems • Membership Systems • Advantage Systems • Compatibility Notes	H2-1 H2-2 H2-10 H2-14 H2-18
128 vs. 256 channel systems	H3-1
Board Revision History	H4-1
Power Supply Revision History - rev. 01	H5-1

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:H0_01_Innh.06.
Printed: December 5, 2000.

Your Notes:

Compatibility Overview – rev. 15

1 Introduction

1.1 Purpose

The intention with this document is to give an overview of the compatibility between the different boards, software and hardware in System FiVe.

1.2 Document History

Rev.	Date	Sign.	Description
01	1 Mar 1996	GRL	First version of document.
02	31 May 1996	GRL	Updated with latest revisions on TX128, RX128, PRC, XDCTRL, BF, SDP.
03	1 Aug 1996	GRL	V1.1 release.
04	5 May 1997	GRL	V1.2 release.
05	20 Jun 1997	GRL	V1.2.1/V1.2.2 releases. Added configuration for the Membership system (128-ch.system).
06	4 Nov19 97	GRL	V1.3 release.
07	22 Dec 1997	GRL	V1.3.1 release
08	12 May 1998	GRL	Updated per V1.4 release
09	16 Sept 1998	GRL	Updated per V1.5 release
10	18 Dec. 1998	GRL	Updated per V1.5.2 release
11	16 Jan 1999	JK	Updated per V1.6 release
12	27 Apr 1999	JK	Updated some of the contents
13	10 Aug 1999	JK/LHS	Reorganized the contents.Updated per V1.7 release.
14	6. Sep 1999	LHS	Updated per V1.8 release. Combined the documents for Elite, Performance and Premium systems.
15	25. Oct.1999	LHS	Updated pr. v 1.7.1 release.
16	22. Dec 1999	JK/LHS	Updated per v.1.9 release.
17	02 Nov.2000	JB	Updated pr. 1.9.x release

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:H1_02_compat_a.16.
Printed: December 5, 2000.

1.3 System Definitions

Elite Systems,
Performance systems,
Premium Systems: (High End):

256 channels (128 tx and analog rx channels, 256 digital BF channels).

Membership Systems (Mid Range):

128 channels (128 tx channels, 64 analog rx channels, 64 digital BF channels).

Advantage Systems:

Same as Premium, except that CLA probes and PAMPTEE probes are optional. 128 channels (128 tx channels, 64 analog rx channels, 64 digital BF channels).

Advantage ^{W}/HFR Systems:

Same as Advantage, but with High Frame Rate.

2 Software Revision History

2.1 History

In order to display the system software revision, press the *Setup* button and select *Configuration &Test* and then *SW*. Both the system software revision and the revision of the local DSP software will be shown. See the System FiVe User manual, FA092423, for more details.

System SW version	Date	Description
V1.0	Dec. 1995	First release of System-5 software.
V1.1b33	Apr. 1996	Improved functionality: M&A improved, APAT support (only 3.25 and adult MPTE), CW Doppler sensitivity, response time decreased.
V1.1b51	May 9. 1996	Improved reliability (less lock-ups)
V1.1	Jul 5. 1996	General improvements. See release notes for details.
V1.1.1	Oct. 1996	Added TVI and Coronary applications, B-color. Support for APA5.0 and mech. ped. MPTE. Extensive bug fixing, see release notes.
V1.1.2	Nov. 1996	Corrected "green" artifact in CFM. Improved image quality. Several new applications added. Several bugs fixed, see release notes.
V1.2	23 May 1997	Added functionality. General improvements. See release notes for details.
V1.2.1	30 May 1997	Corrected three bugs in V1.2. (one of them regarding BF4 setup on boards without conf. prom - id).

System SW version	Date	Description
V1.2.2	20 June 1997	5 different V1.2.2 configurations are made available for the mid range (128-ch.) systems and the high end (256-ch.) systems. Reduced power for Oldelft probe. Default image storage to EchoPAC.
V1.2.3	Sept. 1997	5 different V1.2.3 configurations available. V1.2.3 together with EchoPAC V5.4 improves reliability of systems with EchoPAC connections. For details, see Release Notes.
V1.3	18 Oct 1997	V1.3 release with 8 different configurations. Body Marks, Biopsy lines, Update function, M&A on playback, VCR remote control, Octave imaging, Contrast and RF Options, support for 6 MHz pencil probe and 5 MHz TEE probe. See Release Notes for more details.
V1.3.1	Dec. 1997	V1.3.1 release with the same 8 different configurations as mentioned above. Support for ECLA 6.25 Endo probe and 2 MHz TC probe, Octave on CLA 3.5, expanded gain range for ECG and Phono. See Release Notes for more details.
V1.3.2	Feb. 1997	V1.3.2 release with the same 8 different configurations as mentioned above. Production release for support of new RLY board, FA200464, new FEC board, FA200764 and new RFT board, FA200574 (only for Membership). Increased TEE temp. limit, minor bug fixing. See Release Notes for more details.
V1.4	May 1998	V1.4 release. Support of Vingmed PAMPTE probe, improved System-5 to EchoPAC reliability, improved Doppler display, improved Octave quality. See Release Notes for more details.
V1.5 & V1.5.1	Sept 1998	V1.5 release.V1.5 is only for Premium systems. Support of Vingmed PAMPTE probe (note: V1.4.1 did not support PAMPTE after all). Support for continuous capture together with EchoPAC V6.1. Improved Doppler audio and display, improved Octave quality.
V1.5.2	18 Dec.1998	V1.5.2 release for both Premium and Membership. First version with PAMPTE support for Membership. Corrected an intermittent lock-up problem from V1.5.1 (GRAPH-board problem).
V1.6	Jan 1999	Introduction of new System FiVe products with the production release v1.6 for Advantage and Performance **only**.
V1.7	Jul 1999	V1.7 release for all System FiVe models V1.5.2 /V1.6 bug-fixes. Support for new RX64, FA200777 and new RX128, FA200907. First version of 10 MHz Pediatric FPA probe. See release notes for more details.
V1.8	Sep 1999	V1.8 release for all System FiVe systems.

System SW version	Date	Description
V.1.7.1	Nov. 1999	Introduced new TX128-2 board. SW 1.7 updated to support this new board. (Sw 1.8 already supports the board).
V.1.9	Dec. 1999	Sw. 1.9 supports one new probe. HFR available as an option for System FiVe Advantage.
V1.9. x	Nov 2000	Support for REM Products

Board Compatibility List

1 Introduction

This is a list showing what different boards, part numbers and revisions that can be used together in System FiVe with different software versions. Most of the boards have E^2PROMS where part numbers and revisions are programmed. **These can be read in the *SysTest* menu, after having pressed the *Setup* button**. *The first revision is the module revision. The second is the MCD revision. Usually the module revision is changed only if the change is significant or if other boards are also affected by it. The MCD revision is updated each time there is a change (minor or major) on the board.*

It should be noted that on the first systems shipped out the fall of 1995, a lot of the boards have revisions lower than the ones listed below, and only a few of them had revisions written into the E^2PROMS. This does not necessarily imply that the boards are incompatible, but rather that they are prototypes that may functionally be equal to the ones in the list. If in doubt, contact GEVU technical support.

The List starts on page H2-2.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:H2_02_compat_a13.
Printed: December 5, 2000.

2 Elite, Performance and Premium Systems

Elite, Performance and Premium Systems (256 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
RLY	FA200020	A-A B-B B-C B-D B-E	A-A B-B B-C B-D B-E	A-A B-B B-C B-D B-E	A-A B-B B-C B-D B-E	
RLY	FA200434	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D	5,8
RLY-2	FA200890	A-A A-B	A-A A-B	A-A A-B	A-A A-B	
RLY-PAL-PB2	FA200799	A-A	A-A	A-A	A-A	
TX128	FA200021	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	1 1 1 1 1 1 1
RX128	FA200022	B-B C-C	B-B C-C	B-B C-C	B-B C-C	3
RX128	FA200638	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	3
RX128	FA200776	A-A B-B	A-A B-B	A-A B-B	A-A B-B	10
RX128-2	FA200907	A-A	A-A	A-A	A-A	
PRC	FA200264	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	5,8
XDCTRL	ML200078	V3.2-T6 V3.3	V3.2-T6 V3.3	V3.2-T6 V3.3	V3.2-T6 V3.3	2

Macintosh HD:User James:@i-arb:Service:S5_ServiceMan:S5_serv_files:H2_03_compat_b1.17.
Printed: December 5, 2000.

Elite, Performance and Premium Systems (256 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
BF32 (2 MLA)	FA200001	A-D A-E A-F A-G	A-D A-E A-F A-G	A-D A-E A-F A-G	A-D A-E A-F A-G	3 3 3 3
BF32 (2 MLA)	FA200382	A-B	A-B	A-B	A-B	3
BF32 (2 MLA)	FA200765	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E B-B B-C B-D B-E B-F B-G	
FEC	FA200009	B-B C-C D-D E-E	B-B C-C D-D E-E	-	-	17
FEC	FA200669	A-A	A-A	A-A	A-A	
FEC	FA200764	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F A-G	5,8
RFT	FA200373	B-B C-C D-D E-E E-F F-G	B-B C-C D-D E-E E-F F-G	B-B C-C D-D E-E E-F F-G	B-B C-C D-D E-E E-F F-G	
RFT1	FA200540	A-A E-B E-C E-D E-E E-F E-G	A-A E-B E-C E-D E-E E-F E-G	A-A E-B E-C E-D E-E E-F E-G	A-A E-B E-C E-D E-E E-F E-G E-H E-I	6

Elite, Performance and Premium Systems (256 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
RFP	FA200039	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	6
RFP	FA200555	A-A A-B	A-A A-B	A-A A-B	A-A A-B	6
SDP	FA200026	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G A-H A-I A-J	
CFP (4 MOD.)	FA200027	A-C	A-C	A-C	A-C A-D	
IMPORT	FA200028	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	
Image Port 2	FA200572	- -	- -	A-A A-B	A-A A-B A-C	15
SCONV	FA200029	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I D-J D-K	11
GRAPH5	FA200030	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I A-J A-K A-L A-M	12
MEMORY	FA200110	A-A B-B	A-A B-B	A-A B-B	A-A B-B	4
CPU	FA200109	A-A A-B	A-A A-B	A-A A-B	A-A A-B	18

Elite, Performance and Premium Systems (256 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
INT I/O bd. (assy)	FA200103 (FA200115)	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	8
EXT I/O bd. (assy)	FA200104 (FA200116)	B-B C-C	B-B C-C	B-B C-C	B-B C-C	
PAT I/O main board (box)	FA200193 (FA200105)	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F C-G	
PAT I/O amplifier board	FA200194	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G D-H	
HVPWR bd (box)	FA200063 (FA200114)	A-C A-D A-E A-F	A-C A-D A-E A-F	A-C A-D A-E A-F	A-C A-D A-E A-F	
AC CTRL	FA200107	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	
FP MAIN	FA200191	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J J-K J-L J-M K-N K-O L-P M-Q M-R	

Elite, Performance and Premium Systems (256 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
FP AUDIO	FA200076	B-B B-C B-D C-E	B-B B-C B-D C-E	B-B B-C B-D C-E	B-B B-C B-D C-E	12
MBD	FA200046	B-B C-C	B-B C-C	B-B C-C	B-B C-C	1 4,8
IV/DP Connector Board	FA200248	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	9

3 REM Systems

REM Systems			
Board	**P/N**	**SW v.1.9.x, Nov.2000**	**Notes** (See page H2-18.)
RLY	FA200434	A-A A-B A-C A-D	5,8,Factory option.
RLY-2	FA200890	A-A A-B	
TX128	FA200021	B-D B-E B-F B-G C-H C-I C-J	1
TX128-2	FA200999	A-A	
RX128-2	FA200907	A-A	
BF32 (2 MLA)	FA200765	A-E B-B B-C B-D B-E B-F B-G	16
FEC	FA200764	A-A A-B A-C A-D A-E A-F A-G	5,8
RFT No MLA	FA200574	E-A E-B E-C E-D E-E E-F E-G E-H	6
RFT1	FA200540	E-H E-I	16

REM Systems			
Board	**P/N**	**SW v.1.9.x, Nov.2000**	**Notes** (See page H2-18.)
SDP	FA200026	A-E A-F A-G A-H A-I A-J	
CFP (4 MOD.)	FA200027	A-C A-D	16
Image Port 2	FA200572	A-A A-B A-C	15
SCONV	FA200029	B-D B-E B-F C-G C-H D-I D-J D-K	- - - - - 11
GRAPH5	FA200030	A-C A-D A-E A-F A-G A-H A-I A-J A-K A-L A-M	- - - - - 12
CPU	FA200109	A-A A-B	 18
INT I/O bd. Complete	FA200925)	A-A	
EXT I/O bd. Complete	FA200926	A-A	
PAT I/O main board (box)	FA200193 (FA200105)	A-B B-C C-D C-E C-F C-G	
HVPWR bd (box)	FA200063 (FA200114)	A-C A-D A-E A-F	

REM Systems			
Board	**P/N**	**SW v.1.9.x, Nov.2000**	**Notes** (See page H2-18.)
AC CTRL	FA200107	A-A B-B B-C B-D	
FP MAIN	FA200191	E-E F-F G-G I-I I-J J-K J-L J-M K-N K-O L-P M-Q M-R	
FP AUDIO	FA200076	B-B B-C B-D C-E	
XD BUS BD	FA20064	A-D	
TempSense	FA200255	A-A	
VME Jumper	FA200075	A-A	15,16

4 Membership Systems

Membership systems (128 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
RLY	FA200020	B-C B-D B-E	B-C B-D B-E	B-C B-D B-E	B-C B-D B-E	
RLY	FA200434	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	5,8
RLY-2	FA200890	A-A A-B	A-A A-B	A-A A-B	A-A A-B	
RLY-PAL-PB2	FA200799	A-A	A-A	A-A	A-A	
TX128	FA200021	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	B-D B-E B-F B-G C-H C-I C-J	1 1 1 1
TX128-2	FA200999	-	A-A	A-A	A-A	
RX64	FA200522	A-D A-E	A-D A-E	A-D A-E	A-D A-E A-F A-G	7
PRC	FA200264	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	5,8
XDCTRL	ML200078	NOT STD.	NOT STD.	NOT STD.	NOT STD.	2
BF32 (1 MLA)	FA200550	B-B	B-B	B-B	B-B	
FEC	FA200669	A-A	A-A	A-A	A-A	
FEC	FA200764	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F	A-A A-B A-C A-D A-E A-F A-G	5,8

Membership systems (128 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
RFT	FA200373	E-E E-F F-G	E-E E-F F-G	E-E E-F F-G	E-E E-F F-G	
RFT1 NO MLA	FA200574	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	E-A E-B C-C E-D E-E E-F E-G E-H	
SDP	FA200026	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G A-H A-I A-J	
CFP (2 MOD.)	FA200409	A-A	A-A	A-A	A-A A-B	
IMPORT	FA200028	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	
Image Port 2	FA200572	- -	- -	A-A A-B	A-A A-B A-C	15
SCONV	FA200029	B-D B-E B-F C-G C-H (D-I)	B-D B-E B-F C-G C-H (D-I)	B-D B-E B-F C-G C-H (D-I)	B-D B-E B-F C-G C-H D-I D-J D-K	11
GRAPH5	FA200030	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I A-J A-K A-L A-M	12

Membership systems (128 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
MEMORY	FA200110	B-B	B-B	B-B	B-B	4
CPU	FA200109	A-A A-B	A-A A-B	A-A A-B	A-A A-B	18
INT I/O bd. (assy)	FA200103 (FA200115)	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	8
EXT I/O bd. (assy)	FA200104 (FA200116)	B-B C-C	B-B C-C	B-B C-C	B-B C-C	
PAT I/O main board (box)	FA200193 (FA200105)	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F C-G	
PAT I/O amplifier board	FA200194	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G D-H	
HVPWR bd (box)	FA200063 (FA200114)	A-C A-D A-E A-F	A-C A-D A-E A-F	A-C A-D A-E A-F	A-C A-D A-E A-F	
AC CTRL	FA200107	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	
FP MAIN	FA200191	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J I-K I-L I-M	E-E F-F G-G I-I I-J J-K J-L J-M K-N K-O L-P M-Q M-R	

Membership systems (128 channels)						
Board	**P/N**	**SW v.1.7, Apr. 99**	**SW v.1.7.1, Nov. 99**	**SW v.1.8, Sep. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
FP AUDIO	FA200076	B-B B-C B-D C-E	B-B B-C B-D C-E	B-B B-C B-D C-E	B-B B-C B-D C-E	12
MBD	FA200046	C-C	C-C	C-C	C-C	1,4,8
IV/DP Connector Board	FA200248	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	A-A A-B A-C B-D B-E B-F	9
VME Jumper	FA200075	A-A	A-A	A-A	A-A	15,16

5 Advantage Systems

Advantage Systems (128 channels)						
Board	**P/N**	**SW v.1.7 Apr. 99**	**SW v.1.7.1 Nov. 99**	**SW v.1.8 Aug. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
RLY	FA200434	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D	5,8,Factory option.
RLY-2	FA200890	A-A A-B	A-A A-B	A-A A-B	A-A A-B	
RLY-PAL-PB2	FA200799	A-A	A-A	A-A	A-A	
TX128	FA200021	B-D B-E B-F B-G C-H	B-D B-E B-F B-G C-H	B-D B-E B-F B-G C-H	B-D B-E B-F B-G C-H C-I C-J	1
TX128-2	FA200999	-	A-A	A-A	A-A	
RX64	FA200522	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D	A-A A-B A-C A-D A-E A-F A-G	
RX64	FA200777	A-A	A-A	A-A	A-A A-B	
PRC	FA200264	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	B-C B-D B-E B-F C-G D-H D-I	5,8,Factory option
XDCTRL	ML200078	V3.2-T6 V3.3	V3.2-T6 V3.3	V3.2-T6 V3.3	V3.2-T6 V3.3	2,Factory option
BF32 (1 MLA)	FA200538	A-A A-B	A-A A-B	A-A A-B	A-A A-B	
BF32 (1 MLA)	FA200811	A-A	A-A	A-A	A-A A-B A-C	

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:H2_03_compat_b5.17.
Printed: December 5, 2000.

Advantage Systems (128 channels)						
Board	**P/N**	**SW v.1.7 Apr. 99**	**SW v.1.7.1 Nov. 99**	**SW v.1.8 Aug. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
BF32 (2 MLA)	FA200765	-	-	-	A-E B-B B-C B-D B-E B-F B-G	16
FEC	FA200764	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C	A-A A-B A-C A-D A-E A-F A-G	5,8
RFT No MLA	FA200574	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	A-A A-B A-C A-D A-E	E-A E-B E-C E-D E-E E-F E-G E-H	6
RFT1	FA200540	-	-	-	E-H E-I	16
SDP	FA200026	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G	A-E A-F A-G A-H A-I A-J	
CFP (4 MOD.)	FA200027	A-C	A-C	A-C	A-C A-D	16
CFP (4 MOD.)	FA200409	A-A	A-A	A-A	A-A A-B	
IMPORT	FA200028	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	A-A A-B A-D A-E A-F	
Image Port 2	FA200572	- -	- -	A-A A-B	A-A A-B A-C	15

Advantage Systems (128 channels)						
Board	**P/N**	**SW v.1.7 Apr. 99**	**SW v.1.7.1 Nov. 99**	**SW v.1.8 Aug. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
SCONV	FA200029	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I	B-D B-E B-F C-G C-H D-I D-J D-K	- - - - - 11
GRAPH5	FA200030	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I	A-C A-D A-E A-F A-G A-H A-I A-J A-K A-L A-M	- - - - - 12
MEMORY	FA200110	A-A B-B	A-A B-B	A-A B-B	A-A B-B	4
CPU	FA200109	A-A A-B	A-A A-B	A-A A-B	A-A A-B	18
INT I/O bd. (assy)	FA200103 (FA200115)	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	C-D C-E C-F E-I E-J E-K E-L	8
EXT I/O bd. (assy)	FA200104 (FA200116)	B-B	B-B	B-B	B-B C-C	
PAT I/O main board (box)	FA200193 (FA200105)	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F	A-B B-C C-D C-E C-F C-G	
PAT I/O amplifier board	FA200194	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G	C-C D-D D-E D-F D-G D-H	

Advantage Systems (128 channels)						
Board	**P/N**	**SW v.1.7 Apr. 99**	**SW v.1.7.1 Nov. 99**	**SW v.1.8 Aug. 99**	**SW v.1.9/ 1.9.x, Dec. 99/Nov.00**	**Notes** (See page H2-18.)
HVPWR bd (box)	FA200063 (FA200114)	A-C A-D	A-C A-D	A-C A-D	A-C A-D A-E A-F	
AC CTRL	FA200107	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	A-A B-B B-C B-D	
FP MAIN	FA200191	E-E F-F G-G I-I I-J I-K	E-E F-F G-G I-I I-J I-K	E-E F-F G-G I-I I-J I-K	E-E F-F G-G I-I I-J J-K J-L J-M K-N K-O L-P M-Q M-R	
FP AUDIO	FA200076	B-B	B-B	B-B	B-B B-C B-D C-E	
MBD	FA200046	B-B C-C	B-B C-C	B-B C-C	B-B C-C	1 4,8
IV/DP Connector Board	FA200248	A-A A-B A-C B-D B-E	A-A A-B A-C B-D B-E	A-A A-B A-C B-D B-E	A-A A-B A-C B-D B-E B-F	- - - 9
VME Jumper	FA200075	A-A	A-A	A-A	A-A	15,16

6 Compatibility Notes

6.1 Special notes from the compatibility list

1.) TX128 and MBD: In order for TX128 rev.B-D and onwards to work (board run on analog +5V instead of digital +5V), the motherboard must have rev. B-B (+5V analog strapped from RX128 to TX128) or later. Part of V1.1 upgrade.

2.) In order to support the mechanical MPTE probe, the XDCTRL board XD2 software must be V3.2-T6 or newer.
The XDCTRL board is optional on 64 ch. systems.

3.) RX board FA200022 (with AD602) is used with BF p/n FA200001 (20 MHz A/D).
RX board FA200638 (with AD604) is used with BF p/n FA200382 (40 MHz A/D).

4.) If MBD is rev.C-C and later, IMMEM must be B-B (or later).

5.) RLY board FA200464 **must** be used only in systems with MBD rev.C-C or later and **together with** FEC board FA200764. The new FEC board requires SW V1.3.2 and onwards. If APA is supported, PRC must be rev. C-G and onwards.

6.) When the RFT1 board, FA200540 is used, the RFP piggyback is **not** used. The piggyback functionality is integrated onto FA200540.

7.) On Membership only: RX board FA200522 rev.A-D is required in order to support the 2.5 FPA rev.C probe in SW V1.4.

8.) RLY FA200434, FEC FA200764, PRC rev.C-G and onwards, MBD rev.C-C and onwards INTI/O rev.E-J and onwards is required for PAMPTE support from SW V1.4 and onwards.

9.) IV/DP rev.B-D and onw. is required for optimal 2MHz Pedof CW performance. The same revision + FEC FA200764 and MBD rev.C-C and onwards supports switchable PW and CW for the 6 MHz pencil probe from SW V1.4 and onwards.

10.) RX128 FA200776 and BF FA200765 can only be used from SW V1.5 and onwards, and only in Premium systems. The new RX board can be used together with BF FA200382, but BF FA200765 can only be used with the new RX FA200776. RX FA200776 requires FEC FA200669 or FA200764.

11.) SCONV rev. D-I requires SW V1.5 or later in order for the self test to pass. It will function well with older SW versions during normal operation, but the test will fail.

12.) V1.5 upgrade: GRAPH rev.A-H gives higher RGB output to better match live system RGB with playback S-VHS levels. NOTE: Monitor needs realignment. This rev. of GRAPH can be used in systems with older SW.
FP Audio amplifier rev.B-B with higher audio gain is required in V1.5.
NOTE that this rev. can be used with older SW versions, but the volume control knob must be turned down.

13.) RX64, FA200777, can only be used from SW V1.7 and onwards, and only in Membership systems. The new RX board can be used together with BF FA200538, but BF FA200811 can only be used with then new RX FA200777. RX FA200777 requires FEC FA200669 or FA200764.

14.) RX128, FA200907 can only be used from SW V1.7 and onwards, and only in Performance and Premium systems. The new RX board can be used together with BF FA200382 and FA200765, but BF FA200765 can only be used with the new RX FA200776 and FA200907. RX FA200907 requires FEC FA200669 or FA200764.

15.) Image Port 2, FA200572, plus the VME Jumper, FA200075, replaces the Image Port (IMPORT), FA200028, and the Image Memory (IMMEM / MEMORY) FA200110.The Scan Converter Board, FA200029, must be function rev. D or above.
Image Port 2 can only be used from system sw. v.1.8 and onwards.

16.) Part of the System FiVe Advantage High Framerate Kit, GEVU P/N FB200188. System sw.v.1.9 is included in the kit.

17.) FA200009 does not work with software v.1.8 and higher, due to memory allocation problems.

18.) Require a 64 Mbyte additional RAM, if Image Port 2 board is not present.

Macintosh HD:User:James:@i-arb:Service:S5_Service Man:S5_serv_files:H2_04_compat_c.17.
Printed: December 5, 2000.

6.2 RX/BF/FEC/MBD combinations

The table below shows the allowed RX/BF/FEC/MBD combinations:

SW Version	RX board	BF boards	FEC	MBD
Premium Systems				
From V1.0 to V1.7.1 and onwards	FA200022	FA200001	FA200009/ FA200669/ FA200764	All revisions
From V1.2.2 and onwards	FA200638	FA200382	FA200009/ FA200669/ FA200764	All revisions
From V1.5 and onwards	FA200776	FA200382/ FA200765	FA200669/ FA200764	Rev.C-C and onwards
From V1.7 and onwards	FA200907	FA200765	FA200669/ FA200764	Rev.C-C and onwards
Performance Systems				
From V1.6 and onwards	FA200776	FA200765	FA200669/ FA200764	Rev.C-C and onwards
From v1.7 and onwards	FA200907	FA200765	FA200669/ FA200764	Rev.C-C and onwards
Membership Systems				
From V1.2.2 and onwards	FA200522	FA200538	FA200669/ FA200764	Rev.C-C and onwards
From V1.7 and onwards	FA200777	FA200538/ FA200811	FA200669/ FA200764	Rev C-C and onwards
Advantage Systems				
From V1.6 and onwards	FA200522	FA200538	FA200669/ FA200764	Rev C-C and onwards
From V1.7 and onwards	FA200777	FA200538/ FA200811	FA200669/ FA200764	Rev C-C and onwards
From V1.9 and onwards	FA200777	FA200538/ FA200811	FA200669/ FA200764	Rev C-C and onwards
Advantage w/HFR (Advantage Systems w/High Frame Rate)				
From V1.9 and onwards	FA200777	FA200765	FA200669/ FA200764	Rev C-C and onwards
SYSTEM FIVE REM				
From V1.9.x and onwards	FA200907	FA200765	FA200764	Rev C-C and onwards

Your Notes:

128 vs. 256 channel systems

1 Hardware differences

Only valid for Premium and Membership.
Advantage is not upgradeable to Performance

Board	128-channel system	256-channel system	Notes
MBD	Rev. C - C or later	All revisions	RX64 support required for 128-ch. system
RX	RX64, FA200522 64 channels with mux. FA200777 (with muxes) 64 channels with CW doppler improvements	RX128, FA200022 (AD602) or FA200638 (AD604) or FA200776 (with muxes) 128 channels FA200907 (with muxes, new coils) 128 channels	FA200776 requires V1.5 and onwards. FA200777 requires V1.7 and onwards. FA200907 requires V1.7 and onwards.
BF	BF32 (1MLA), FA200538 (AD9042) or FA200811 (Burr Brown)	BF32 (2MLA), FA200001(AT&T) or FA200382 (AD9042) or FA200765 (Burr Brown)	FA200765 requires V1.5 and onwards.
FEC	FA200669 with RX64 mux support or FA200764	FA200009 or FA200669 or FA200764	FA200764 requires V1.3.2 SW and onwards. FA200009 does not work with sw. v1.8 and higher.
RFT	FA200373 without RFP p.b. or FA200574	FA200373 with RFP p.b. or FA200540	
RFP p.b.	Not installed.	FA200039 (old) or FA200555	
CFP	FA200409 (2 modules)	FA200027 (4 modules)	
XDCTRL (APA supp.)	Not standard, but can be installed	Standard	APA support requires special software.

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:H3_05_compat_d17.
Printed: December 5, 2000.

2 Probe Support Differences

Probe	128 channel systems
2.5 FPA, KG100001	Rev.A not supported
3.5 FPA, KK100001	Rev.A not supported
5.0 FPA (96 el.-small), KN100002	Rev.A not supported
5.0 FPA (128 el. -large), KN100001	Not supported
5.0 MPTE (Oldelft), KN100007	Rev.A not supported

All other probes are supported (depending on SW version). See Probe Support List in the Probe chapter (*page E2-1*) in this Service Manual for details.

Board Revision History

1 RLY, P/N: FA200020

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200020	A	A	-	Initial production release. Identical to rev. 06.
FA200020	B	B	6024	EMC modifications on print revision D.
FA200020	B	C	6157	New print revision (rev. E). Changes for improved EMC performance. Installed from system s/n 144.
FA200020	B	D	6396	Corrected doc. error on ASSY drawing.
FA200020	B	E	6995	PAL startup delay changed (R17)

2 RLY, FA200434

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200434	A	A	7577	Initial production release. PAMPTE support. **Must be used with FEC FA200764.** **Not compatible with FA200020.**
FA200434	A	B	8354	New PAL piggyback
FA200434	A	C	8701	New version of test procedure
FA200434	A	D	9104	New BM. New piggyback, with protection diodes on PRB_PRES lines. Piggyback has got its own BM.

Macintosh HD:User:James:@\-arb:Service:S5_ServiceMan:S5_serv_files:H4_06_compat_e.17.
Printed: December 5, 2000.

3 RLY, FA200870

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200870	A	A	8456	Release of new board without APAT support.

4 RLY-2, FA200890

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200890	A	A	8476	Release of new board without APAT support.
FA200890	A	B	9103	PAL piggyback is released as a “standalone”. Change in BM.

5 RLY–PAL-PB2, FA200799

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200799	A	A	9105	Doc. release. New piggyback used for ESD protection. Plugs into FA200890.

6 TX128, FA200021

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200021	A	A	-	Initial production release. Identical to MCD rev. 04.
FA200021	A	B	5785	Minor timing problem corrected (TXFBTSEQ PLD). No affect on the system performance.
FA200021	A	C	5985	New print revision (rev. C). Improved decoupling of high voltage supplies to reduce voltage drop on transmitted pulse in PW Doppler. No major impact on Doppler performance.
FA200021	B	D	6332	Modification: Analog +5V is used to power the digital circuitry on the board. Reduction of transmit noise in CW Doppler. Part of V1.1 upgrade.
FA200021	B	E	6397	The modifications above are implemented into the new print rev.D. Test points on HV supplies added.
FA200021	B	F	6738	Voltage rating of HV decoupling capacitors increased.
FA200021	B	G		Minor change in BM.
FA200021	C	H	7924	Changed p/n on hybrids.
FA200021	C	I	8183	New PCB. Obsolete 93 p female PCB conn.
FA200021	C	J	8622	New test procedure.

7 TX128-v2, FA200999

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200999	A	A	-	Initial release. New ASIC. (Replaces FA200021.) Requires SW.1.7.1 or higher.

8 RX128, FA200022

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200022	A	A	-	Initial production release. Identical to rev. 05

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200022	B	B	6383	Changes to test signal implementation. Necessary for CW improvement. Part of V1.1 upgrade. NOTE: R1595 changed from 22 to 10 ohm in V1.2 upgrade (no rev. change).
FA200022	C	C	5818	New component AD604 replaces AD602+CLC425

9 RX128, FA200638

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200638	A	A	7552	AD604 board. Adjusted test signal gain. **Must be used with BF p/n FA200382.**
FA200638	A	B	7640	Changed some capacitor to reduce 2D near field artifact with FLA probes.
FA200638	A	C	8186	New PCB. Obsolete 93 p female PCB conn.
FA200638	A	D	8448	Mod., remove noise from HPRF and CW. Change in BM.
FA200638	A	E	8628	New test procedure from Kitron (Vendor).

10 RX128-2, FA200776

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200776	A	A	8397	New board require v.1.5 and onwards. New muxes mounted.
FA200776	B	B	8525	New PCB. LC power supply filters on analog 5V removes noise in CW and HPRF

11 RX128-2, FA200907

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200907	A	A	8616	Initial production release of RX128-2 with improved power supply filtering. New SMD coils mounted.

12 RX64, FA200522

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200522	A	A	7273	For 64 channel system. Release of 64 channel board with multiplexers and AD604 TGC amplifier.
FA200522	A	B	7552	Changed values for R751 and R759 to reduce straight down noise in Color Flow.
FA200522	A	C	7641	Changed values for C449-C512 to reduce 2D near field artifacts.
FA200522	A	D	8081	Changed prom RXMUX to V1.1 to support 2.5 FPA rev.C probe.
FA200522	A	E	8190	Connector obsolete. Change PCB.
FA200522	A	F	8447	Added LC filter at analog 5V to remove noise from HPRF and CW.
FA200522	A	G	9533	New Test Procedure, Production test

13 RX64 v.2, FA200777

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200777	A	A	8595	New board for 64 channel system with LC filter mounted on board.
FA200777	A	B	9534	New test procedure.

14 PRC, FA200264

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200264	A	A	5874	Production release.
FA200264	A	B	5974	New artwork rev.C. Compatible with old rev.
FA200264	B	C	6444	Power distribution modification (+5V analog strap) to reduce transmit noise in CW Doppler. Removed ferrites on AA tx-channels to avoid oscillations in 2D (APAT only). Part of V1.1 upgrade.
FA200264	B	D	6504	The above modifications are implemented into artwork rev.D.
FA200264	B	E	7196	Revised board test procedure.
FA200264	B	F	7779	Changed value of fuses F1 and F2 to 5A and resistors R346, R347, R360 and R373 to 10k.
FA200264	C	G	7838	4 straps for support of new RLY, FA200434 and new FEC, FA200764.

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200264	D	H	7925	New p/n on hybrids.
FA200264	D	I	8163	Change artw PCB. P3 change from 93 to 185 pin.

15 Xducer Bus Board, FA200064

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200064	A	A	RD5722	Release.
FA200064	A	B	ED7538	Added ground strap in BM and new mod. instruction.
FA200064	A	C	ED7913	Ground strap removed.
FA200064	A	D	ED8717	Ground strap reintroduced.

16 XDCTRL, ML200078

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
ML200078				SW version V3.2-T6 or later to support mech. MPTE probe on System 5.

17 BF32 (2 MLA, 20 MHz A/D), FA200001

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200001	A	A		Initial production release. Based on FA208001, rev. 07.
FA200001	A	B		Removed unmounted comp. from ASSY.
FA200001	A	C	5836	Changed termination of test enable for ASICs.
FA200001	A	D		10 ground straps to avoid crackling noise in PW Doppler. Part of V1.1 upgrade.
FA200001	A	E	6808	New print to eliminate modification above
FA200001	A	F	6867	Corrected doc. error
FA200001	A	G	7034	New mod.instr. for BF heatsink.

18 BF32 (2MLA, 40 MHz A/D), FA200382

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200382	A	A	7440	Release of new board with AD9042 A/D converters. **Must be used with RX128 p/n FA200638.**
FA200382	A	B	7585	Two straps for using different A/D clock.

19 BF32 (1MLA, 40 MHz A/D), FA200538

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200538	A	A	7441	For 64 channel system. Release of new board with only 1 MLA and AD9042 A/D converters.
FA200538	A	B	7586	Two straps for using different A/D clock.

20 BF32 (2MLA), FA200765

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200765	A	A		First revision
FA200765	B	B		New ADC: AD5807
FA200765	B	C	8399	New ADC: AD5807E with 3 V input range.
FA200765	B	D	8723	Heatsink introduced.
FA200765	B	E	8806	Mod updated. Spacers changed to nylon. 6 GND straps removed.
FA200765	B	F	9253	New MOD. Heatsink on Beam-adder removed. A new heat-sink on the Focusor ASIC introduced. (Noise removal in Color Flow with the CLA probes.)
FA200765	B	G	9545	MTP updated. DC Offset calibration and ADC bit test included.

21 BF32 (1MLA), FA200811

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200811	A	A	8475	First revision. Based on FA200765, rev. C, with 1 MLA. To be used together with FA200777, RX64 v.2.
FA200811	A	B	9417	New MOD. Heatsink introduced

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200811	A	C	9817	Improved decouplingin order toremove noise in Doppler and FPA probes.

22 FEC, FA200009

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200009	A	A		Initial production release.
FA200009	B	B		Test signal modification in order to get correct signal level for the test signal to the RX128 board. Necessary for CW improvement. Part of V1.1 upgrade.
FA200009	C	C		Changed “VMEIF2” from v1.0 to v1.1
FA200009	D	D		Mod. for reduction of near field color noise with FLA probes.
FA200009	E	E	7680	Updated MCD. Noise reduction in 2D for some CLA and FLA probes. (Corrected polarity on the signal PMX_LE_L from FPGA U918 to Probe Mux.) SPAs changed from V01 to V02.

23 FEC, FA200669

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200669	A	A		For 64 channel system. Release of new board with support for RX64 board with multiplexers.

24 FEC, FA200764

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200764	A	A	7917	For all systems. Release of new board. Built-in temp.sense and probe sense support. Requires SW V1.3.2 or onwards.
FA200764	A	B	8018	New SCD
FA200764	A	C	8192	Mod for JTAG.
FA200764	A	D	8543	Check of components legs.
FA200764	A	E	8676	ECL mod. U114.
FA200764	A	F	8832	Doppler noise MOD. Temp Sense Fix.
FA200764		G	9120	New PCB

25 RFT, FA200373

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200373	A	A	FA302024	D		Release of doc.
FA200373	B	B	FA302024	D		INCTL pld V1.0 -> V1.1, this change fixes a design error in CW Doppler.
FA200373	C	C	FA302024	D		CTLPLD3 V1.0 -> V1.1, fix read failure from FE fifo on some boards with TMS320C31 date code ED-55A900W RFTB V1.1 -> RFTB V1.2)
FA200373	D	D	FA302024	D		More gain in spectrum Doppler. More gain selections in the SATSP pld. New version
FA200373	E	E	FA302024	D		C801 (47pF) -> 130 ohm R813 New 120 ohm Strap pin 33 to pin 61 on U601. Stability problem due to change of external RAM vendor fixed.
FA200373	E	F	FA302024	D	ED 7407	Doc. change only.
FA200373	F	G	FA302024	D	ED 7460	Change in software PAL. Pltest from v.1.0 -> v.1.1.

26 RFT1 - 2 MLA, FA200540

P/N:	Func Rev:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200540	A	A	FA302540	B	7855	Release of new board with 2 MLAs on-board (piggyback implemented on main board). Requires SW 1.3 or higher. (Introduced Nov.1997)
FA200540	E	B	FA302540	B	7922	Local sw on the RFT1 board use the functional version to adjust it's control of the board. It did not handle func. rev. A correctly. The default func. rev. in the sw was E, and that version handles the board correctly also. (Note that RFT FA200373 func. rev. F was the basis for the RFT1 board, so selecting func. rev. E is questionable, but was done to make the change as simple as possible).
FA200540	E	C	FA302540	B	7999	A small fix. so RFT1-NOMLA can be detected. New version of DCD (07-08)

P/N:	Func Rev:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200540	E	D	FA302540	C	8074	Changed PCB to accept 300mill wide SRAM's (400mill becomes obsolete)
FA200540	E	E	FA302540	C	8379	Changed FCT574 to ABT574 to normalize vs. FA574 (same board but not fully populated)
FA200540	E	F	FA302540	C	8509	Change all MACHxx0 to MACHxx1 due to cost reduction. Make Logic Devices components as an second source for Harris.
FA200540	E	G	FA302540	C	8869	Noise in CW and M mode on some boards. Caused by use of Lattice instead of Vantis PAL. Fixed by new termination on iq-buffer. Hang of system on some boards, caused by limitations in the synchronous fifo design, fixed by change of: ctlpld3 V2.1 -> V2.2 ctlpld4 V2.1 -> V2.2
FA200540	E	H	FA302540	D	9005	New PCB. BM changes.
FA200540	E	I	FA302540	D	9201	MOD introduced in order to avoid problems caused by fpga's switching to test-state. Termination of boundary scan test signals on U470, U475, U480, U485, U772.
FA200540	E	J	FA302540	E	9508	New PCB. MOD removed/included in PCB. New version of DCD (10-11).
FA20054	E	I	FA302540	E	9509	New PCB rev E. MOD removed/included in PCB.

27 RFT1-NO MLA, FA200574

P/N:	Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200574	E	A	FA302540	B	7999	Release of new board with 1 MLAs only. For 128 ch. systems only. Requires SW V1.3 or higher. Func rev E selected for compatibility with all RFT boards.
FA200574	E	B	FA302540	C	8075	PCB Release. Rev. C due to new SRAMs. No functional change.
FA200574	E	C	FA302540	C	8331	BM change. FCT to ABT, No functional Change.

P/N:	Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200574	E	D	FA302540	C	8510	0Change all MACHxx0 to MACHxx1 due to cost reduction. Make Logic Devices components as an second source for Harris.
FA200574	E	E	FA302540	C	8728	New MOD: Termination of DCLK.
FA200574	E	F	FA302540	C	8870	Noise in CW and M mode on some boards. Caused by use of Lattice instead of Vantis PAL. Fixed by new termination on iq-buffer. Hang of system on some boards, caused by limitations in the synchronous fifo design, fixed by change of: ctlpld3 V2.1 -> V2.2 ctlpld4 V2.1 -> V2.2 Remove all GND straps and test points.
FA200574	E	G	FA302540	D	9006	New PCB. SW800 removed. BM changed.
FA200574	E	H	FA302540	D	9202	MOD introduced in order to avoid problems caused by fpga's switching to test-state. Termination of boundary scan test signals on U470, U475.

28 RFP, FA200039

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200039	A	A	FA302039	B		Release of doc.
FA200039	A	B	FA302039	B	ED 7001	Change Assy P1/P2.
FA200039	A	C	FA302039	B	ED 7408	Doc. change only.

29 RFP, FA200555

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200555	A	A	FA302555	A	ED 7352	Release of doc.

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200555	A	B	FA302555	A	ED 7485	SCD Rev. A -> B. (Typing errors).

30 SDP, FA200026

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200026	A	A	FA302026	C	5897	Production release, same as rev. 02.
FA200026	A	B	FA302026	C	5991	PLD change, corrected data buffer timing.
FA200026	A	C	FA200026	C	5991	PLD change. Corrected pipelink register timing.
FA200026	A	D	FA302026	C	6257	Changed resistors R4-R6, R17, R37-R40 to correct intermittent problems with the ECL clocks causing intermittent Doppler lock-up problems. Part of V1.1 upgrade.
FA200026	A	E	FA302026	C	6603	Corrects a lock-up problem in Duplex/Triplex Doppler. Part of V1.1 upgrade.
FA200026	A	F	FA302026	C	7373	PLD change.
FA200026	A	G	FA302026	D	8197	New PCB.
FA200026	A	H	FA302026	D	9325	New SCD.
FA200026	A	I	FA302026	D	9448	U122 and U123 changed to 74ABT574.
FA200026	A	J	FA302026	D	9477	New Actel, XL cost reduction.

31 CFP (4 modules), FA200027

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200027	A	A	FA302027	C	5931	Release of documentation Functional revision 08 -> A.
FA200027	A	B	FA302027	C	5994	Added termination networks on VELFIFO read. Fixed timing error on the M_INT1_L signal (masc)
FA200027	A	C	FA302027	C	6275	Added termination networks on VSTRB_L. Corrects an intermittent color lock-up problem. Part of V1.1 upgrade.

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200027	A	D	FA302027	C	9478	New actels, Cost reduction

32 CFP (2 modules), FA200409

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200409	A	A	FA302027	C	7531	Release of board with only two processing modules (instead of four).
FA200409	A	B	FA302027	C	9479	New Actels,cost reduction

33 IMPORT, FA200028

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200028	A	A	FA302028	C		Release of module.
FA200028	A	B	FA302028	C		Mod:
FA200028	A	C	FA302028	D	6213	New artwork, piggyback removed. Not used.
FA200028	A	D	FA302028	E	6699	New artwork without p.b.
FA200028	A	E	FA302028	E	7042	Corr. for production.
FA200028	A	F	FA302028	E	7725	New BM and PCB.

34 Image Port 2, FA200572

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200572	A	A	FA302572	F	8699	First release version. Replaces Fa200028 and FA200110.
FA200572	A	B	FA302572	F	8960	New software (pfwxctl.jed)
FA200572	A	C	FA302572	F	9368	New SCD, (IPflashboot).

35 SCONV, FA200029

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200029	A	A	5933	Release version.
FA200029	A	B	6092	Simple fix of noise on PBGNT1_B signal due to ground bounce during D64 VME accesses.
FA200029	B	C	6330	Fix of pixel port error, extra functionality in ENCCTL for speed gain.
FA200029	B	D	6380	Removed MOD (resistor-capacitor filter) since the noise due to D64 VME block accesses was found to be at the IMEM board. Part of V1.1 upgrade.
FA200029	B	E	6758	New SCD due to error in D64 block transfers. New MTP.
FA200029	B	F	6817	New SCD due to error in TDP FENC test.
FA200029	C	G	7084	New print with full video format and new DDP filter.
FA200029	C	H	7962	New FPGA type.
FA200029	D	I	8352	New components to reduce cost.
FA200029	D	J	9562	New SCD due to Power up error in DTBCTL
FA200029	D	K	9781	New Print and added JTAG programming

36 GRAPH, FA200030

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200030	A	A	FA302030	C	5981	Released version.
FA200030	A	B	FA302030	C	6124	Changed VME_MS and VME_RI from V1.0 to V1.1
FA200030	A	C	FA302030	C	6124	Part of V1.1 upgrade.
FA200030	A	D	FA302030	C	6739	Oscillator for NTSC video changed to 12272725 Hz
FA200030	A	E	FA302030	C	6986	VxWorks label added.
FA200030	A	F	FA302030	C	7083	PLD change (Pentium only)
FA200030	A	G	FA302030	D	7866	ASSY, CD, DRILL, PCB, BM, SCD, DCD updated
FA200030	A	H	FA302030	D	8339	Video improvement. Change BM
FA200030	A	I	FA302030	D	9094	Change BM, R72 Introduced
FA200030	A	J	FA302030	D	9137	Change BM. Latchup fix. Removed un-used RAM.
FA200030	A	K	FA302030	E	9181	New PCB. Change BM.

P/N:	Func Rev.:	MCD rev.:	PCB P/N:	PCB Rev.:	C/N:	Change description:
FA200030	A	L	FA302030	E	9681	New SCD.
FA200030	A	M	FA302030	E	9821	New SCD(VMS RI/FBPP TX

37 IMMEM (MEMORY), FA200110

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200110	01	N/A	N/A	Added to enable the possibility of further changes. This version is not necessary for the production of the board.
FA200110	A	A	6378	Update of firmware on previously delivered boards. This revision corrects a VME bus problem known to cause a 2D lock-up. Part of V1.1 upgrade.
FA200110	B	B	7353	Cut all pins on P2, row a and c. **Must be used when MBD is rev. C-C and onwards.**

38 CPU, FA200109

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200109	A	A	---	Release of document.
FA200109	A	B	6987	Vxworks label added.

39 INT I/O, FA200103

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200103	A	A	5905	Release of doc.
FA200103	A	B	6067	Correction of BM error.
FA200103	B	C	6122	New artwork rev. C.
FA200103	C	D	6328	Modification on SWPWOF_L signal.
FA200103	C	E	6813	Fix RDYINTF, updated test procedure.
FA200103	C	F	6847	New PROM for test of new Pat I/O.
FA200103	C	G	7068	Updated test procedure.
FA200103	E	I	7368	New PCB with 3D Pos Det and VMS PAMTPE support.
FA200103	E	J	7665	Improved PAMPTE support.
FA200103	E	K	8039	Fix of power on problems.

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200103	E	L	8315	The correct MTP is rev E and new ASSY (explain dips for MAC).

40 EXT I/O, FA200104

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200104	A	A	RD 5956	Release of doc.
FA200104	B	B	CN 6123	New artwork rev.C.
FA200104	C	C	ED 8465	New artwork rev.D. New components to accommodate UL specifications.

41 Patient I/O Main Board, FA200193

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200193	A	A	5908	Release of doc.
FA200193	A	B	6141	Removed transient suppressor.
FA200193	B	C	6333	New print rev.E with new DC-DC converter. For EMC purposes.
FA200193	C	D	6993	Removed the unused A/D converter.
FA200193	C	E	7084	Corrected pull up in BM and MOD
FA200193	C	F	8312	Doc. change.
FA200193	C	G	9347	Included CD, new DCD.

42 ECG/Phono module, (Patient I/O Amplifier Board), FA200194

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200194	A	A	5909	Release.
FA200194	B	B	6387	C3 and C7 changed to 33nF
FA200194	C	C	6846	R7 changed to 4k7 (reduced ECG gain).
FA200194	D	D	6497	New PCB - rev. C.
FA200194	D	E	7959	Changed R1 and R2 back to 38 Mohm

P/N:	Rev.:	MCD rev.:	C/N:	Change description:
FA200194	D	F	8148	New Artwork. Increased ECG contact pin diameter
FA200194	D	G	8311	Separated MTP from FA103. PCB rev. D was not listed in MOD instruction.
FA200194	D	H	9350	New BM and DCD,included CD. MTP moved up one level. Connectors changed.

43 HV Power Supply Board, FA200063

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200063	A	A	6200	Release of doc. Both HV1 and HV2 have extended shutdown limits compared to older versions.
FA200063	A	B	6262	Included fuse labels onto the board/box.
FA200063	A	C	6861	Corrected doc. error. **NOTE: R74 -> 22k and R66 -> 33k per V1.2.2 upgrade procedure**.
FA200063	A	D	7166	Added protection zener diodes. Increased maximum power limit.
FA200063	A	E	8685	Introduced FA200982 as repl. for 012E2208.
FA200063	A	F	8772	Increased power for HV1/HV2 to 12W.

44 AC Controller Board, ACCTRL, FA200107

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200107	A	A	5907	Release of doc.
FA200107	B	B	7019	Changed R203 to increase default fan speed.
FA200107	B	C	7091	New print. Added heat sink to diodes.
FA200107	B	D	7584	Changed R203. Decreased fan voltage (fan speed).

45 FP Main Board-2, FA200191

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200191	A	A	5704	Release of doc.
FA200191	B	B	5782	New artw. FA302191A with better power filtering and grounding.
FA200191	C	C	6120	New SW V3.1 (for old artw. FA302055C).

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200191	D	D	6121	New SW V3.1 (for current artw. FA302191A), 1 new jumper.
FA200191	E	E	6319	4 new capacitors for trackball filt. (on FA302055C). Part of V1.1 upgrade.
FA200191	F	F	6320	4 new capacitors for trackball filt. (on FA302191A). Part of V1.1 upgrade.
FA200191	G	G	ED7454	Changed SW to V3.2. (It is not necessary to upgrade old systems with this PROM.)
FA200191	H	H	ED7728	Changed SW to V3.3.
FA200191	I	I	ED7733	New trackball bracket. New artwork. Removed mod's.
FA200191	I	J	ED7916	New paddles & trackb. switches. Support bracket for paddles impl.
FA200191	J	K	ED8409	New FP-sw; V3.4.
FA200191	J	L	ED8514	MTP added in Ref. Other Doc.
FA200191	J	M	ED8532	Change in Mounting Instructions.
FA200191	K	N	ED8653	New FP-sw; V4.0.
FA200191	K	O	ED9062	Change of FA307780.
FA200191	L	P	ED9156	New FP-sw; V4.2. Self test modified. Part of "On/off control for LCD screen".
FA200191	M	Q	9549	New FP-sw; V4.3.
FA200191	M	R	9805	Paddle switches changed and new support bracket (FB762).

46 FP Rotary & Display Board, FA200057

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200057	A	A	RD5702	Release.
FA200057	A	B	CN6377	New artwork. Holes grounded.
FA200057	A	C	ED8511	Updated "Ref. other doc."

47 FP Rotary & Display Board, FA200682

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200682	A	A	7681	Release of board for int. MAC support (3" LCD power connector).
FA200682	A	B	8512	Updated "Ref other doc" in this MCD.

48 FP Rotary & Display Board 3, FA200989

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200989	A	A	8698	Initial release. Replaces FA200682. Output voltage, VR1 is 12 VDC. To be used for 4” LCD screen on Front Panel.

49 FP Rotary & Display Board 4, FB200177

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FB200177	A	A	9158	Initial release. Replaces FA200989. To be used for 4” LCD screen on Front Panel. Includes power control (on/off) for the LCD screen.

50 FP Audio Amplifier board, FA200076

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200076	A	A	5703	Doc. release.
FA200076	B	B	8386	R1 and R3 changed to 4K7.
FA200076	B	C	8446	MTP added in Ref. Other Doc.
FA200076	B	D	8640	Modification of Heatzink TO-220.
FA200076	C	E	8705	New artwork, D. Input relay added. (Artwork C is not for use.)

51 Motherboard, MBD, FA200046

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200046	A	A	5726	Release.
FA200046	B	B	6313	Added +5V analog straps to TX128 slot for CW noise reduction purposes. Part of V1.1 upgrade.
FA200046	C	C	7341	New artw. E which supports RX64 and the Vingmed PAMPTE probe.

52 IV & DP Connector Board, FA200248

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200248	A	A	5902	Documentation release.
FA200248	A	B	6093	New artwork rev.C
FA200248	A	C	6503	New artwork rev. D with studs for improved mounting.
FA200248	B	D	7228	New artwork rev.E with 2 MHz Pedof filter. Requires V1.2 SW or newer. **Optional V1.2 upgrade**.
FA200248	B	E	7900	Changed R6 to 100 ohm to reduce saturation with 2 MHz Pedof probe.
FA200248	B	F	8184	PCB. 064E5010 "Conn. PCB female 93p." is obsolete.

53 VME BG/IACK Jumper (VME Jumper), FA200075

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200075	A	A	RD5723	Release.

Your Notes:

Power Supply Revision History - rev. 01

1 DC Power, FA200034

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200034	A	A	RD5919	Doc Release
FA200034	A	B	ED7906	Mechanical fastening change
FA200034	A	C	ED7921	Decreased 5Vd current from 150 to 120A
FA200034	A	D	ED7996	New 5Vd module incl. PFC./100A
FA200034	A	E	ED9155	Improved +12V regulation.

2 AC Power Supply, FA200231

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA20023	A	A	7636	Doc release
FA20023	A	B	8191	Index-1 = 115V, Index-2 = 100V. A. 0V. Added Fan Kit; P/N: FA200706
FA20023	A	C	9139	Changed AC mains cable.
FA20023	A	D	9196	Changed VCR lable to FB314164.

3 AC Power Supply, Complete with Box, 220 VAC,

Macintosh HD:User:James:@\-arb:Service:S5_ServiceMan:S5_serv_files:H5_07_compat_e.17.
Printed: December 5, 2000.

FA200040

P/N:	Rev.	MCD Rev.	C/N:	Change Description:
FA200040	A	A	5910	Doc release
FA200040	A	B	6260	Labels included
FA200040	A	C	7219	Moved label FA314390 and fuse to FA200107
FA200040	B	D	7734	New current limiter, FA200558
FA200040	B	E	7847	Mod. of FA307040. Incl. mech dwg
FA200040	B	F	7905	Changed mech.dwg. FA307120 and FA307412
FA200040	B	G	8257	Corrected measurements
FA200040	B	H	8623	Changed mech. drwg. FA307040
FA200040	B	I	8730	Introduced 4 slots for power cable lock
FA200040	B	J	9197	Changed VCR lable to FB314166.

4 HV Power Supply Board, - FA200063

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200063	A	A	6200	Doc release
FA200063	A	B	6262	Labels included.
FA200063	A	C	6861	Doc error. Incorrect CD revision.
FA200063	A	D	7166	Increased power Added two zener diodes.
FA200063	B	E	8685	Introduced FA200982 as repl. for 012E2208.
FA200063	C	F	8772	Increased power for HV1/HV2 to 12W

5 HV Power Supply Subassembly (Box), FA200114

P/N:	Rev.:	MCD Rev.:	C/N:	Change Description:
FA200114	A	A	5915	Doc Release
FA200114	B	B	7670	New mounting frame (FA307509)
FA200114	C	C	7746	Use of old VERO box (FA200118).

SYSTEM FIVE Revision Req. List

Reference

This list has been included in Chapter H.
Please refer to “Board Compatibility List” on page H1-1.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:I_01_Innh.
Printed: December 5, 2000.

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SYSTEM FIVE Troubleshooting Guide

Overview

Introduction

This part of the SYSTEM FIVE Service manual describes how to troubleshoot the instrument.

Describsions in this part of the manual

The following describsions are included in this part of the manual:

Chapter	Description	Page
1	Introduction	K01-1
2	Minimum Boot Configuration	K02-1
3	Faults Diagnosis	K03-1
4	Test- and Setup Procedures	K04-1
5	LEDs	K05-1
6	Test Connectors	K06-1
7	Booting Sequence	K07-1
8	Introduction to Test Software Guide	K08-1
9	Board Tests via External Terminal/PC	K09-1
17	Power-up Test	K10-1
18	Performance Test (System Test) Procedure	K11-1
19	Lock-ups and Bus Errors	K12-1
20	System FiVe Noise Guide	K13-1
21	Fuses and Circuit Breakers	K14-1
22	Voltage Distribution Overview	K15-1
23	FE "Calibration" Procedure	K16-1
24	Debug Commands	K17-1
25	Monitor Setup Procedures	K18-1

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K00_TroubleshootGuide.13.
Printed: December 5, 2000.

Your Notes:

Troubleshooting Guide – rev. 15

1 Introduction

1.1 Abstract

The purpose of this guide is to give the field service engineer help with troubleshooting different problems that might occur with the system.

1.2 Document History

Rev.	Date	Sign.	Description
11	10 Nov 1998	GRL	Updated according to V1.5 release.
12	30 Sep 1999	LHS	Added some missing Part Numbers. Minor lay-out changes. Divided section in several separate files. Updated Part Numbers. Updated the LED section. Added Boot Sequence for sw. v.1.8. Replaced the System Test. Updated the FE Calibration Procedure.
13	10 Nov 1999	LHS	Updated per sw.v.1.7.1 (and 1.8) release.
14	20 Dec 1999	LHS	Updated per sw.v.1.9 release. Removed boot-sequences for v.1.2, v.1.3 and v.1.5.x.
15	June 2000	LHS/ JB	Updated per 1.9.x release

1.3 Abbreviations

Please refer to the Abbreviations, Definitions, Glossary, Terminology, Nomenclature list starting on page P-1.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K01_Intro.15.
Printed: December 5, 2000.

Your Notes:

2 Minimum Boot Configuration

2.1 Minimum Board Configuration for System to Boot

In order to get the system to boot to the so-called "no-mode" screen, the below listed boards/parts are required. (**NOTE**: No probes must be connected).

- *CPU* board
- *GRAPH* board
- *SCONV* board
- *FEC* board (generates clocks for GRAPH).
- *INT I/O* (link between disks/ethernet and CPU, and required for on/off switching).
- *Patient I/O box*
- *Front Panel*
- *RFT* (must be in since we have no VME jumpers to install in this position).
- Hard disk with system software or connection to ethernet with server/MAC/PC with system software.

If you wish to run the system in 2D mode, the below boards must be added to the list.

- *BF4* (can be left out if there are no probes connected during power-up).
- *IMMEM* (can be left out if there are no probes connected during power-up).

If you want to use the system for any **test purposes**, the following parts are also required:

- *EXT I/O* (is required only when booting from ethernet or if you want to connect a terminal to the RS-232CPU connector).
- *Terminal or PC* (is required if you want to connect to the RS-232CPU connector on the External I/O board.)

The following boards can be left out without having to do any special modifications:

- RLY,
- TX128,
- RX,
- PRC,
- BF1, BF2, BF3 and BF4,
- HV-Supply.

If the following boards are pulled out, VME jumpers FA200075 must be installed in the P1 (upper) connectors:

- SDP,
- CFP,
- IMPORT, IP2
- IMMEM

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K02_MinimumBoot.14.
Printed: December 5, 2000.

2.2 Minimum Cable Configuration for System to Boot

The following cables must be connected between the INT I/O board and the rest of the system:

- SCSI-cable to harddisk.
- Patient I/O cable to Patient I/O box.
- I/O RS-232 GR1 serial cable to front panel.
- ACCTRL cable between INT I/O and ACCTRL (power-on signal).
- DC Power cable to harddisk
- DC Power cable to front panel.

All other cables including MAC cables, can be removed and the system will still boot.

3 Faults Diagnosis

3.1 Instructions on How to Use This Chapter

1. Find the observed problem in Fault Classification Overview which follows below.
2. Then, in the detailed fault diagrams, find the symptom description which matches the failure. Follow the suggested sequence of troubleshooting. Retest after each replacement of parts.
3. If the problem still exists after all recommended parts have been tested/replaced, contact technical support.

3.2 Fault Classification Overview

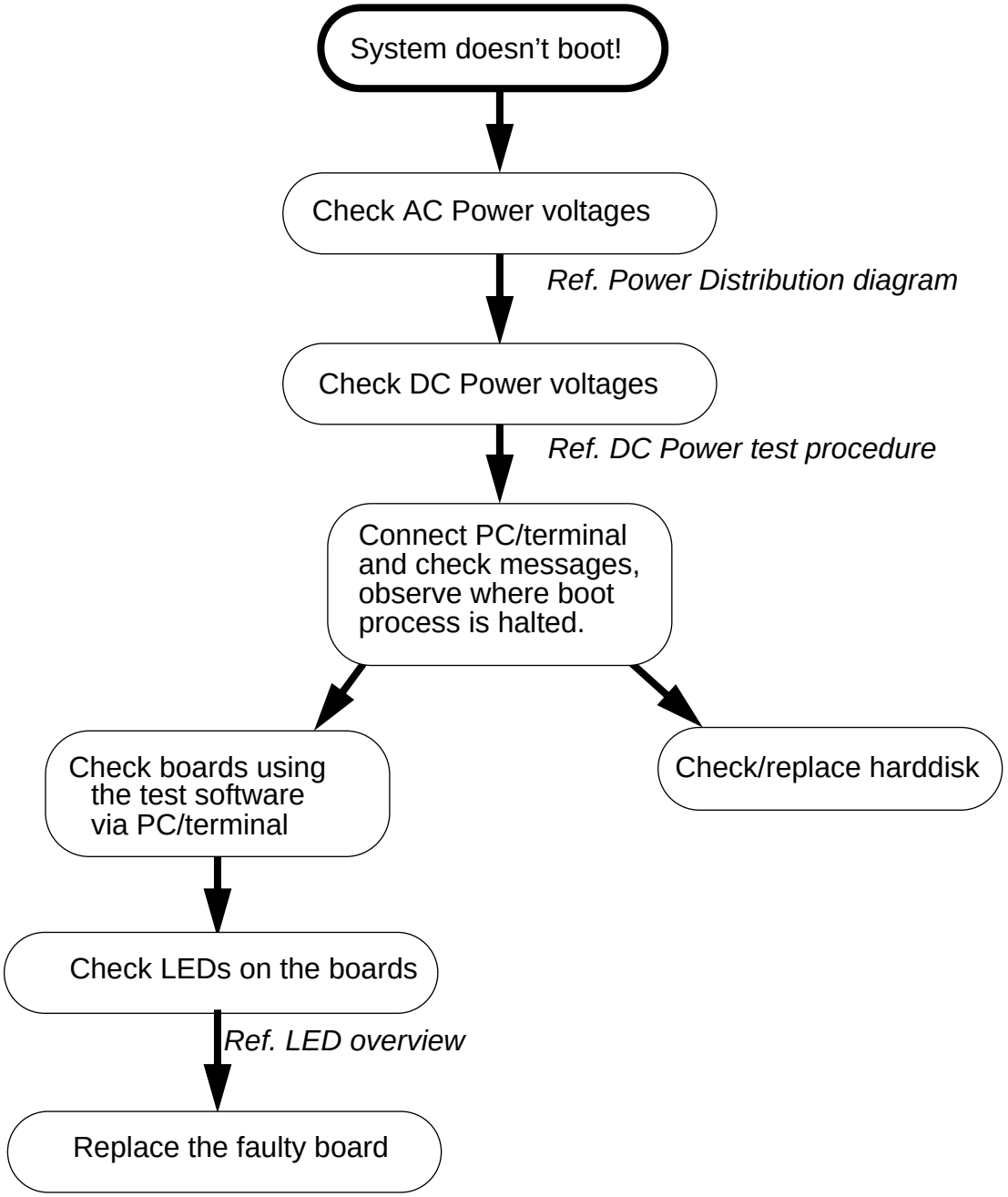
- Start-up Problems K03-2
  - System Doesn't Boot K03-2
  - Start-up Problems, AC Power Related. K03-3
  - Start-up Problems, DC Power Related (AC Power ok). K03-4
  - Start-up Problems, System Doesn't Boot, Possible Harddisk Problem.K03-5
  - Start-up Problems, System Doesn't Boot, Possible Board Problem. . K03-6
- Display Problems K03-7
  - No Display on Monitor, System Appears to Have Booted. K03-7
  - No Display in the Image Field K03-8
  - Data in Image Field Frozen K03-9
  - Only Noise in image Field K03-10
- Peripheral Problems K03-11
  - VCR Related Problems K03-11
  - Printer Problems. K03-13
- Front Panel Problems K03-14
  - No Response to Front Panel Controls K03-14
- Probe Problems. K03-15
  - Probe Recognition and Switching Problems K03-15
  - AA Probes Do Not Run K03-16
- Specific 2D Problems K03-17
  - "Frozen" images, Images with Artifacts K03-17
  - "Pulsing" or Fading Image K03-17
  - Noisy Images (also see Noise Guide Chapter) K03-17
  - Poor Image Quality. K03-18
- Specific M-Mode Problems K03-19
- Specific Color Flow problems K03-19
  - No Color Flow (2D ok) or Frozen Color Flow K03-19
  - Noise Problems (Also see Noise Guide Chapter) K03-19
  - Poor Flow Quality K03-19
- Specific Color M-Mode Problems K03-19
- Specific Doppler Problems K03-20
  - No Doppler (2D ok) K03-20
- Specific Doppler Problems K03-20
- Analog Traces (ECG, Phono, Pressure, Respiration) K03-20
- Misc. Problems K03-21
  - Fan Related Problems K03-21
  - AC Power Heating Problems (System Shut-down) K03-21
  - Power Switch Problems K03-22

Macintosh HD:User:James:@i-ant:Service:S5_ServiceMan:S5_serv_files:K03_Diagnosis:13.
Printed: December 5, 2000.

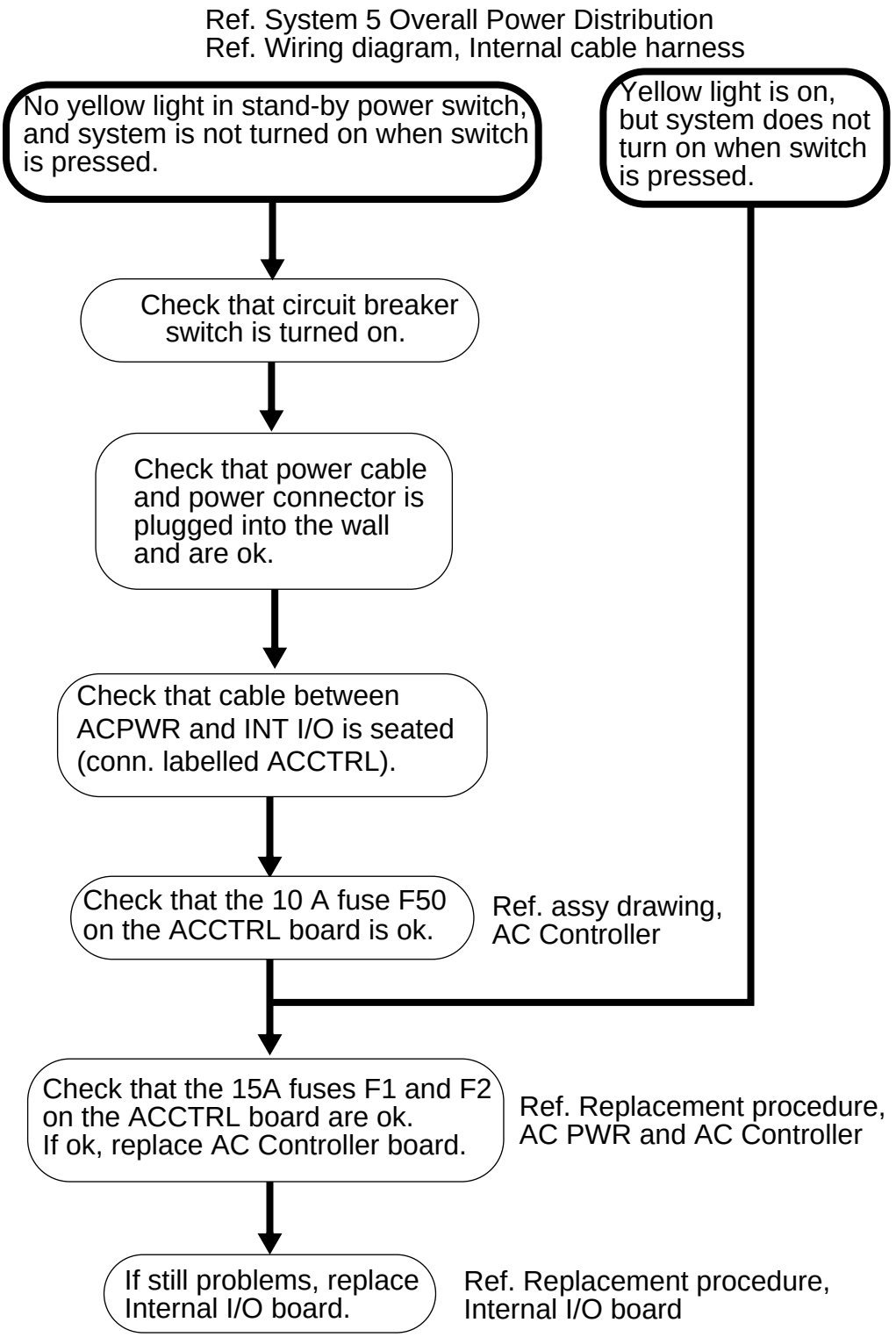
3.3 Start-up Problems

3.3.1 System Doesn't Boot

This is an overall diagram showing a recommended sequence for troubleshooting a no-boot situation.

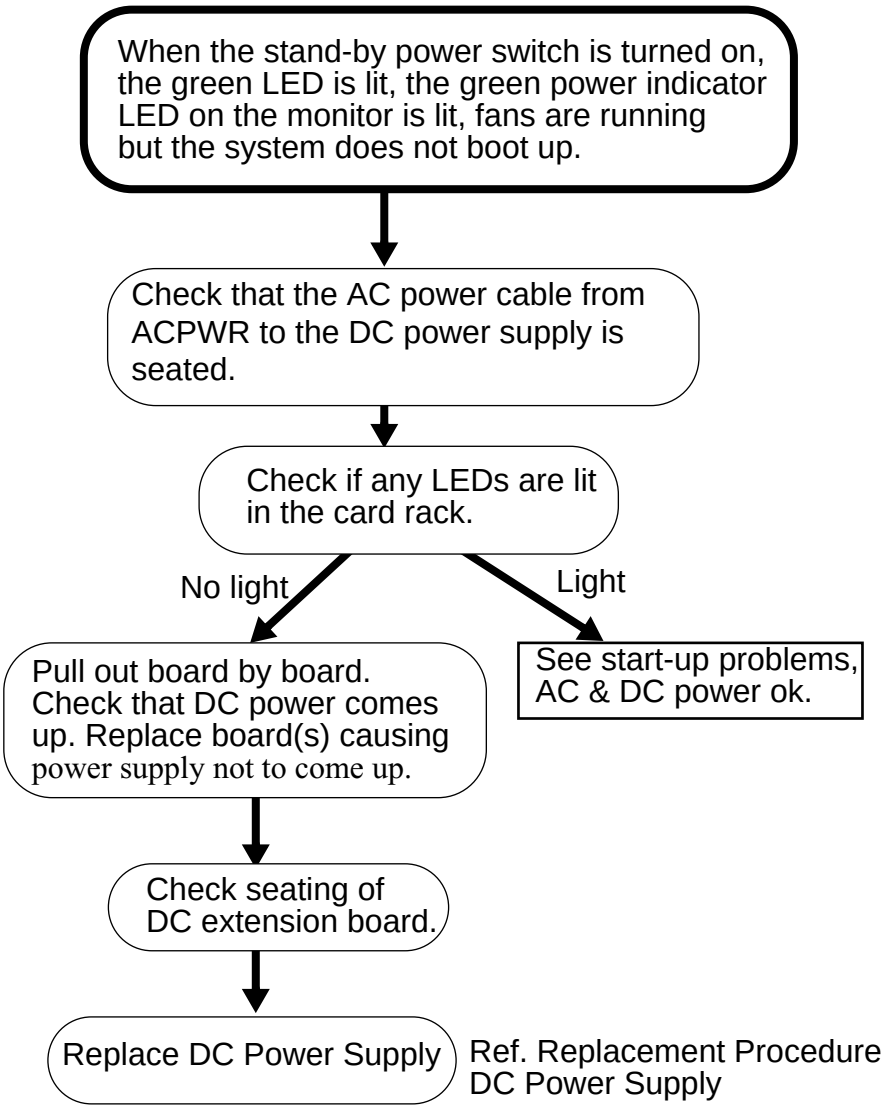


3.3.2 Start-up Problems, AC Power Related

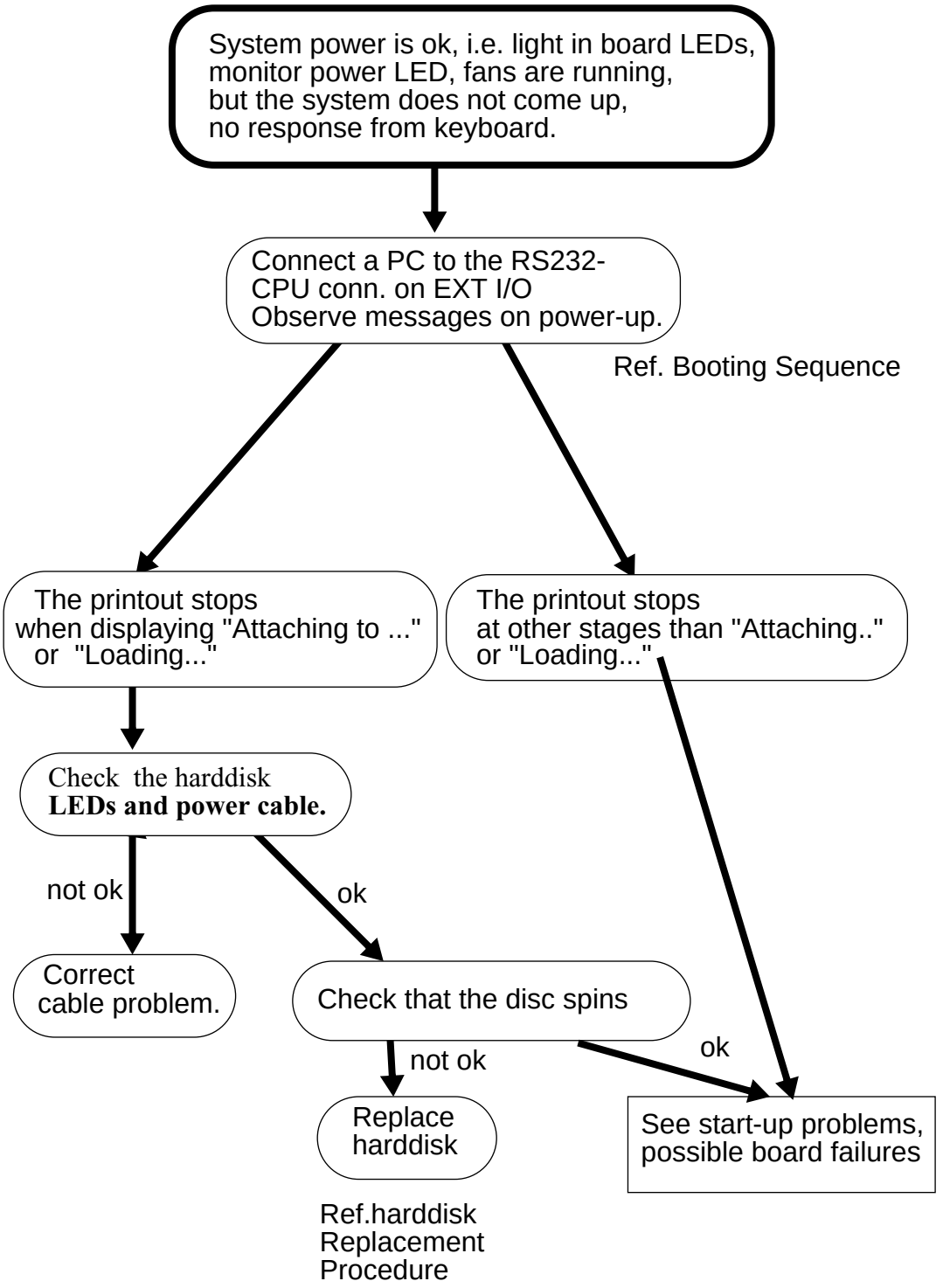


3.3.3 Start-up Problems, DC Power Related (AC Power ok).

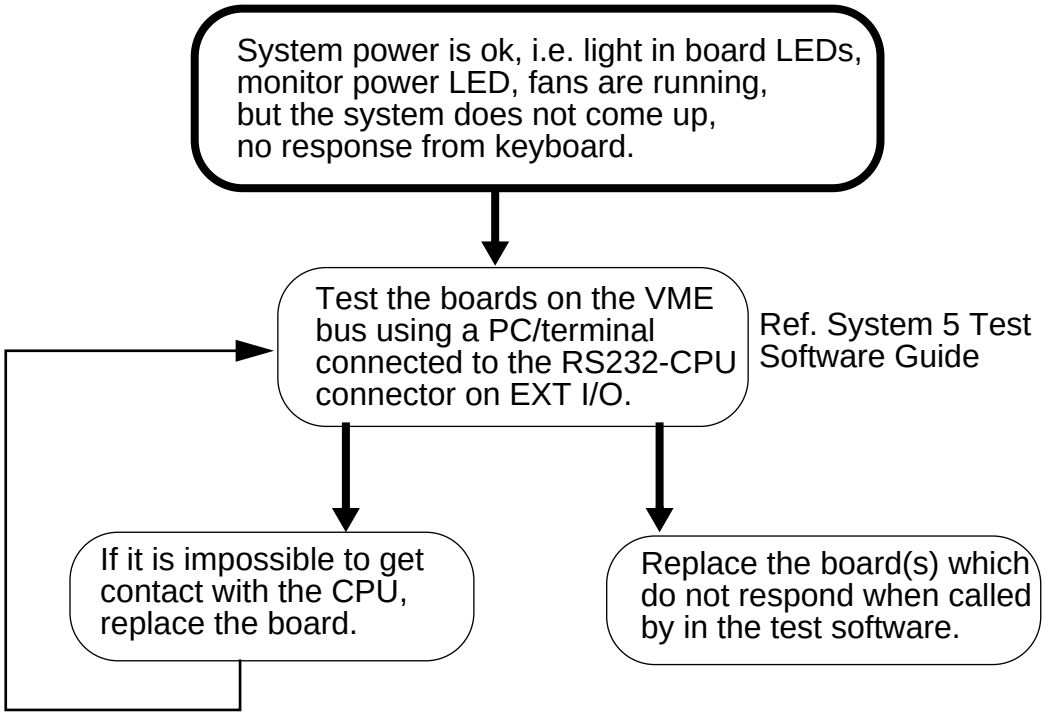
Ref. System 5 Overall Power Distribution
Ref. Wiring diagram, Internal cable harness



3.3.4 Start-up Problems, System Doesn't Boot, Possible Harddisk Problem.



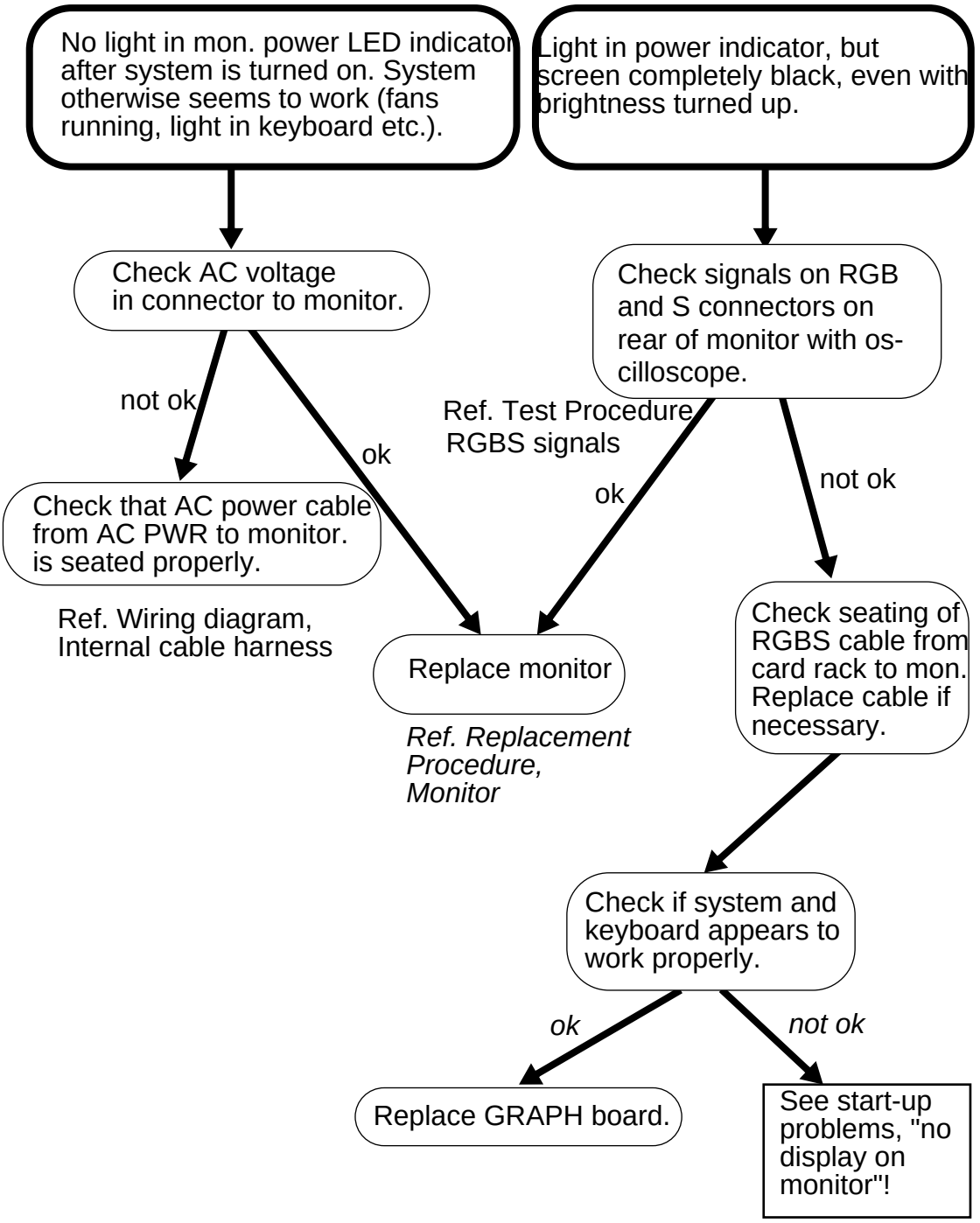
3.3.5 Start-up Problems, System Doesn't Boot, Possible Board Problem.



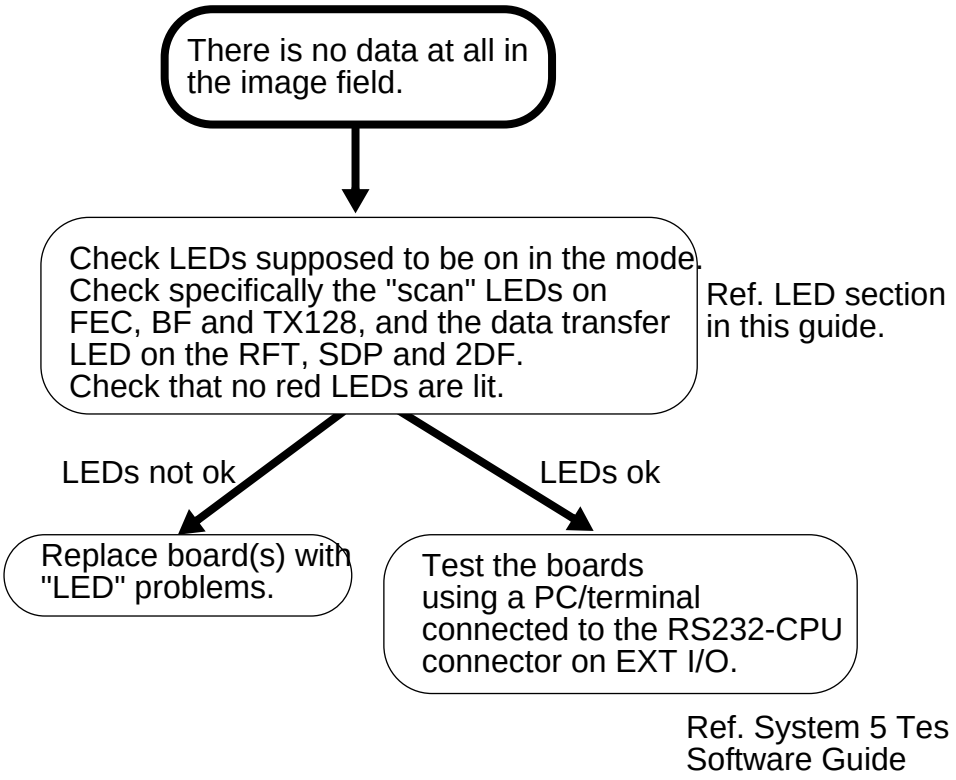
3.4 Display Problems

3.4.1 No Display on Monitor, System Appears to Have Booted.

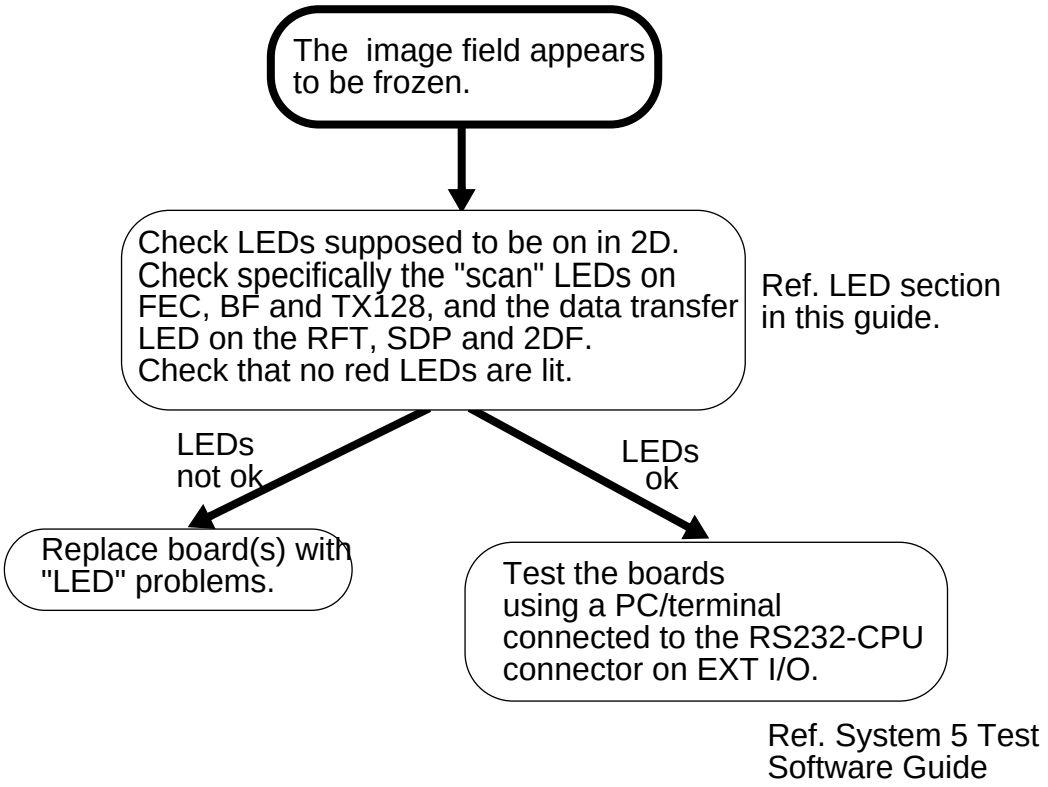
(Monitor display is black)



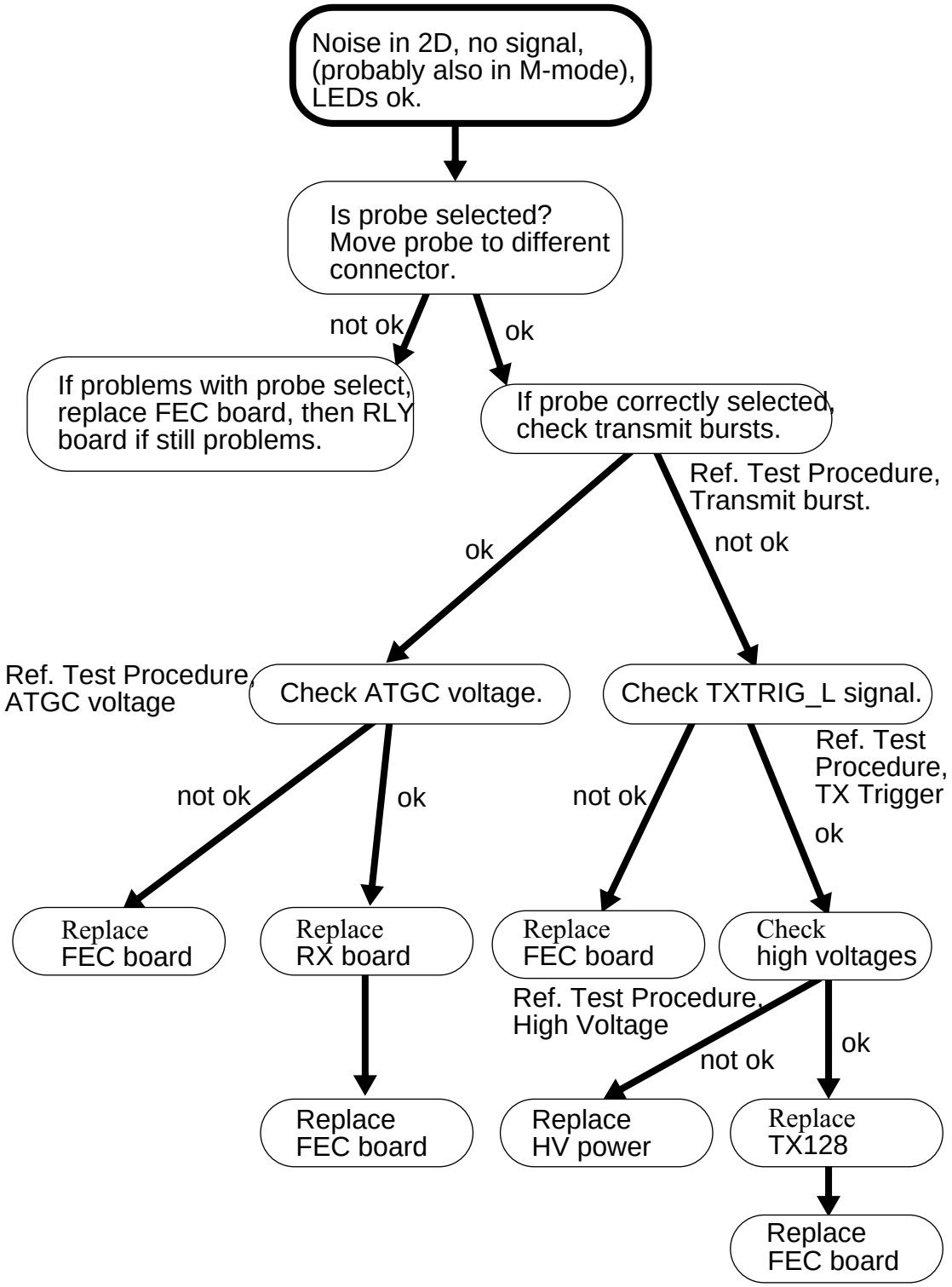
3.4.2 No Display in the Image Field



3.4.3 Data in Image Field Frozen

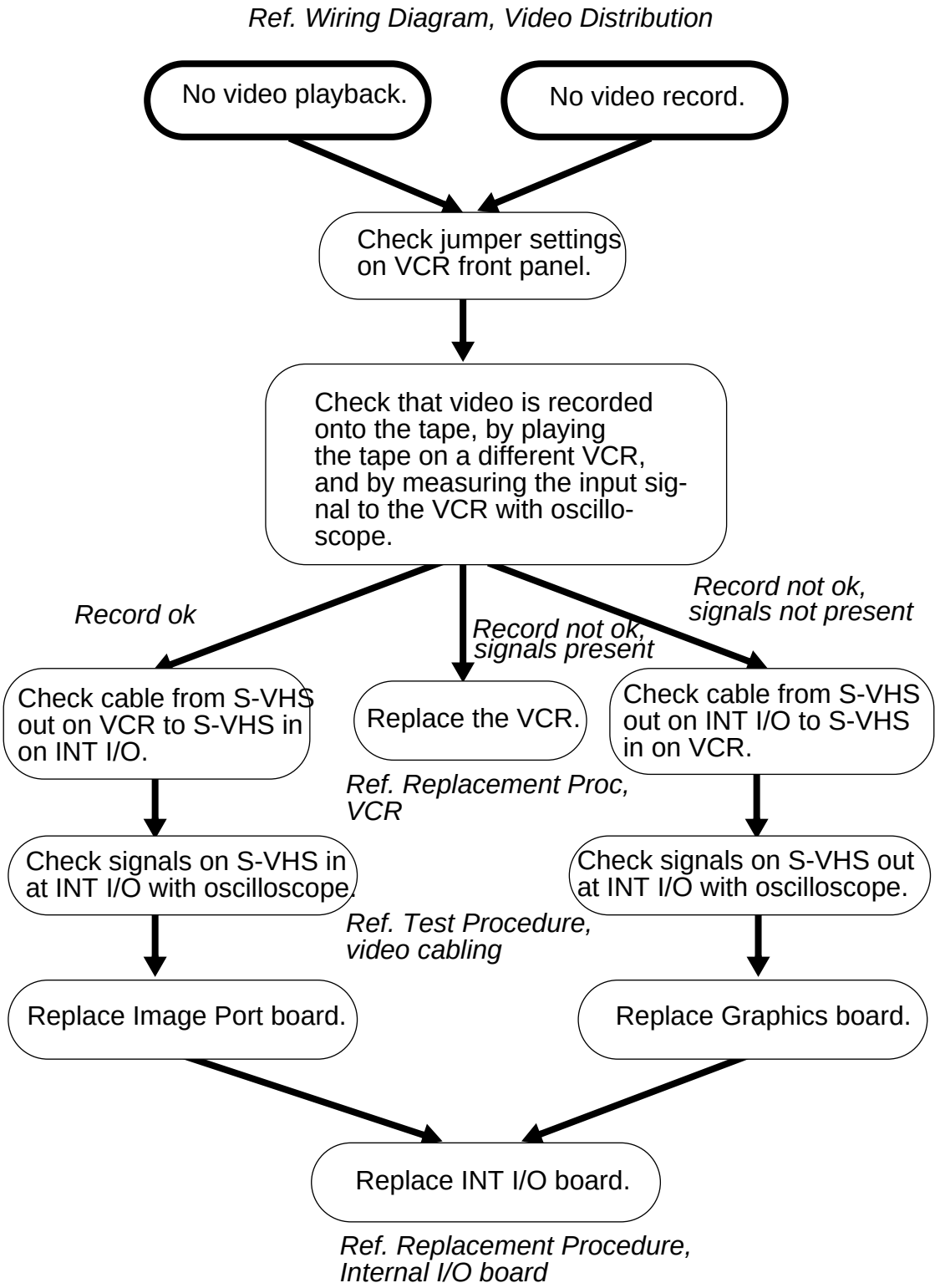


3.4.4 Only Noise in image Field



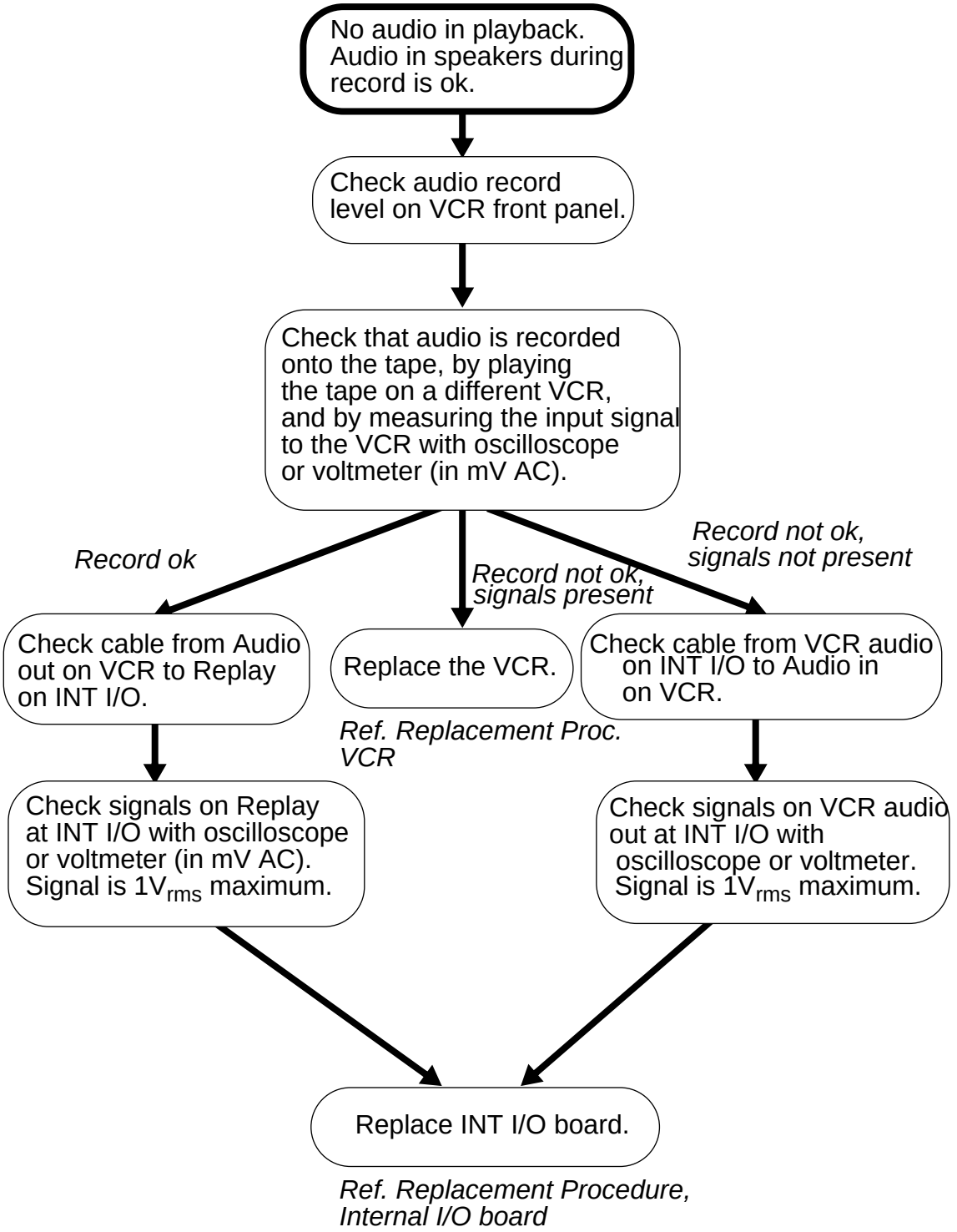
3.5 Peripheral Problems

3.5.1 VCR Related Problems



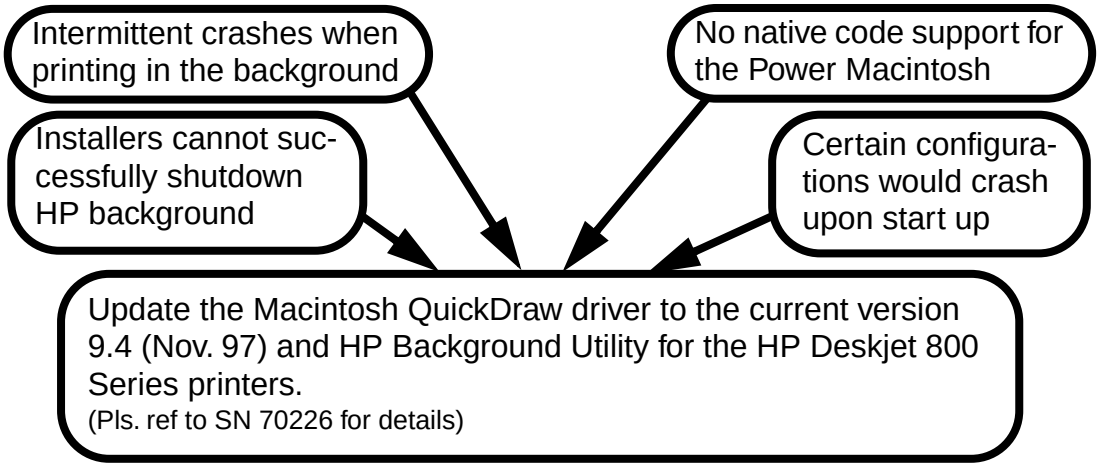
VCR related problems, continued

Ref. Block Diagram, Keyboard, I/O and Peripherals
Ref. Wiring diagram, Internal Cable Harness

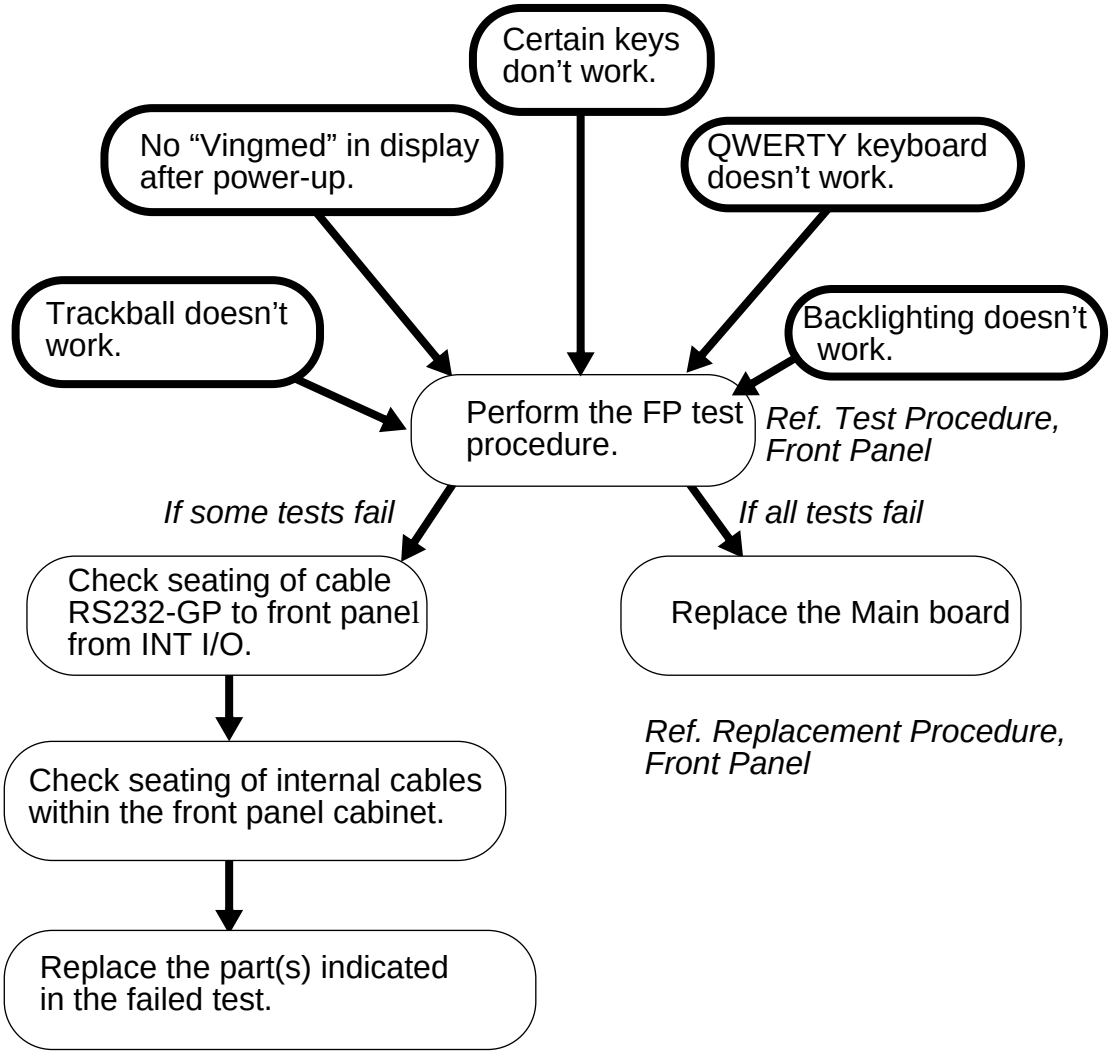


3.5.2 Printer Problems

Attached HP printer to print reports from EchoPAC (ref. SN 70226)



3.6 Front Panel Problems

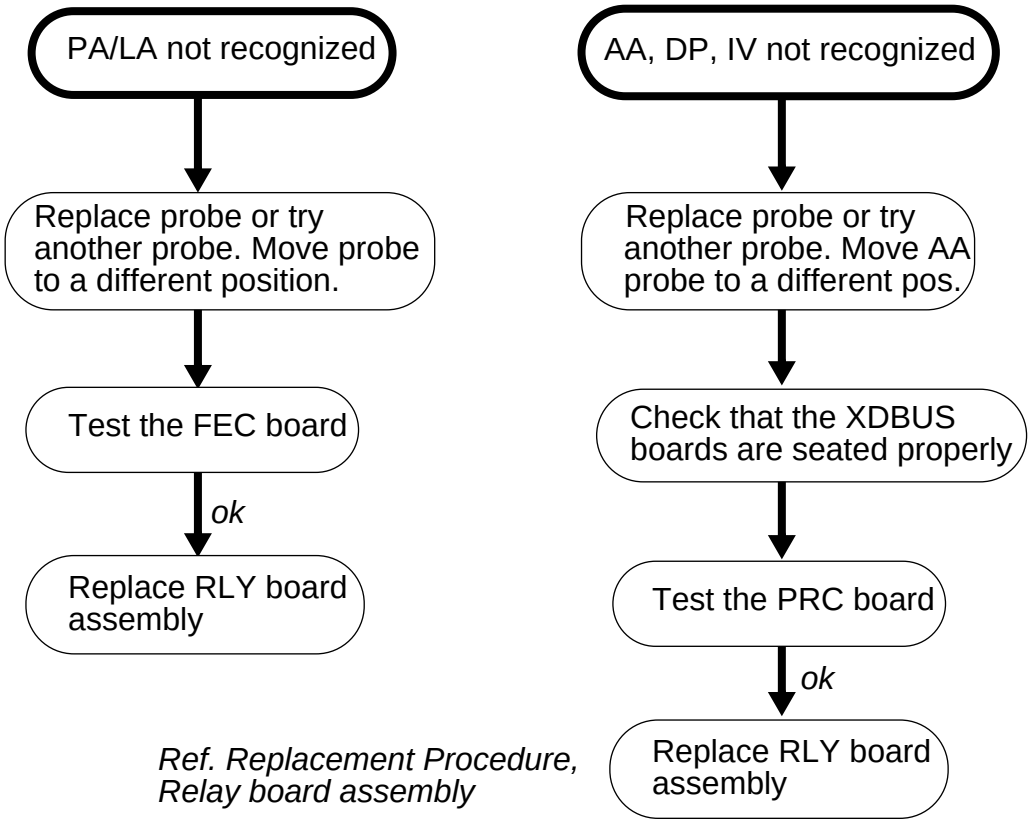


3.6.1 No Response to Front Panel Controls

1. Test the Front Panel.
2. If the Front Panel is ok, and only certain functions doesn't work, test the boards where the actual functions are performed. See Front Panel Controls in the Front Panel section for the coupling between function and board.

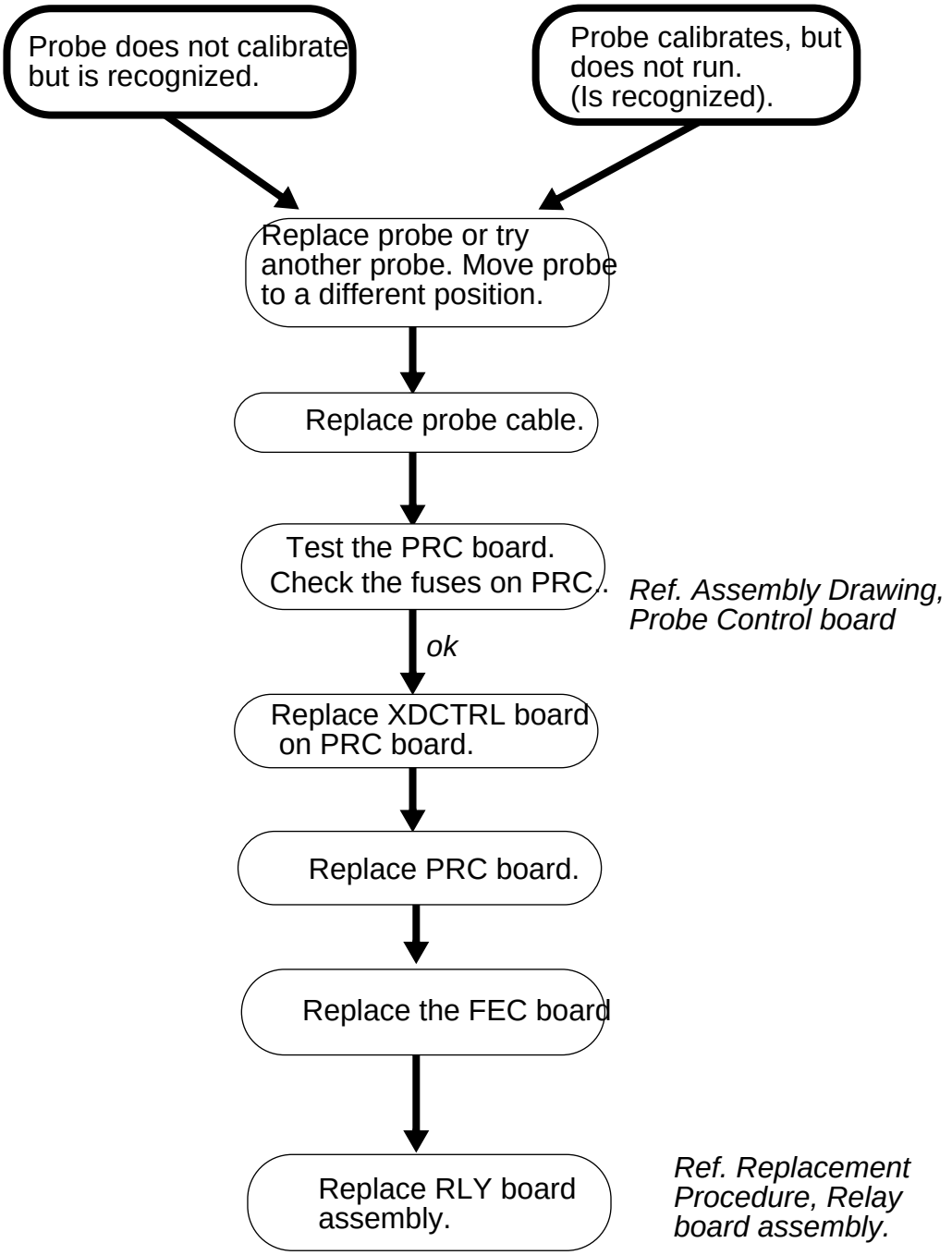
3.7 Probe Problems

3.7.1 Probe Recognition and Switching Problems



Ref. Replacement Procedure, Relay board assembly

3.7.2 AA Probes Do Not Run



3.8 Specific 2D Problems

3.8.1 “Frozen” images, Images with Artifacts

1. Test RFT board
2. Test IMPORT (and IMMEM implicit) boards
3. Test SCONV board
4. Test GRAPH board.
5. Test FEC board (and TX/BF cache)

3.8.2 "Pulsing" or Fading Image

1. The HV supply is marginally designed, and can for some probes and applications fade out at some special settings. See **service memo no. 43** for details. Modifications have been done to the power supply in order to improve the situation, **see service bulletin no. 101**.

3.8.3 Noisy Images (also see Noise Guide Chapter)

The most typical noise problem is coherent noise patterns straight down in the image field. Usually the noise is only picked up when coupling the probe to your body.

1. Disconnect all external cables to the EXT I/O board (if mounted) to establish whether the noise is due to interference from external devices. There are possible ferrite solutions to most of the cable connections, including the ethernet connection.
   - On video cables:
     Wind the cable twice through a split ferrite, GE Vingmed P/N: 038X1012 / 038X1112.
   - On RS232 cables:
     Wind the cable 5-6 times trough a ferrite ring, GE Vingmed P/N: 038X0028.
   - On ethernet: Use the GEVU ethernet noise filter cable, GE Vingmed P/N: FA200460, between the system connector and the AUI box.
2. Try another probe (and cable if APAT).
3. Disconnect all probes that are not in use (keep only the active probe connected).
4. Is the FE Alignment performed?
5. Make sure that the shield for the Patient I/O cable is connected to ground. Otherwise you may have flashes of noise straight down.
6. Check that all noise modifications in the V1.1 and V1.2 upgrades have been done.
7. Other possible internal noise sources:
   - HV Power Supply,
   - DC Power Supply,
   - Peripherals.

3.8.4 Poor Image Quality

1. Check setup of monitor according to setup procedure.
2. Perform the *element test*.
3. There have been problems with the quality of the 3.5 FPA probe (loose lenses) causing poor image, CFM and Doppler quality. Probes with rev. C are improved.
4. Try another probe (and cable if APAT).
5. Disconnect all probes that are not in use (keep only the active probe connected).
6. Test FEC board (and BF cache and TX128 cache and TPGs).
7. Check ATGC voltage (*Ref. Test Procedure, ATGC Voltage*).
8. Test HV Supply (*Ref. Test Procedure, HV Supply*).
9. Test BF boards (digital FE tests).

3.8.5 Only Center Part of FLA/CLA Probes Image Shown

If in 2D with a linear probe only one third of the image is shown and the rest is black,, this could be the problems:

* All multiplexers in the probe connector could be bad (not very likely).

* +/- 80 V from the TX Supply feeding the multiplexers could be missing.

* +15 V from the RLY board to the multiplexers could be missing.

To check the last to points:

*Pull out the probe in connector 1, insert a strap between pin AA10 and AA9 in order to enable the probe present signal. (See I/O section in service manual for location of pins).

* +80V should be present on pin X10.

* -80V should be present on pin Z10.

* +15V should be present on pin V10.

On at least two systems, the problem has been that +15V has been missing. The +15V
out to the probe connector goes through a recovery-fuse. We have seen problems with
a component, SN75352, on the RLY board breaking and loading down the +15V on the connector side of the fuse. The fix is to replace the bad chip (localized because of its heat) or replace the whole RLY board.

3.8.6 "Phantom" Images with CLA Probes

If 'phantom" images are shown e.g. inside the descending aorta on abdominal images with CLA probes, the problem is most likely due to a down rev. version of the FEC board, see. service Memo no. 47. The FEC board shoulds be replaced with a newer version.

3.9 Specific M-Mode Problems

TBD

3.10 Specific Color Flow problems

3.10.1 No Color Flow (2D ok) or Frozen Color Flow

1. Test CFP board.
2. Test RFT board (IQ buffer may fail).
3. Test IMPORT board.
4. Test SCONV board.

3.10.2 Noise Problems (Also see Noise Guide Chapter)

The most typical noise problem is coherent noise patterns straight down in the image field. Usually the noise is only picked up when coupling the probe to your body.

1. Disconnect all external cables to the EXT I/O board (if mounted) to establish whether the noise is due to interference from external devices. There are possible ferrite solutions to most of the cable connections, including the ethernet connection.

   On video cables: Wind the cable twice through a split ferrite, 038X1012/ 038X1112.

   On RS232 cables: Wind the cable 5-6 times trough a ferrite ring, 038X0028.

   On ethernet: Use the GE Vingmed ethernet noise filter cable, p/n FA200460 between the system connector and the AUI box.
2. Try another probe (and cable if APAT).
3. Disconnect all probes that are not in use (keep only the active probe connected).
4. Make sure that the shield for the Patient I/O cable is connected to ground. Otherwise you may have flashes of noise straight down.
5. Check that all noise modifications in the V1.1 upgrade have been done.
6. Other possible internal noise sources: HV Power Supply, DC Power Supply, peripherals.

3.10.3 Poor Flow Quality

1. Try another probe (and cable if APAT)
2. Test FEC board (and BF cache and TX128 cache and TPGs).
3. Check ATGC voltage (*Ref. Test Procedure, ATGC Voltage*).
4. Test HV Supply.

3.11 Specific Color M-Mode Problems

TBD

3.12 Specific Doppler Problems

3.12.1 No Doppler (2D ok)

1. Test SPD board.
2. Test RFT board (LV reject function performed on RFT).
3. Test FEC board.
4. If no CW only (PW ok), check HV Supply (HV2). (*Ref. Test Procedure, High Voltage*).

3.12.2 Noisy Doppler (Also see Noise Guide Chapter)

The most typical noise problem is horizontal lines. Usually the noise is only picked up when coupling the probe to your body.

1. Disconnect all external cables to the EXT I/O board (if mounted) to establish whether the noise is due to interference from external devices. There are possible ferrite solutions to most of the cable connections, including the ethernet connection.

   On video cables: Wind the cable twice through a split ferrite, 038X1012/ 038X1112.

   On RS232 cables: Wind the cable 5-6 times trough a ferrite ring, 038X0028.

   On ethernet: Use the GE Vingmed ethernet noise filter cable, p/n FA200460 between the system connector and the AUI box.
2. Try another probe (and cable if APAT).
3. Disconnect all probes that are not in use (keep only the active probe connected).
4. Make sure that the shield for the Patient I/O cable is connected to ground. Otherwise you may excessive noise lines when the cursor is placed straight down.
5. Check that all noise modifications in the V1.1 upgrade have been done.
6. In order to determine if the noise is coming from the HV Supply, turn power a few dB down. If noise the disappears, the source is the HV Supply. The HV supply is marginally designed, and can for some probes and applications fade out at some special settings. See service memo no. 43 for details. Modifications have been done to the power supply in order to improve the situation, see service bulletin no. 101.
7. Other possible internal noise sources: DC Power Supply, peripherals.
8. Make sure that the TX128 board is rev. B-D or later (+5V analog noise mod.).

3.13 Analog Traces (ECG, Phono, Pressure, Respiration)

Unstable ECG

The quality and stability of the ECG is directly related to the cable being used (impedance is important). For optimum performance the cables with the following VMS part numbers should be used (also see service memo no. 45):

- 164L0036 ECG Cable (gray) for clip-on electrodes.or

- 164L0037 ECG Cable (gray) for clamp electrodes.

NOTE: The blue cable does not have the right impedance for use on System FiVe and will cause unstable ECG.

Flat ECG Trace

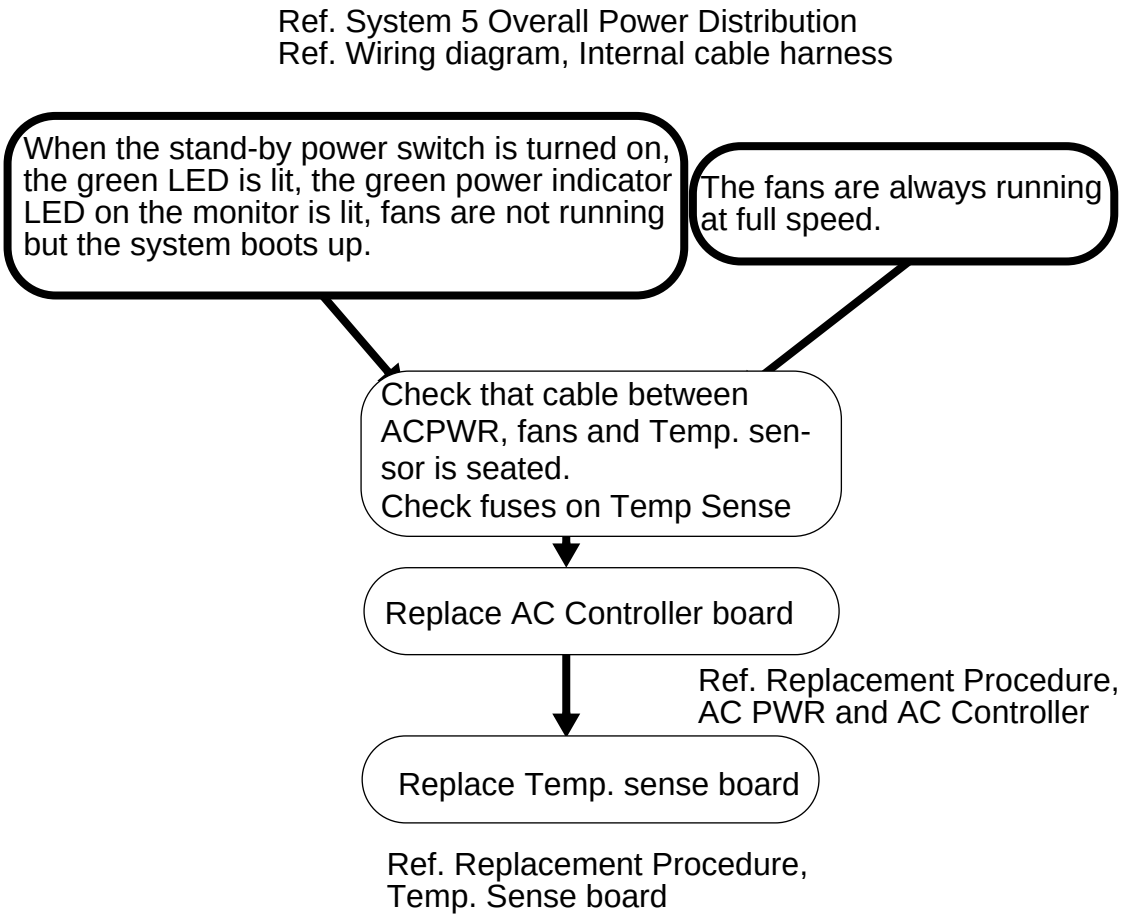
There have been report on intermittant flat ECG. This problem has not yet been reproduced at VMS, so there are no solutions for this. Reboot is the only way out.

For Other Problems:

1. Test the IOP boards (INT I/O, EXT I/O, Patient I/O).
2. Check seating of the Patient I/O cable.
3. Even if the Patient I/O passes the test, it is quite possible that the problem could be on the analog part of the module.

3.14 Misc. Problems

3.14.1 Fan Related Problems



3.14.2 AC Power Heating Problems (System Shut-down)

Some systems have shut themselves off due to overhetaing of the mains transformers inside the ACCTRL box. In order to improve the situation, the thermal fuses in-

side the transformers should be connected in parallel, **see service memo no 44**. Also, fans can be installed below the box, **see service bulletin no. 102**. From November 97, a **new current limiter, FA200558**, replaces the old one, 046M0140. With this solut.ion, the mains current does not go through the thermal fuses inside the transformer. Thus, the temperature on the fuses will not be as high as before. The fuses are used to control a relay inside the new current limiter. The extra fan kit below the AC box is not required with this solution. Neither is parallelling of the thermal fuses.

3.14.3 Power Switch Problems

On the early systems, there were problems with turning the system on. You had to push the power switch several times. The fix is to cut the wire to pin 8 on the AC CTRL cable that goes from the INT I/O board to the AC Power module.

On the first systems we also had problems with the STBY power signal from the power switch to the AC CTRL board being shorted to ground by a screw on the small IV & DP board (the piggyback board on the RLY board). The fix is to just unscrew the top center screw that attaches the IV/DP board to the RLY board.

4 Test- and Setup Procedures

4.1 Front Panel test

4.1.1 Start of Test

- Turn on the system.
- Wait a while until the Front Panel is reset by the system (until VINGMED or SYSTEM FIVE is turned off in the display).
- Push down ALT, SHIFT and 1 after “VINGMED” is displayed. (Release 1 first, then the other two buttons). You should now have the following text in the two displays.:

SW VER.	DATE	OK	CONN

EXIT	TEST	CLEAR	BOOT

- SW VER is the current local front panel software version.

- DATE is the date of software release.

- OK is the status of a serial comm. test. Otherwise ERROR will be displayed.

- CONN

- EXIT test mode.

- TEST enters test mode.

- CLEAR

- BOOT is used during in-house module test of serial communication.

- Enter test mode. You will now have the following text in the lower display:

DONE	DOTS	LEDS	KEYS

4.1.2 Display Test

- Press DOTS: All dots in the display should light up.

4.1.3 LED Test

- Press LEDS: The backlighting LEDs for all keys (except ADD MODE/CURSOR and ACTIVE MODE) should be lit.

4.1.4 Key Test

- Press KEYS (the LED will blink):
- Pressing each of the keys will result in a beep and the hex code for that particular key will be displayed in the upper keyboard.

Macintosh HD:User:James:@i-an:Service:S5_ServiceMan:S5_serv_files:K04_Test-SetupProc: 14.
Printed: December 5, 2000.

4.1.5 Rotary Knob Test

- Turn the rotary knobs. A 4-digit code in the upper display shows up. The first two digits is a code for the 8 rotaries. 00-03 are the knobs between the display. 04 is the ACTIVE MODE knob, 05 is the 2D GAIN knob, 06 is the ZOOM knob and 07 is the DEPTH knob. The last two digits indicates the speed of rotation: low numbers clockwise and high numbers counterclockwise.

4.1.6 Paddle Stick Test

- Move the paddle sticks. Another 4-digit code in the upper display shows up. The two left digits indicate the paddle stick number: 00 is the upper and 01 is the lower. The two right digits indicate the position of the paddle sticks: 00 is up (or left), 01 is center and 02 is down (or right).

4.1.7 TGC Slide pot. Test

- Move the TGC slide pot.'s. A 16 digit code (divided in eight 2-digit sections) in the upper display shows up. The position of the upper slide pot. is displayed in the upper left section of the display code field, and the lower slide pot. is displayed in the lower right code field. Values range from 00 (slide pot. left) to 33 (slide pot. right).

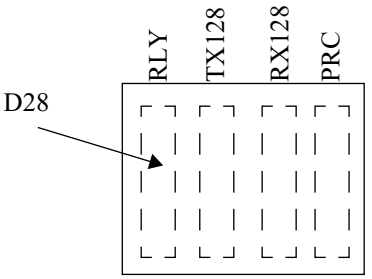
4.1.8 Trackball Test

- Move the trackball up and down, left and right and verify the corresponding position of the arrow on the upper display.

4.2 Transmit Pulse Test

The purpose of this test is to verify that high-voltage transmit pulses are generated on the TX128 board.

- While the system is running in 2D mode, connect oscilloscope ch.A to e.g. pin D28 (channel 65) on the lower XDBUS board (on RLY or TX128 location).



- The signal should be a high-voltage burst. Pulse width, amplitude and frequency will vary with probe type and mode. Amplitude can be controlled with Power.

4.3 Transmit Trigger (TXTRIG) Test

The purpose of this test is to verify that the FEC board generates TTL level transmit trigger pulses.

- Connect scope to coax connector P4 on FEC. (P4 is the lower connector).
- Enter 2D and verify a low TTL pulse of 50 ns width. Prf will vary with system setup.

4.4 ATGC Test

The purpose of this test is to verify that the FEC board generates the correct analog TGC control signals, ATGCVP and ATGCVN.

- Connect a scope to P5 (ATGCV) on FEC. (P5 is the upper connector).
- Enter 2D and verify a voltage ramp signal on the scope, typically ranging from 0V (+10dB) to +8V (+30dB). (The full range is from -10V to +10V).

4.5 High Voltage Test

4.5.1 HV1 and HV2 Tests

On systems with **TX128** boards with artwork rev.D and newer, there are test points for the high voltages located between the two XDBUS boards. **The voltages on the test points are scaled down with a factor of 10.**

Voltage range	TX128 test points
HV1+ (0 to +80V)	4th from top
HV1- (-80 to 0V)	5th from top
HV2+ (0 - to 40V)	3rd from top
HV2- (-40 to 0V)	2nd from top

There are two ways to verify that the voltages are correct:

Alternative 1:

1. Connect your PC to the RS232 port on External I/O as described in 9 "Board Tests via External Terminal/PC" on page K09-1.
2. Write **modSetupDebug=0x2** at the > prompt on the terminal (note the capital letters).
3. Change Power, and the estimated HV1 and HV2 voltages will be printed on the terminal.
4. Verify the voltages on the test points with a voltmeter (remember that the measured values are 1/10’th of the actual values).

Alternative 2:

1. Connect your PC to the RS232 port on External I/O as described in chapter 9 "Board Tests via External Terminal/PC" on page K09-1.
2. Start the test software as described.

3. Enter **Transmitter, HV Supply and PRC** test, then **HV1 test**.

:-) 1

HvTxPrcTest::setHVtestVoltage called with [1,10]

This means that HV1 is programmed to 10V. Verify this with a voltmeter on TP27 (+10V +/- 0.5V) and on TP31 (-10V +/- 0.5V).

:-) 2

HvTxPrcTest::setHVtestVoltage called with [1,0]

HvTxPrcTest::setHVtestVoltage called with [2,1]

:-)

This means that HV1 is set to 0V and HV2 is set to 1V. Verify this with a voltmeter on TP29 (+1V +/- 0.05V) and on TP30 (-1V +/- 0.05V).

4.5.2 Changing the High Voltages

If you wish to select other high voltages, the below command can be used to add or subtract to the original 10 (HV1) or 1 (HV2) voltages.

'+xy.z' or '+x.z' increments HV voltage .

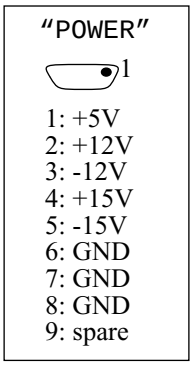
(Eg.: +2.5 will give increase HV1 with 2.5V to 12.5V if test 1 was selected previously).

'-xy.z' or '-x.z' decrements HV voltage

4.6 DC Voltage Test

4.6.1 Measuring DC Voltages on the INT I/O Power Connector(s):

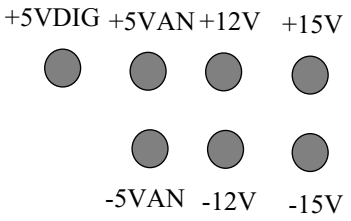
Note that each output is protected with a recovery fuse. Pin 1 is the upper right pin.



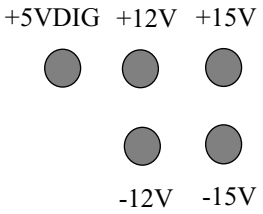
4.6.2 Watching LEDs

1. On the **INT I/O** there are 5 (or 7) LEDs which should be lit when the system is on. If any of the LEDs are off, please measure the voltage(s) as described above before replacing the DC power supply. (The LED could be bad). The only voltage which is not displayed here is +10V.

"New" INT I/O boards:



"Old" INT I/O boards:



All LEDs should have apprx. the same intensity, and they should be stable.

4.6.3 Measuring DC Voltages on the Motherboard.

There are test points for all voltages on the motherboard. By ejecting the IMPORT and GRAPH boards, these test points (not pins, only holes) can be accesses with a voltmeter. They are located in a horizontal row between the P2 and P3 connectors. Starting from the right side, the voltages are:

Nominal Voltage [V]	Voltage Range [V]	Test point label on backplane
+5V DIG	4.75 - 5.25	P5V
+5V AN	4.75 - 5.25	AVCC
-5V AN	-(4.75 - 5.25)	AVEE
+10V	9.5 - 10.5	VDRIVER
+12V	11.4 - 12.6	P12V
-12V	-(11.4 - 12.6)	M12V
+15V	14.25 - 15.75	P15V
-15V	- (14.25 - 15.75)	M15V

4.7 Element Test

In order identify bad elements in probes and bad transmit/receive channels in the system (verifying RLY/TX128/RX and BF), the following test procedure can be used:

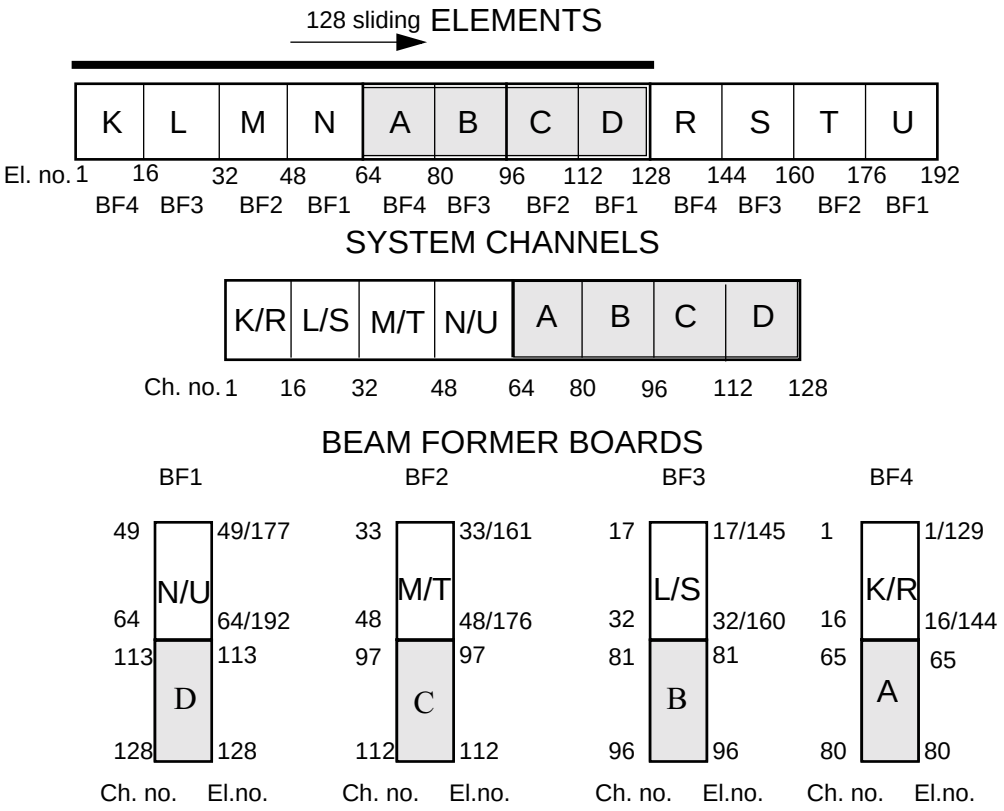
1. Put a little gel on the probe face, and slide the back of a scalpel (or another object with a sharp edge) across the elements, starting from element 1 (the LED side).

2. As the scalpel is moved, watch the intensity of the echo in the 2D image. (At each end, the intensity will gradually drop). Bad elements (or channels) will cause a drop in the intensity. The problem might be the probe or a bad channel on one of the boards mentioned above.
3. In order to distinguish between the probe and the system, try another probe. If you don't have another probe of the same type, you can use a different type together with the channel mapping drawings shown in section 4.8. The map shows the routing from an element to a channel and then to the BF board used. Thus, you should be able to tell if it is the probe, the RLY/TX128/RX boards or the BF boards that are the problem. If one of the BF boards has a failure, you can even determine which of the BF boards are bad.

4.8 Element to Channel Mapping

This section shows the mapping between probe element numbers and system channel numbers for the different types of probes. This information can be used for troubleshooting purposes. The 64 and 96 element probes exist in two channel mapping versions, here called old and new. The purpose of changing to the new type is to be able to run these probes on a 64-channel system.

4.8.1 192 Element Probes



This mapping is true for: 5.0 FLA-192, KN100003 all rev's.

7.5 FLA-192, KT100001 all rev's.

10 FLA-192, KW100001 all rev's.

3.5 CLA-192, KK100004 all rev's.

5.0 CLA-192, KN100008 all rev's.

On a 192 element probe the 64 center elements are always routed to channels 65-128, while the first 64 elements are multiplexed with the last 64 elements onto channels 1-64. Element 1 is multiplexed with element 129, element 2 with 130 and so on.

All channels are used.

All BF boards are used.

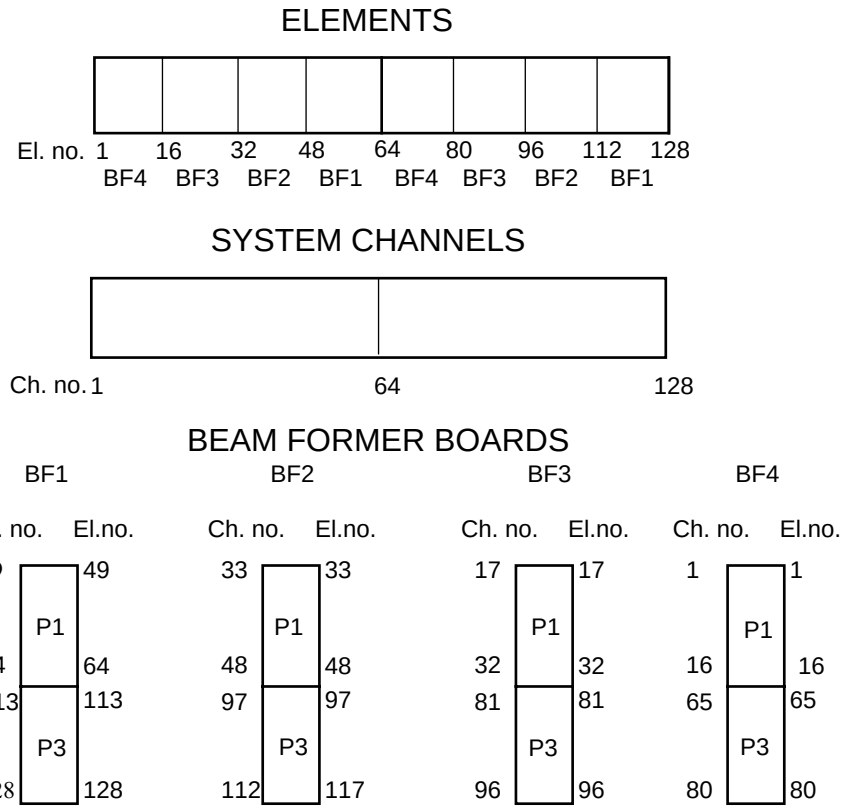
4.8.1.1 Troubleshooting Technique:

One bad probe element (or e.g. one bad coax in the probe cable) will turn up as one point with less intensity in the scalpel test.

One bad channel (RLY/TX/RX, among channels 65-128) will turn up as one point with less intensity in the center part of the probe.

One bad channel (RLY, TX, RX, among channels 1-64) will turn up as two points with less intensity, one point on each side of the center part.

4.8.2 128 Element Probes



This mapping is true for 5.0 FPA-128, KN100001 all revisions.

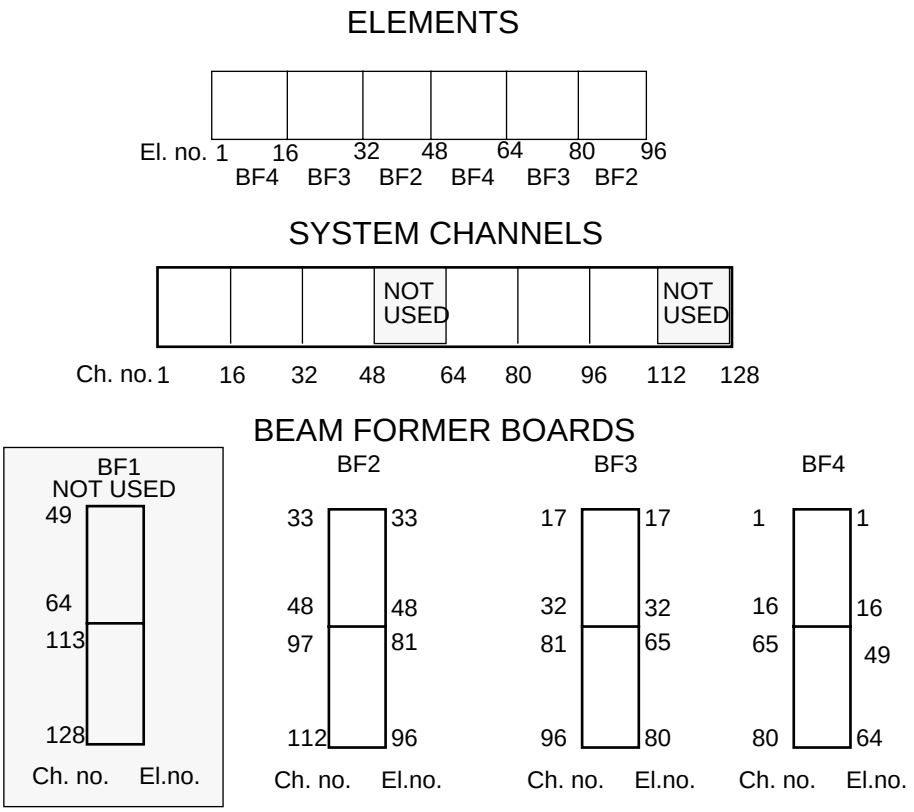
On a 128 element probe there is a one-to-one mapping between element numbers and channel numbers.

All channels are used.

All BF boards are used.

A bad element or a bad channel will turn up at the same spot in the test.

4.8.3 96 Element Probes, Old Mapping



This mapping is true for 3.5 FPA-96, KK100001 rev. A.

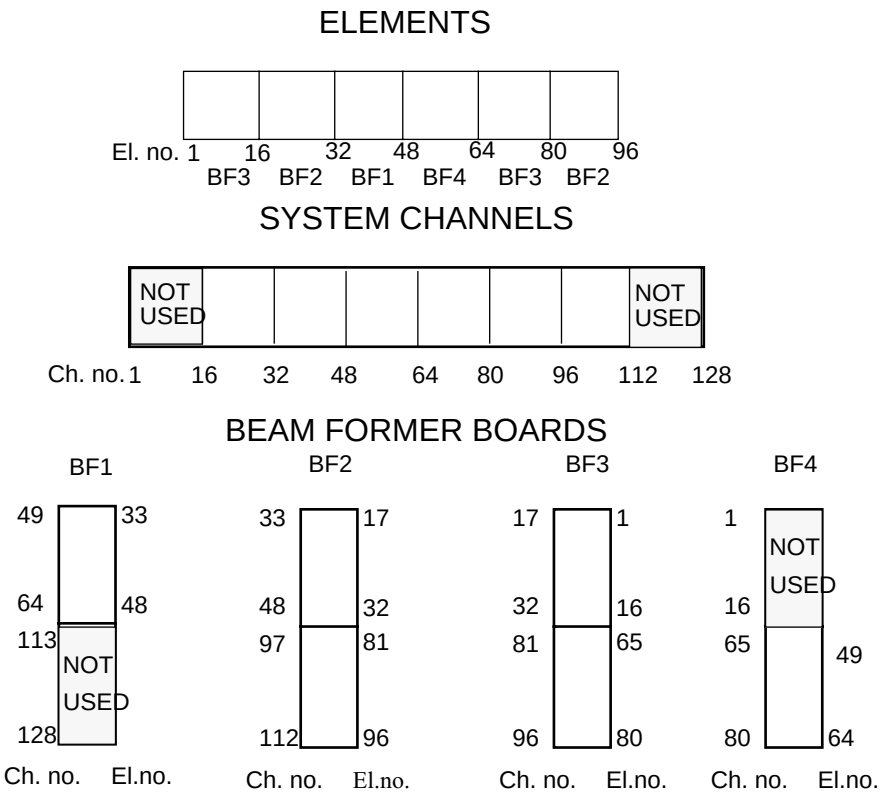
5.0 FPA-96, KN100002 rev. A

On a 96 element probe elements 1-48 are routed to channel 1-48, and elements 49-96 are routed to channels 65-112. By doing this, one BF board (BF1) is not in use.

96 channels are used.

Three BF boards are used: BF2, BF3 and BF4.

4.8.4 96 Element Probes, New Mapping



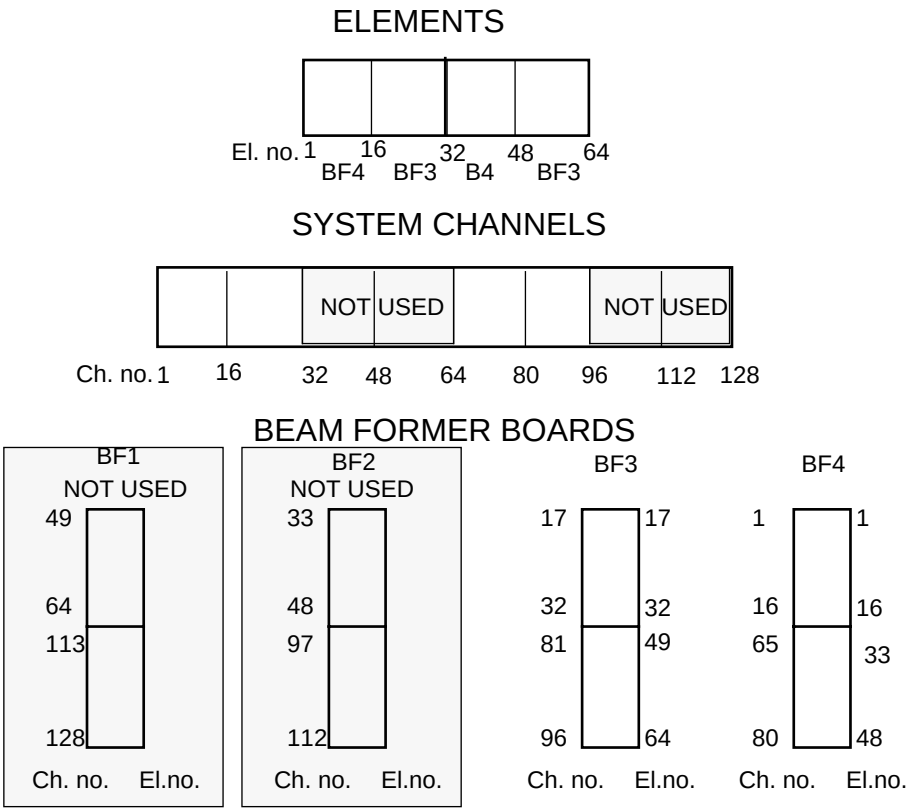
This mapping is true for 3.5 FPA-96, KK100001 rev. B.

3.5 FPA-96, KK100001 rev. C

96 channels are used.

All 4 BF boards are used.

4.8.5 64 Element Probes, Old Mapping



This mapping is true for 2.5 FPA, KG100001 rev.A.

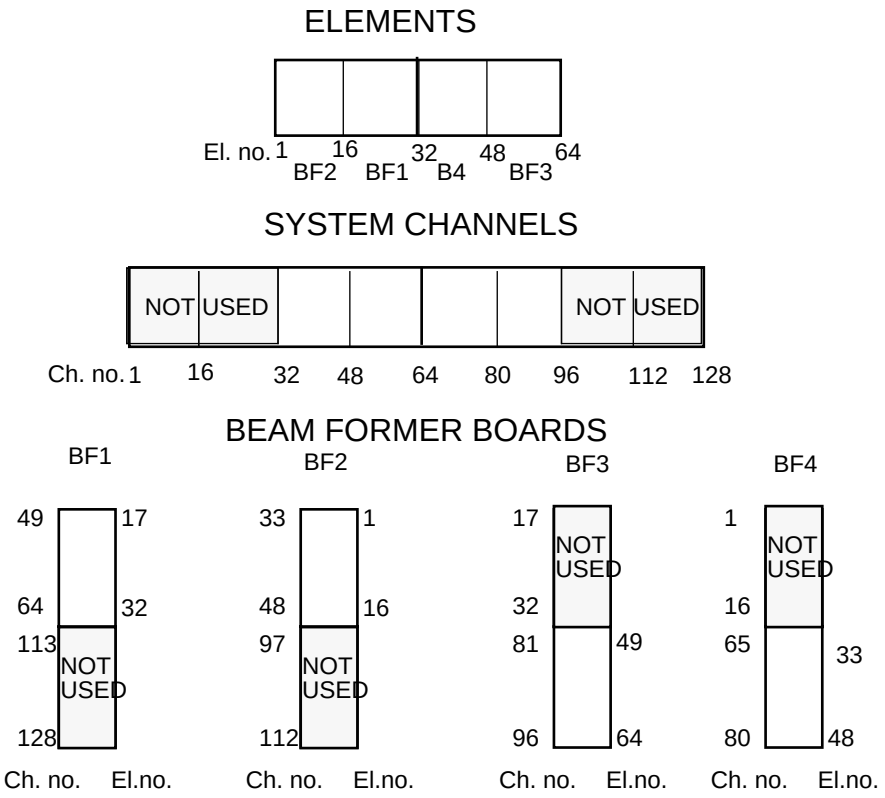
5.0 MPTE, KN100007 rev.A.

On a 64 element probe elements 1-32 are routed to channel 1-32, and elements 33-64 are routed to channels 65-96. By doing this, two BF boards (BF1 and BF2) are not in use.

64 channels are used.

Two BF boards are used: BF3 and BF4.

4.8.6 64 Element Probes, New Mapping



This mapping is true for 2.5 FPA, KG100001 rev.B.

5.0 MPTE, KN100007 rev.B

64 channels are used.

All 4 BF boards are used.

4.8.7 APA Probes

Element 1 (AAXD1) is mapped to 16 receive channels, 4 on each BF board.

Element 2 (AAXD2) is mapped to 16 receive channels, 4 on each BF board.

Element 3 (AAXD3) is mapped to 16 receive channels, 4 on each BF board.

Element 4 (AAXD4) is mapped to 16 receive channels, 4 on each BF board.

[Element 5 (AAXD5) is mapped to 16 receive channels, 4 on each BF board].

4.8.8 Stand Alone Doppler Probes

Element 1 (AAXD6) is mapped to 16 receive channels, 4 on each BF board.

Element 2 (AAXD7) is mapped to 16 receive channels, 4 on each BF board.

5 LEDs

5.1 LEDs, Descriptions

Most of the boards have a red, a green and one or more yellow LEDs.

- When a red LED is lit, it indicates that an error situation has occurred on the board.
- A green LED indicated that the board is ok.
- Yellow LEDs are usually software defined.

Below are the LEDs for each board summarized. The LEDs are listed as viewed from the top of the board when inserted in the rack.

5.1.1 TX128/TX128-2

LED Color	Description	Normally state
Red	Board failure	Normally off
Green	Board ok	Normally on
Yellow	Bus protocol error	Normally off
Yellow	Scan	Normally off
Yellow	Spare	

5.1.2 Probe Controller

LED Color	Description	Normally state
Yellow	AA current overload	Normally off
Yellow	IV current overload	Normally off (not mounted on FA264)
Yellow	TEE temp. ok	On when TEE temperture is ok, else off
Yellow	spare	Not mounted
Yellow	spare	Not mounted
Green	Board ok	Normally on
Yellow	Bus protocol error	Normally off
Red	Board failure	Normally off

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K05_LEDs.14.
Printed: December 5, 2000.

5.1.3 Beam Formers

LED Color	Description	Normally state
Red	Board failure	Normally off
Green	Board ok	Normally on
Yellow	Bus protocol error	Normally off
Yellow	Scan	Normally off
Yellow		

5.1.4 Front End Controller

LED Color	Description	Normally state
Red	Board failure	Normally off
Green	Board ok	Normally on
Yellow	Scan	On when scanning
Yellow	Probe change	On during probe change
Yellow	No-probe	On if no-probe is selected
Yellow	HV overrange	On if excessive HV is output, usually on with V1.1 SW due to HV surveillance
Yellow	VME access	On when communicating with CPU
Yellow	DSP running	Normally blinking (1Hz), "heartbeat"

5.1.5 RF and Tissue Processor

LED Color	Description	Normally state
Red	Board failure	Normally off
Green	Board ok	Normally on
Yellow	DSP runs	Normally blinking
Yellow	Data out on pipelink	On during data transfers to pipelink
Red	Clock problems	Normally off
Red	Clock problems	Normally off
Red	Clock problems	Normally off

5.1.6 Spectrum Doppler Processor

LED Color	Description	Normally state
Upper batch of LEDs:		
Red	DSP1 status	Normally off, on if errors/warnings detected.
Green	ok	Normally on, off if errors detected.
Yellow 0	DSP1 local sw running	Normally flashing
Yellow 1	DSP1 ready for data	On when scanning, else off
Yellow 2	DSP1 has received data	On in Doppler mode, else off
Yellow 3	Data out on pipelink	On during data transfers to pipelink fifo
Yellow 4		On in Doppler mode and audio present.
Lower batch of LEDs:		
Red	Failure	Normally off, on if errors detected.
Green	ok	Normally on, off if errors detected.
Yellow	DSP2 local sw running	Normally flashing
Yellow	audio path ok	On in Doppler and audio present.
Red	Pipelink clock problem	Normally off, on if SDP clock is out of phase with RFT clock. (Note: if system is working and LED is on: System ok.)

5.1.7 2D Flow

LED Color	Description	Normally state
Red	Error	Normally off
Green	ok	Normally on, off if errors detected
Yellow 0	Error	Normally off
Yellow	Error	Normally off
Yellow	Error	Normally off
Yellow	Data processing	On when flow data processed
Yellow	Data processing	Blinking when data arrives
Yellow	VME	Dim light when VME traffic
Green	+5V	Normally on when power on
Green	-5V	Normally on when power on

5.1.8 Image Port

LED Color	Description	Normally state
Yellow	VME master	On during scanning, i.e. data transfers
Yellow	VME slave	
Green	Board ok	Normally on
Red	Board failure	Normally off

5.1.9 Image Port 2

LED Color	Description	Normally state
Red	Lit on CPU selftest failure or reset.	Normally off
Yellow	Lit when CPU is addressing the local bus	
Yellow	Lit when Firmware empties data FIFO to Image Memory.	
Yellow	Lit when IP2 registers/FIFOs are accessed by the local CPU	
Green	Board ok	Normally on
Red	Board failure	Normally off

5.1.10 Graphic uP

LED Color	Description	Normally state
Red	Board failure	Normally off, on during power-up
Green	Board ok	Normally on
Yellow	Local bus active	On during bus activity
Yellow	VME slave	
Yellow	VME master (x-server)	On when graphics updated on screen

5.1.11 Scan Converter

LED Color	Description	Normally state
Green	Board ok	Normally on
Red	Board failure	Normally off, on during power up
Yellow	Bus master	On during scanning, i.e. data transfers

5.1.12 Image Memory

LED Color	Description	Normally state
Green	VME	On during scanning, i.e. data transfers
Green	VSB	Normally off
Green	D64	On during scanning, i.e. data transfers
Green	ALU	On during scanning, i.e. data transfers
Red	ERROR	Normally off

(Some boards only have 3 LEDs, 2 green and one red).

5.1.13 CPU

LED Color	Description	Normally state
Red	Fail	Normally off
Yellow	Stat, status	Normally off
Green	Run	On during booting
Green	Scon	Normally on
Green	LAN	Blinking when running sw from ethernet
Green	+12V	On when +12V for ethernet present
Green	SCSI	Blinking when running sw from hd.
Green	VME	On during VME bus transactions

5.1.14 Internal I/O

LED Color	Description	Normally state
Green	on when ECG	
Green		Normally off
Red	+5V fused	Normally off (error if lit)
Green	DSP ok	Normally blinking (3 Hz)
Yellow	Data processed	Dim light when scanning

5.1.15 LED Overview

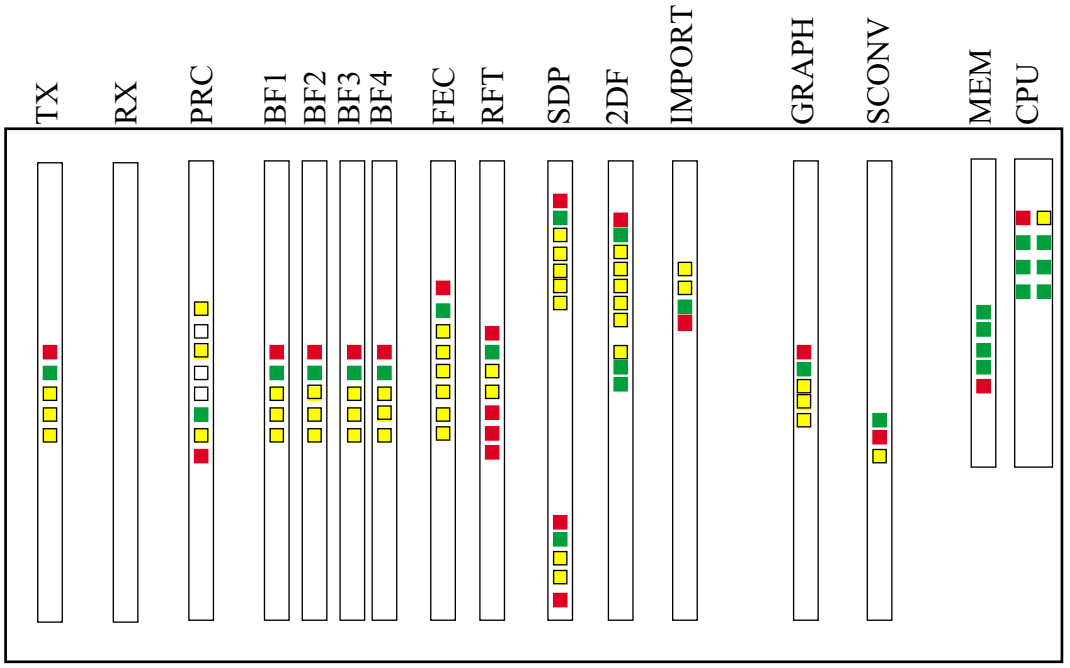


Fig. 5.1 LEDs Overview.
Systems with Image Port / Image Memory on separate boards.

5.1.16 LED Overview

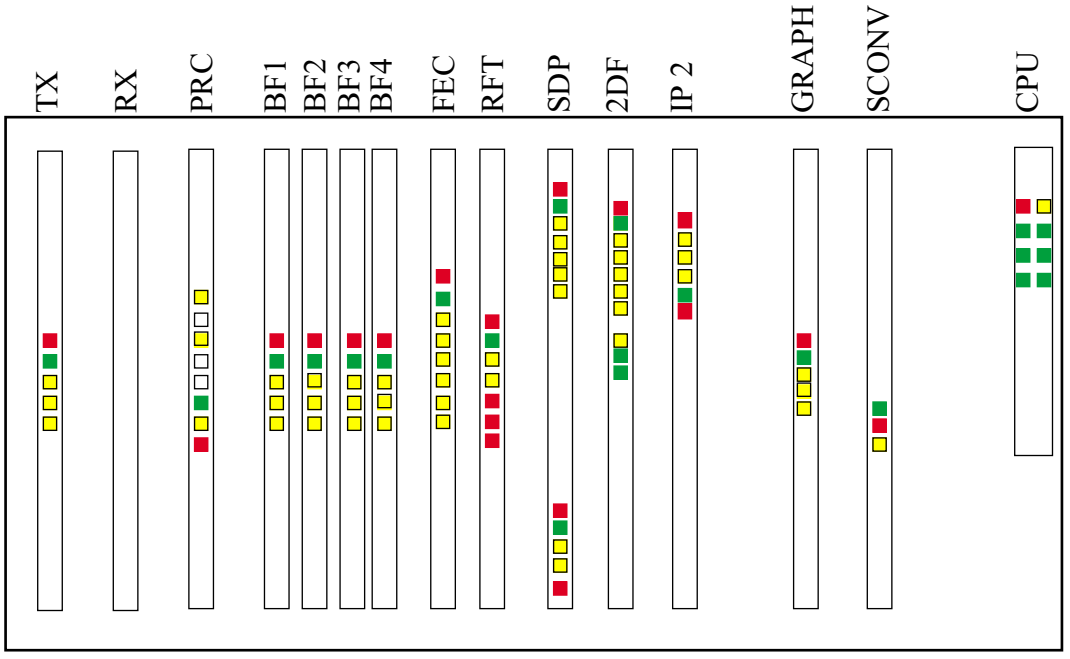


Fig. 5.2 LEDs Overview.
Systems with Image Port 2 board (Mem is included on the IP2 board).

5.2 LED Status During Power-up

5.2.1 TX128/TX128-2

1. Red LED on for 0.5 s, then off.
2. Then the green (ok) LED goes on.

5.2.2 PRC

1. Red LED on for 0.5 s, then off.
2. Then the green (ok) LED goes on.

5.2.3 BF

1. Red LED on for 0.5 s, then off.
2. Then the green (ok) LED goes on.

5.2.4 FEC

1. Red LED (fail) on for 0.5 s, then off.
2. Then the bottom yellow LED start to blink and.
3. the green LED (ok) goes on.

5.2.5 RFT

1. The 3 red LEDs are on for 0.5 s, then off .
2. Then the green (ok) is turned on,
3. and the yellow ”DSP runs” LED is blinking rapidly.

5.2.6 SDP

1. The two red LEDs are on for 0.5 s, then off.
2. Then both green LEDs (DSP1 and DSP2 ok) are turned on and
3. the first yellow LED (# 3 from top) is blinking.

5.2.7 2DF

1. Red LED is on for 0.5 s, then off.
2. Then the upper green LED (ok) goes on.
3. Then all yellow LEDs are lit twice for about 1 s.
4. The bottom yellow LED is on for a few seconds, then goes off.
5. The bottom two green LEDs (+5V and -5V) are on immediately.
6. The fifth yellow (from the top) LED is blinking.

5.2.8 IMPORT

1. The green LED is lit after a while (> 30 s).

5.2.9 IP2

1. The green LED is lit after a while (> 30 s).

5.2.10 GRAPH

1. The red LED is lit for apprx. 25 s.
2. Then the red and green alternate a few seconds, before the red goes off and the green on permanently.
3. The first yellow LED ("local bus active") is intermittently lit.

5.2.11 SCONV

1. The red LED is lit.
2. Then the red goes off and the green on after a while (>30 s).

5.2.12 IMMEM

No LEDs lit.

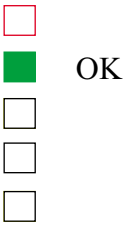
5.2.13 CPU

1. FAIL goes off, Stat off, SCSI off.
2. SCON and +12V goes on.
3. RUN starts to blink when software is loaded from harddisc to internal memory.
4. VME blinks initially during power up.
5. LAN off (but blinks during software loading via ethernet).

5.3 LEDs turned on in 2D

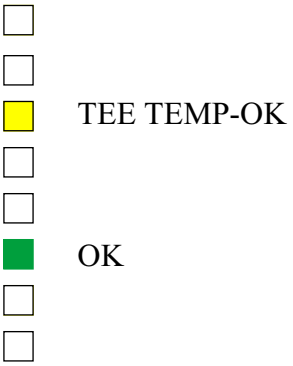
5.3.1 TX128/TX128-2

1. Yellow LED (scan) goes on (not always due to bug).



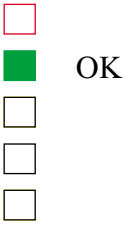
5.3.2 PRC

1. The TEE Temp-ok LED goes on if TE probes are connected and the temperature is ok.



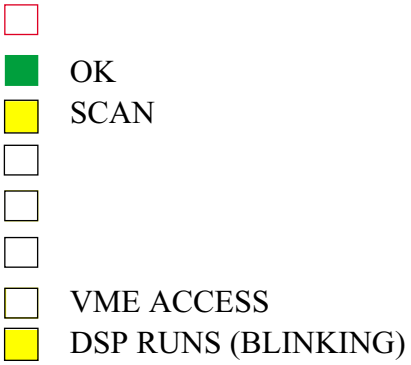
5.3.3 BF1-4

1. Yellow LED (scan) goes on (not always due to bug).



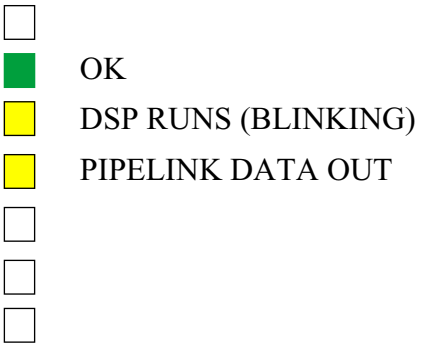
5.3.4 FEC

1. Yellow LED (scan) goes on.



5.3.5 RFT

1. The yellow ("Data out on pipelink") LED goes on.



5.3.6 SDP

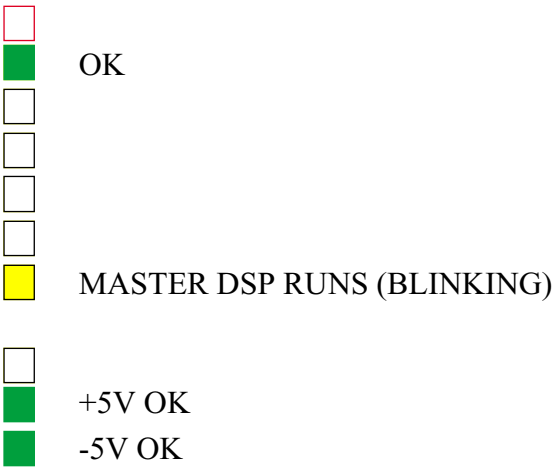
1. The yellow ("DSP1 ready for data") LED goes on

.

5.3.7 2DF

No LEDs go on in addition to the ones already lit.

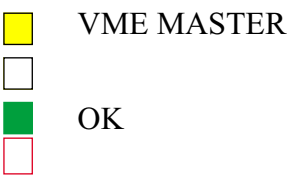
.



5.3.8 IMPORT

1. The upper yellow LED goes on.

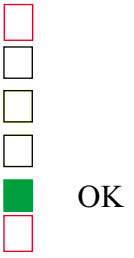
.



5.3.9 IP2

1. The upper yellow LED goes on.

.



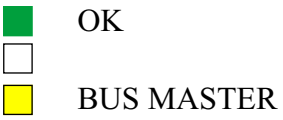
5.3.10 GRAPH

No LEDs go on in addition to the ones already lit.

.SCONV

1. The yellow ("Bus master") LED goes on.

.



5.3.11 IMMEM

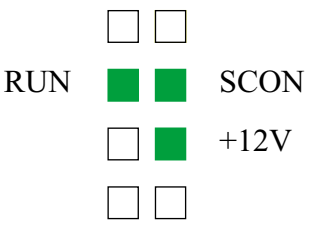
1. Yellow LED (D64) goes on.
2. Green LED (VME) goes on.

.

5.3.12 CPU

1. The RUN LED (green) is brighter.

.

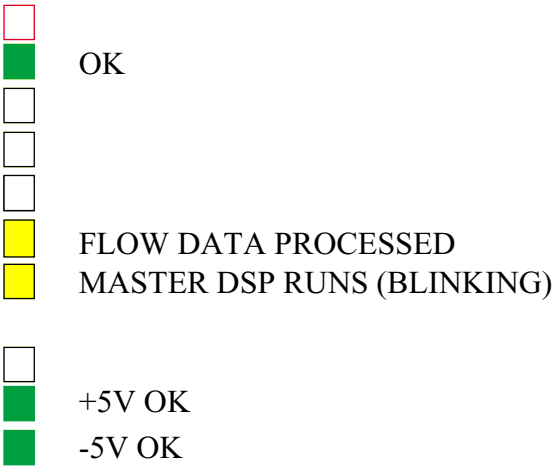


5.4 Additional LEDs Turned on in Color Flow

5.4.1 2DF

1. Yellow LED (flow data processed) goes on.

.

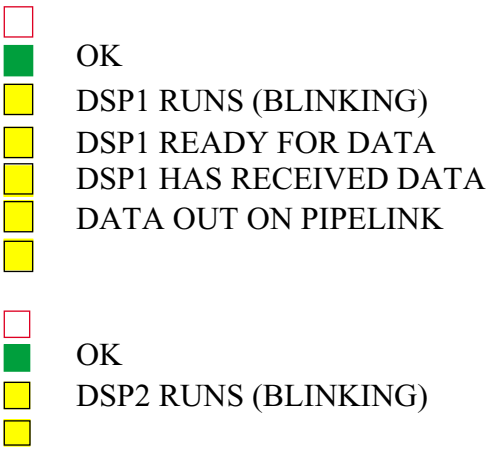


5.5 Additional LEDs Turned on in Doppler

5.5.1 SDP

1. The second, third fourth and fifth yellow LEDs in the upper section all goes on.
2. The first yellow in the lower section blinks, and the bottom yellow goes on.

.



Your Notes:

6 Test Connectors

Some of the boards (FEC, RFT, SDP and 2DF) have pinrows on the edge. On these pins, so-called Debug Piggyback boards can be installed. These Debug boards have 9 pin female D-connectors for RS-232 communication. By conncting a "switched" cable to a terminal or PC with RS-232 interface (baudrate 9600, 1-8-1) to this connector, one can get access to local test software on each of these boards. Note that the Debug board must be connected when the system is powered off.

Depending on where the Debug board is connected, you should get a prompt on the terminal, e.g.

rft>

immediately after the system is powered on.

If you now write "mon" followed by enter, you will enter the local board monitor:

rft> mon (enter)

rftmon>

You can now write "help" followed by enter, or you can directly enter "t m", meaning test monitor, followed by enter.

rftmon>tm (enter)

and the different tests will be displayed.

To start the tests (e.g. test no.1) enter:

rftmon> t 1 (enter)

and this test will be executed.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K06_TestConnectors.12.
Printed: December 5, 2000.

Your Notes:

7 Booting Sequence

By connecting a PC/terminal to the RS-232 CPU connector on the External I/O panel, you can observe the messages the CPU is printing during booting.

Note:
Please be aware that some of the messages written may be different from sw-version to sw-version.

Boot sequences for the following sw versions are included in this service manual:

- V1.7 & V1.7.1 Booting Sequence, see page K07-3
- V1.8.x & V1.9.x Booting Sequence, see page K07-6

7.1 Autoboot Start

The CPU starts autobooting from its boot PROMs.

VxWorks System Boot

Copyright 1984-1993 Wind River Systems, Inc.

CPU: Motorola MVM167

Version: 5.1.1

BSP Version: 1.0

Creation date: Tue May 24 ...

Press any key to stop auto-boot.

3. The programmable address information stored in the boot PROM's is displayed. The information in the Harddisk column is printed out on the terminal. (The Network setup is also listed below).

Description	Harddisk	Network (LAN)
boot device	scsi=0,0	ei
processor number	0	0
host name		xanadu-pcnet
file name	/hd0/vx040.st	/usr/local/netboot/r0/ vx040.st
inet on ethernet (e)	193.69.49.232:ffffff00 or in new systems with GE address: 3.222.21.232:fffffc00	193.69.49.232:ffffff00
inet on backplane (b)		
host inet (h)		193.69.49.111
gateway inet (g)		
user (u)	s5_rack	s5_rack
ftp password (pw)		
flags (f)	0x8	0x8

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K07_BootSequence.15.
Printed: December 5, 2000.

Description	Harddisk	Network (LAN)
target name (tn)	wind8	wind8
startup script (s)	etc/init	etc/init
other (o)	ei	

7.2 V1.7 & V1.7.1 Booting Sequence

```
                VxWorks System Boot

Copyright 1984-1993 Wind River Systems, Inc.


CPU: Motorola MVME167
Version: 5.1.1
BSP version: 1.0
Creation date: Tue May 24 11:24:05 MET DST 1994
Press any key to stop auto-boot...
0
auto-booting...
Waiting for disk to spin up..... done.
Attaching to scsi device... done.

Loading /hd0/vx040.st...655308 + 112484 + 64852
Starting at 0x20000...

Host Name: bootHost
Attaching network interface ei0... done.
Initializing backplane net with anchor at 0x600... done.
Backplane anchor at 0x600... Attaching network interface sm0... done.
Backplane address: 3.222.21.233
Creating proxy network: 3.222.21.233
Attaching network interface lo0... done.
Attaching shared memory objects at 0x600... done

Adding 3447 symbols for standalone.

CPU: Motorola MVME167. Processor #0.
Memory Size: 0x2000000. BSP version 1.0.

Executing startup script etc/init ...
cintStartupScript ("etc/init.c", 0x10000, 0, 0, 101)
value = 0 = 0x0

Done executing startup script etc/init

Executing C startup script etc/init.c...
Mounting "/hd0"... nfs export... done.
Loading "lib/dmem.o"... done.
dmem: Allocated memory pool of 31593372/0 bytes
Starting dynamic memory garbage collector... done.
Today is MON JAN 11 18:17:39 1999
Verifying graph5... data path test... done.
Loading "lib/g5.img" onto graph5... dmem: GCTask waiting ticks to start
done.
```

NOTE

Backplane address indicates whether system is an old system or a new system.
3.222.... series addresses are new systems and
193.69... series addresses are old systems or Network systems.
A different address than these two, indicates a network connection.
Write the down IP-address here :

Boot sequence continues :

```
Loading "usr/lib/X11lfs/fs.o"... dmem: Free memory at 0x01F82578 not allocated tt
dmem: Free memory at 0x01F73124 not allocated by dmem – lost
dmem: Free memory at 0x01FAD780 not allocated by dmem – lost
dmem: Free memory at 0x01F79DE0 not allocated by dmem – lost
dmem: Free memory at 0x01F728A8 not allocated by dmem – lost
dmem: Free memory at 0x01FA4F6C not allocated by dmem – lost
dmem: Free memory at 0x01F71DCC not allocated by dmem – lost
dmem: Free memory at 0x01F71EFC not allocated by dmem – lost
dmem: Free memory at 0x01FA4F58 not allocated by dmem – lost
done.
Awaiting graph5 boot... done.
Awaiting X server start...dmem: Free memory at 0x01F86BC0 not allocated by
dmemtt
..... done.
Awaiting frontpanel start..... done.
Waiting for app to finish loading..... done.
Executing C++ config... done.
Calling static contructors...

All systems go...
dmem: Free memory at 0x01F17040 not allocated by dmem – lostdmem: Free
memory at 0x01F37C58 not allocated by dmem – lost

dmem: Free memory at 0x01F27048 not allocated by dmem – lost

spawning filecache update task...Done
–> Create dispatcher...done
Create Datamodule...
Exception task started....

ImagePort: Hardware present !!!,

Scan converter Functional revision: C software support level 6
tTdpSched id accb34 up and listening ...
tSdpSched id ad0cc4 up and listening ...
done
Create Displaymodule...done
Create Framebuffer...done
Create USParameters...done
Create DisplayParameters...done
Initialize ParameterDictionary...done
initialized supervisor
Connected to front panel
Create VideoOut View...

(6 seconds)filecache entries : 1033
dircache entries : 181
FileCache is up to date...
done
Initialize gaGui...done
Create Users View and slider...SONY VCR detected
Registering ProbeTempSource: pipe(/pipe/probeTemp)
Registering RackTempEventSource: pipe(/pipe/rackTemp)
Registering FootSwitchEventSource: pipe(/pipe/footSwitch)
Registering PowerDownEventSource: pipe(/pipe/powerDown)
Registering HeartRateEventSource: pipe(/pipe/heartRate)
```

Boot sequence continues :

```
Registering ProbeEventSource: pipe(/pipe/probeEvent)
Registering EventSource3D: pipe(/pipe/acq3D)
Registering ScanPlane2EventSource: pipe(/pipe/scanPlane2)

RFT_RPC::loadprogram()...ok.
FEC_RPC::loadprogram()...ok.

SYSTEM FIVE Version: High End
SDP_RPC::loadprogram()...ok.
CFP_RPC::loadprogram()...ok.
IOP_RPC::loadprogram()...ok.
done
Create Remote contrd...done
Create setup dialog...done
Create screen conf dialog...done
Create patient browser...PatientBrowser: readUDTData() failed!
done
Create macXfer...EchoPAC_talk successfully started ! Waiting for EchoPAC to con.
done
Create Clipboard...ClipboardDisplay::ClipboardDisplay: getObject failed. Name r
ClipboardDisplay::ClipboardDisplay: getObject failed. Name = mm ode
ClipboardDisplay::ClipboardDisplay: getObject failed. Name = mm odec
done

Create report generator...Task VMSDiskWriter successfully started. Ready to rec.
done
Create M&A...done
Create Annotation...done
Initialize VCR calibration...done
Initialize VideoScreen...done
started
initialized applications
states created
Entering running mode
Entering scanning mode
Entering users view mode
EchoPAC_talk::establishContact.....Contact established with EchoPAC !
dmem: GCTask started
->
```

7.3 V1.8.x & V1.9.x Booting Sequence

```
                VxWorks System Boot

        Copyright 1984–1993 Wind River Systems, Inc.


        CPU: Motorola MVME167
        Version: 5.1.1
        BSP version: 1.0
        Creation date: Tue May 24 11:24:05 MET DST 1994


        Press any key to stop auto–boot...
        0
        auto–booting...
        Waiting for disk to spin up.......... done.
        Attaching to scsi device... done.

        Loading /hd0/vx040.st...655308 + 112484 + 64852
        Starting at 0x20000...

        Host Name: bootHost
        Attaching network interface ei0... done.

Initializing backplane net with anchor at 0x600... done.
        Backplane anchor at 0x600... Attaching network interface sm0... done.
```

Note:

Backplane address indicates whether system is an old system or a new system. 3.222.... series addresses are new systems and 193.69.... series addresses are old systems or Network systems.

```
        Backplane address: 3.222.21.233
        Creating proxy network: 3.222.21.233
        Attaching network interface lo0... done.

        Attaching shared memory objects at 0x600... done

        Adding 3447 symbols for standalone.

        CPU: Motorola MVME167. Processor #0.
        Memory Size: 0x2000000.BSP version 1.0.

        Executing startup script etc/init ...
        cintStartupScript (”etc/init.c”, 0x10000, 0, 0, 101)
        value = 0 = 0x0

        Done executing startup script etc/init

        Executing C startup script etc/init.c...
        Mounting ”/hd0”... nfs export... done.
        Loading ”lib/dmem.o”... done.
        dmem: Allocated memory pool of 31593372/0 bytes

        Starting dynamic memory garbage collector... done.
        Today is MON JAN 11 18:17:39 1999
        Verifying graph5... data path test... done.
        Loading ”lib/g5.img” onto graph5... dmem: GCTask waiting ticks to start
        done.
        Loading ”usr/lib/X11/fs/fs.o”... dmem: Free memory at 0x01F82578 not
        allocated tt
        dmem: Free memory at 0x01F73124 not allocated by dmem – lost
        dmem: Free memory at 0x01FAD780 not allocated by dmem – lost
        dmem: Free memory at 0x01F79DE0 not allocated by dmem – lost
        dmem: Free memory at 0x01F728A8 not allocated by dmem – lost
```

```
dmem: Free memory at 0x01FA4F6C not allocated by dmem – lost
dmem: Free memory at 0x01F71DCC not allocated by dmem – lost
dmem: Free memory at 0x01F71EFC not allocated by dmem – lost
dmem: Free memory at 0x01FA4F58 not allocated by dmem – lost
done.
Awaiting graph5 boot... done.
Awaiting X server start...dmem: Free memory at 0x01F86BC0 not allocated
by dmemtt
......... done.
Awaiting frontpanel start....... done.
Waiting for app to finish loading......... done.
Executing C++ config... done.
Calling static contructors...

All systems go...
dmem: Free memory at 0x01F17040 not allocated by dmem – lostdmem: Free
memory at 0x01F37C58 not allocated by dmem – lost

dmem: Free memory at 0x01F27048 not allocated by dmem – lost

spawning filecache update task...Done
–> Create dispatcher...done
Create Datamodule...
Exception task started....

ImagePort: Hardware present !!!,

Scan converter Functional revision: C software support level 6
tTdpSched id accb34 up and listening ...
tSdpSched id ad0cc4 up and listening ...
done
Create Displaymodule...done
Create Framebuffer...done
Create USParameters...done
Create DisplayParameters...done
Initialize ParameterDictionary...done
initialized supervisor
Connected to front panel
Create VideoOut View...

(6 seconds)filecache entries : 1033
dircache entries : 181
FileCache is up to date...
done
Initialize gaGui...done
Create Users View and slider...SONY VCR detected

Registering ProbeTempSource: pipe(/pipe/probeTemp)
Registering RackTempEventSource: pipe(/pipe/rackTemp)
Registering FootSwitchEventSource: pipe(/pipe/footSwitch)
Registering PowerDownEventSource: pipe(/pipe/powerDown)
Registering HeartRateEventSource: pipe(/pipe/heartRate)
Registering ProbeEventSource: pipe(/pipe/probeEvent)
Registering EventSource3D: pipe(/pipe/acq3D)
Registering ScanPlane2EventSource: pipe(/pipe/scanPlane2)

RFT_RPC::loadprogram()...ok.
FEC_RPC::loadprogram()...ok.

SYSTEM FIVE Version: High End
SDP_RPC::loadprogram()...ok.
CFP_RPC::loadprogram()...ok.
IOP_RPC::loadprogram()...ok.
done
Create Remote control...done
Create setup dialog...done
Create screen conf dialog...done
Create patient browser...PatientBrowser : readUDTData() failed!
done
Create macXfer...EchoPAC_talk successfully started ! Waiting for EchoPAC
to con.
done
```

```
Create Clipboard...ClipboardDisplay::ClipboardDisplay : getObject
failed. Name r
ClipboardDisplay::ClipboardDisplay : getObject failed. Name = mmode
ClipboardDisplay::ClipboardDisplay : getObject failed. Name = mmodec
done

Create report generator...Task VMSDiskWriter successfully started. Ready
to rec.
done
Create M&A...done
Create Annotation...done
Initialize VCR calibration...done
Initialize VideoScreen...done
started
initialized applications
states created
Entering running mode
Entering scanning mode
Entering users view mode
EchoPAC_talk::establishContact.....Contact established with EchoPAC !
dmem: GCTask started
–>
```

8 Introduction to Test Software Guide

8.1 Abstract

This is a document describing how to use the System 5 Test Software. The first version of the document (and the system software) only supports board tests via an external terminal/PC.

8.2 Overview

Chapter 9 "Board Tests via External Terminal/PC" on page K09-1 is a description of how to use the Board Test Software.

Chapter 17 "Power-up Test" on page K10-1 describes what power-up tests that are performed.

Chapter 18 "Performance Test (System Test) Procedure" on page K11-1 describes how to use the test software which will be accessed via the Setup button on the keyboard.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K08_TestSW_intro.12.
Printed: December 5, 2000.

Your Notes:

9 Board Tests via External Terminal/PC

9.1 Parts Requirements

- Terminal or PC with a terminal emulator program. The terminal must have the following configuration:
  - Baudrate: 9600
  - Stopbit: 1
  - Parity: None
- "Crossed" RS-232 cable (rx and tx swapped, i.e. pins 2 and 3 swapped). The cable must have a 9 pin female D-connector on the System 5 side, and whatever connector that is appropriate on the terminal/PC side.
- If Hyperterminal is used,

9.2 Interconnections

- Connect the cable between terminal/PC COM connector and RS-232 CPU connector on External I/O on System 5.

9.3 System Requirements

A probe (preferably an FPA probe) must be installed in connector 1.

9.4 VxWorks Operating System Commands

In order to move between directories and view what's on them, the following commands can be used (usr is a directory used as an example):

- **pwd** : print working directory — hd0 is the highest working directory.
- **cd "usr"** — change directory to usr — from hd0 working directory.
- **cd "/usr"** — change directory to usr — from any directory.
- **cd ".."** — change to previous dir. — from working directory.
- **ls** — list files/directories — on working directory.
- ll — list files/directories — on working directory (long).
- **copy "file1" , "file1.bac"** — e.g. copy file1 to file1.bac

9.5 Start-up of Board Test Program

- Turn the system on.
- Depending on if the system boots or not, follow the instructions below (the instructions are made for systems with harddisk, SW V1.2).

9.5.1 If the GRAPH Board Doesn't Boot

In cases where the GRAPH board doesn't boot (no start-up screen) , the test software will be automatically started and the menu shown in 9.6 "The Board Test Menu" on page K09-2 will be shown on the terminal.

Macintosh
HD:User:James:@:arb:Service:S5_Service\Man:S5_serv_files:K09_BoardTests:12:

9.5.2 If you wish to start the test software instead of normal booting

There are two ways to do this:

9.5.2.1 Hold down the t key (preferred way)

Hold down the character **t** on the System-5 keyboard while the system is booting. You must hold the t down for apprx. 40 seconds (until VINGMED SOUND/SYSTEM FIVE is turned off in the keyboard display). You will then automatically start the test software. The menu shown in 9.6 "The Board Test Menu" on page K09-2 will be shown on the terminal.

9.5.2.2 Hold down the Shift key

Hold down the Shift key on the System FiVe keyboard while the system is booting. You must hold the key down for apprx. 40 seconds (until GE Vingmed Ultrasound/ System FiVe is turned off in the keyboard display).

At the prompt >, enter **<usr/app/test/bin/brdtm** on the terminal. It is very important that the character **<** is used and **not >** .This command will start the script (batch file) *brdtm* which loads the test software from the harddisk.

9.5.3 If you wish to start the test software after normal booting

1. After the system has finished booting, press freeze.
2. Enter **<usr/app/test/bin/brdtm** on the terminal. It is very important that the character **<** is used and **not >** .This command will start the script (batch file) *brdtm* which loads the test software from the harddisk.

   NOTE: In V1.5 and V1.5.1 this method can NOT be used; the brdtm file is missing on the disk.
3. The board test menu should now be shown on the terminal.

9.6 The Board Test Menu

A help menu can be accessed by entering 'h'. This help menu describes how to start and stop the tests for the different boards. The test menu is typically looking like this:

***** Board Test Monitors (c) Vingmed Sound A/S v.1.2 1997 *****

M E N U

0:	*Transmitter, Tx Supply and PRC tests*	
1:	*Front End Boards*	
2:	*Radio Frequency and Tissue Processor Board*	*(RFT)*
3:	*Spectral Doppler Processor Board*	*(SDP)*
4:	*Color Flow Processor Board*	*(CFP)*
5:	*In/Out Processor Board*	*(IOP)*
6:	*Image Port Board*	*(IMPORT)*

7: Scan Converter Board (SCONV)

8: Graphic Processor Board (GRAPH)

'hw' : Get Hw versions

'sw' : Get Sw versions

probe : Get Probe Information

'loop' : Toggle LOOP-flag On/Off

'mon' : Toggle MON-flag: Enter test monitors when MON is ON

'?' : Get help text

'm' : Get this menu

'x'/'q': (EXIT) Terminate testing and leave Board Test Menu

The first step in order to start a board test, is to press the number, followed by enter.

NOTE that you get no feedback (keystroke printout) from the terminal when pressing characters on your keyboard.

9.7 Help Menu

When inside the local testmenus, the information in the help menu is useful.

Board test program, v.1.3 (c) 1997 Vingmed Sound A/S

Test menu options for FEC, RFT, SDP, CFP and IOP:

An automatic self test is run when you enter the test number.

"m " to get the current main menu

"mon" toggles the MON flag ON/OFF

When the MON-flag is ON, You will enter the local test monitor.

A few commands when INSIDE a test monitor:

"tm " to get menu when inside test monitor

"t #" to run board test number #

"t 1" to run a complete board test

"help" to get help menu for the local monitor

"q" to leave the board test monitor menu

"?" to get the help text

Enter <CR> to get next page.

Test menu options for IMPORT and GRAPH:

"?" to get a menu displayed

"r" to run board test

"q" to leave the test program

Special for GRAPH:

"x" to run external G5 tests

"p" to get the G5 test results

Enter <CR> to return to the menu:

9.7.1 Transmitter, HV Supply and PRC test

**** HV, TX and PRC Tests ****

M E N U

1: HV 1 test
2: HV 2 test
3: PW test 1 on TX board
4: PW test 2 on TX board
5: Test CW lower on TX board
6: Test CW upper on TX board
7: PRC setup for test
8: Enter PRC test monitor
9: Run automatic PRC test
10: Test ADC input noise

'+xy.z' or '+x.z' increments HV voltage
'-xy.z' or '-x.z' decrements HV voltage
'm' : Get this menu
'q' : Return to BTM menu

9.7.1.1 HV1 and HV2 tests

There are test points on the TX128 board (only artwork D and onwards). These test points are **scaled down with a factor of 10**.

Voltage range	PRC test points	TX128 test points
HV1+ (0 to +80V)	TP27 (3rd from top)	4th from top
HV1- (-80 to 0V)	TP31 (4th from top)	5th from top
HV2+ (0 - to 40V)	TP29 (2nd from top)	3rd from top
HV2- (-40 to 0V)	TP30 (top)	2nd from top

:-) 1

HvTxPrcTest::setHVtestVoltage called with [1,10]

This means that HV1 is programmed to 10V.

:-) 2

HvTxPrcTest::setHVtestVoltage called with [1,0]

HvTxPrcTest::setHVtestVoltage called with [2,1]

:-)

This means that HV1 is set to 0V and HV2 is set to 1V.

9.7.1.2 Changing the high voltages

'+xy.z' or '+x.z' increments HV voltage .

(Eg. +2.5 will give increase HV1 with 2.5V (from whatever it was before)).

'-xy.z' or '-x.z' decrements HV voltage

9.7.1.3 PW, CW and PRC tests

For factory test only, requires special hardware.

9.7.1.4 Test of ADC input noise

This test is for the RX128 board and the analog part of the BF boards (before A/D-conversion).

The noise level for each channel ismeasured. The ATGC level is set to maximum, and the noise level is digitally read from the IQ memory on the RFT board. .

10

Opened usr/app/test/etc/wkaiser.mat

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

FrontEndCtrl_C::enableNoProbeScan: enable = 1

Reading IQ-buffer.....ok)

Sample RMS [1] =0.853985

Sample RMS [2] =0.853046

Sample RMS [3] =0.837349

Sample RMS [4] =0.862293

etc.

9.7.2 Front End Boards

The boards in the Front End are tested in the Front End Test submenu.

**** *Front End Tests* ****

M E N U

1: FEC Hw and Interface tests

2: Probe Controller Board

4: Digital Tests

5: Analog Tests

6: DC-Offset Calibration

'loop' : Loop On/Off

'mon' : Toggle MON-flag

(To enable the test monitor for each board, enter mon. When then pressing the desired test number, you will enter the test monitor and not the automatic test).

'mla' : Toggle MLA number

'?' : Get help text

'm' : Get this menu

'q' : Return to BTM menu

:-)

9.7.2.1 A sequence of FEC, TX and BF tests

This is a self test of the FEC board and the TX and BF cache interfaces.

:-> 10

10

FEC and TX/BF Interface test automatic test .... PASSED

9.7.2.2 FEC Hw tests

This is a test of the FEC board only.

:-) 11

FEC automatic test ..... PASSED

9.7.2.3 TX tests

:-) 11

11

TX Cache and TPG tests ..... PASSED

9.7.2.4 BF Cache tests

:-) 13

BF Cache test ..... PASSED

9.7.2.5 PRC board

:-> 2

***** PRC Tests *****

20: Automatic self test

21: AA power test

22: AA temperature sensor test

23: PA temperature sensor test

24: Temperature threshold test

25: Probe sensor test

26: AA TPG test

20

****** Automatic test of the PRC board ******

Initializing the board

Testing Front End Interface:..passed (8) <08 hex>

Testing AA Temp. sensor

AA low temp test:.....passed (36.3) <36.0-36.8>

AA medium temp test (low ref):.passed (42.1) <41.9-42.7>
AA medium temp test (h. ref):..passed (42.1) <41.9-42.7>
AA high temp test:.....passed (45.3) <44.9-45.7>

Testing PA Temp. sensor
PA low temp test:..... passed (37.5) <37.0-37.8>
PA medium temp test (low ref): passed (42.7) <42.1-42.9>
PA medium temp test (high ref):passed (42.7) <42.1-42.9>
PA high temp test:..... passed (44.4) <43.9-44.7>

Testing Temperature Thresholds
PA 43.0 threshold:.....passed (3.89) <3.85-3.93>
PA 41.3 threshold:.....passed (3.69) <3.64-3.72>
AA 43.0 threshold:.....passed (3.79) <3.74-3.82>
AA 41.3 threshold:..... passed (3.57) <3.53-3.61>

Testing probe sensor
Current range 0:..... passed (4) <02-04 hex>
Current range 1:..... passed (18) <16-1b hex>
Current range 2:..... passed (a2) <90-af hex>
Current range 3:..... passed (ff) <ef-ff hex>

Testing AA Power Amplifier
Power amp. voltage test:.....passed (2.60) <1.93-3.08>
Power amp. current test:.....passed (0.47) <0.40-0.60>
Current overload test:.....passed

Testing AA Transmitter
TPG readback test:..... passed (8) <08 hex>

***** Automatic test.....passed *****

Manual transmitter test (not for field)
Put scope on AA_XD channels 1 - 6 and verify

transmit pulses according to test procedure

******PRC automatic test ..... PASSED*

:->

9.7.2.6 Digital Tests

:-) 3

***** Digital BF Tests *****

30: Digital test 1 : One beam/all channels (BF x-4)

31: Digital test 2 : All beams/one channel

32: Digital test 3 : 32 shots/one channel (BF output to file)

33: Digital test 4 : single channel (BF output to file)

34: Digital test 1 for MLA 0-1 (if more than one MLA)

35: Digital test 2 for MLA 0-1 (if more than one MLA)

All these digital tests are injected in the Focusor ASICs on the BF boards. They test the Focusors and Beamadders. The test result is read from the IQ buffer on the RFT board. Tests.

:->

***** Digital BF Tests *****

30: Digital test 1 : 1 shot/all channels (BF 1-4)

:-) 30

Digital test 1

Opened usr/app/test/etc/digtest1x.mat

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

FrontEndCtrl_C::enableNoProbeScan: enable = 1

Reading IQ-buffer.(ok)

Digital test 1 (MLA 0) ..... PASSED

A digital test pattern is injected into all channels (one MLA only, selected by toggling mla) and the result is summed and compared to a master value. If a channel is bad, the test will fail, but you won't know which channel.

31: Digital test 2 : 128 shots/one channel

Digital test patterns are injected into each channel (one MLA only, selected by toggling mla) and the result for each channel is compared to a master value. If channels are bad, the channel number and BF board will be listed. See example below:

Digital test 2

Digital test 2

Opened usr/app/test/etc/digtest2x.mat

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Reading IQ-buffer.....(ok)

Digital test 2 (MLA 0) ..... PASSED

32: Digital test 3 : 32 shots/one channel (BF output to file)

Digital test patterns are injected into each channel (one MLA only, selected by toggling mla) **on BF4** and the result for each channel is compared to a master value.

:-) 32

Digital test 3

Opened usr/app/test/etc/digtest2x.mat

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Reading IQ-buffer.....(ok)

Digital test 3 (MLA 0) ..... PASSED

33: Digital test 4 : single channel test

Digital test pattern is injected into a channel (one MLA only, selected by toggling mla) which can be selected and the result is compared to a master value.

:-) 33

Digital test 4

Channel number [1-128] : 23

Opened usr/app/test/etc/digtest2x.mat

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Reading IQ-buffer.(ok)

Digital test on channel 23: (MLA 0) ..... PASSED

34: Digital test 1 for MLA 0-1 (if more than one MLA)

A digital test pattern are injected into all channels (both MLAs) and the result is summed and compared to a master value.

Digital test 5

Opened /hd0/usr/app/test/etc/digtest1x.mat

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test0.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test0.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

FrontEndCtrl_C::enableNoProbeScan: enable = 1

Reading IQ-buffer.(ok)

Digital test 1 (MLA 0) ..... PASSED

Opened /hd0/usr/app/test/etc/digtest1x.mat

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test0.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test0.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Reading IQ-buffer.(ok)

Digital test 1 (MLA 1) ..... PASSED

35: Digital test 2 both for MLA 0 and MLA 1

Digital test patterns are injected into each channel (both MLAs) and the result for each channel is compared to a master value.

:-) 35

Digital test 6

Opened /hd0/usr/app/test/etc/digtest2x.mat

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test1.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test1.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Reading IQ-buffer.....(ok)

Digital test 2 (MLA 0) ..... PASSED

Opened /hd0/usr/app/test/etc/digtest2x.mat

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test1.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/test/etc/dig_test1.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Reading IQ-buffer.....(ok)

Digital test 2 (MLA1) ..... PASSED

9.7.2.7 Analog Tests

40: Analog test 1 : All beams/one channel

41: Analog test 2 : 32 beams/one channel (BF output to file)

42: Analog test 3 : single channel (BF out and EPS to file)

43: Noise test : One BF-board (timing errors test)

44: ADC bit test : One BF-board (bit-error test)

45: ADC input noise: All BFs (noise on input to ADCs)

These tests (except 45) require special probe terminator boxes, currently not available. Test 45 is the same as test 0.10.

9.7.2.8 DC offset calibration

This is not a test, but rather a mechanism to read the DC offset from the different A/D converters on the BF boards, so that it can be compensated for later. Also see 23 "FE "Calibration" Procedure" on page K16-1.

**** DC-Offset Calibration ****

60: DC-offset Calibration

61: DC-offset Verification

62: Reset DC-offset to factory DEFAULT

:-) 60

HACK setting nonlinear zone sequence

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/etc/dc_cal.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/etc/dc_cal.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

ReadingIQbuffer.....(ok)

average beam 0 : -6

average beam 1 : -7

average beam 2 : 0

average beam 3 : -13

average beam 4 : -2

average beam 5 : -27

average beam 6 : -23

etc.

The offset for each of the channels is read. "Good" values are within +/- 150.

:-) 61

HACK setting nonlinear zone sequence

Loading tx setup from /hd0/usr/app/acquis/test/etc/tx_params.res

AcquisitionTest::feTest : using default ATGC curve

AcquisitionTest::feTest : disabling testsignal

Loading BF cache setup from /hd0/usr/app/acquis/etc/dc_cal.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Loading BF cache setup from /hd0/usr/app/acquis/etc/dc_cal.res

Loading TX cache setup from /hd0/usr/app/acquis/test/etc/tx_delays0.res

Reading IQ-buffer.....(ok)

average beam 0 : 0

average beam 1 : 0

average beam 2 : 0

average beam 3 : 0

A new offset for each of the channels is read. The old value is subtracted from the new value and the result is printed. "Good" values are within +/- 30.

:-) 62

:-)

9.7.3 RFT tests

Under this test we have shown how to enter the local test monitor. For the other boards the procedure is similar, but it is not shown. The reason that the test monitor is not shown, is that for service it is normally not necessary to do other tests that the automatic ones.

Enter **mon** to toggle monitor on. Enter **mon** once more to toggle monitor off.

:->> 2

2

: RFT automatic test ..... PASSED

:->> mon

MON flag is ON

:->> 2

Type "mon" to enter the test monitor.

Type the character "q" to leave the test monitor!

ft> mon

rftmon> tm

1 All
2 Wait state
3 DSP ext. RAM 0
4 DSP ext. RAM 1
5 IMP RAM
6 DEMOD RAM
7 OMP RAM
8 TAG RAM
9 WEIGHT RAM
10 LOG RAM
11 I buffer
12 Q buffer
13 All ext. RAM
14 Boot PROM
17 MLA 0
18 MLA 1 (RFP on J1,J2)
19 MLA 2 (RFP on J3,J4)
20 FULL BAND
21 CF (IQ)
22 Tissue
23 SD PW
24 Processing
25 Processing, all
26 Output addr. gen.
27 VME interface
28 FEC fifo com.
29 FEC serial com.
30 LED TEST

15 Conf. E2 PROM 31 PipeLink failure

16 FE bus interface 32

rftmon>

9.7.4 SDP tests

:->> 3

SDP automatic test .....IOP MID Exception:ID: 121,MDOM: 0,SDOM: 0,cond: 0,sev: 1,Error in interface to SDP,Request from SDP, but no active traces

SDP automatic test ..... PASSED

:->>

NOTE: The above listed Exception is normal.

9.7.5 CFP board

:->> 4

4

: CFP automatic test ..... PASSED

:->>

9.7.6 I/O Processor board

-:>> 5

5

: IOP automatic test ..... PASSED

:->>

NOTE: If you have older versions of the ECG board, warnings will be written before the testresult is written. E.g.:

IOP MID Exception:ID: 126,MDOM: 0,SDOM: 0,cond: 2,sev: 2,HW not recommended version warning,The Patient IO main board is not EMC compliant.

IOP MID Exception:ID: 126,MDOM: 0,SDOM: 0,cond: 2,sev: 2,HW not recommended version warning,The Patient IO input board is not correct version, periodically flat ECG could be the result.

9.7.7 IMPORT board

-:>> 6

6

: Image Port automatic test ..... PASSED

:->>

9.7.8 SCONV board

:->> 7

Before you can start any tests, the below text in *recursive* is printed.

7

SCONV5 found at VME address d4000000

Scan converter Functional revision: 4 software support level 4

tTdpSched id b66438 up and listening ...

tSdpSched id b61eb0 up and listening ...

SCONV5 Idprom

FO : 7577

Serial number : 0007

Functional revision : 04

Module Name : SCONV5

Part number : FA200029

MCD revision : 4

Production Date (dd.mm.yy) : 17.03.95

Date of last update (dd.mm.yy) : 06.06.95

Service count : 0

ID PROM structural revision : 1

Info string: [Originally rev C prototype. Updated with correct radix calc. in split.]

Then the test menu is displayed:

SCONV5 TEST

Test Status Command

Test access [P] 0

Test registers [X] 1

Test tables [X] 2

Test Tempstore [X] 3

Test TDP [X] 4

Test SDP [X] 5

Test All a

Toggle random/det r (current value: Random)

Toggle test looping l (current value: off)

TDP state t

SDP state s

Tempstore i

Tables j

Configure c

Quit q

Command: **a** (Enter **a** to start a full automatic test).

Some test pictures can be displayed on the monitor when running the automatic test (and the *SDP state* tests).

Note: Never try to alter any parameters in the *Configure* menu.

9.7.9 GRAPH board

:->> 8

GRAPH test ... WARNING!!

Some tests leaves the Graphic board in a "locked mode"!

This will obstruct a subsequent Scan Converter test.

Enter <CR> to continue or any other key to skip tests :

GRAPH automatic self test .....: PASSED

To print out status of internal tests [p]

To enter the Graphic board test monitor [y]

else return to BTM menu.

Please input a character [p/y/n] ?> ***n***

:->>

Note: Never try to alter any parameters in the *Update Configuration PROM* menu.

Your Notes:

Relay Board - RLY

10 Maintenance Aids

10.1 Configuration PROM

The configuration PROM U3 on the relay board has a hard-wired address of 000. It contains information about the board like part number and revision.

Transmitter Board - TX128 – rev. 04

11 Maintenance Aids

11.1 Test Points

TP*n*	Signal Name	Description
TP1		TPG 1 transmit cycle in progress. Active low TTL signal
TP2		TPG 2 transmit cycle in progress.
TP3		TPG 3 transmit cycle in progress.
TP4		TPG 4 transmit cycle in progress.
TP5		TPG 5 transmit cycle in progress.
TP6		TPG 6 transmit cycle in progress.
TP7		TPG 7 transmit cycle in progress.
TP8		TPG 8 transmit cycle in progress.
TP9	SAS_L	Synchronous address strobe
TP10	RFSH_L	Cache Refresh

Receiver Board - RX 128

12 Maintenance Aids

12.1 Test Points

TP*n*	Signal Name	Description
TP1	TSIG	Buffered test signal
TP2	VCTLP	Buffered TGC control voltage (non-inverting)
TP3	VCTLN	Buffered TGC control voltage (inverting)

12.2 Test Connectors

P*n*	Signal Name	Description
P6	TESTSIG	Analogue test signal

12.3 Configuration PROM

The configuration PROM U224 has a hard-wired address of 010. Its contents are to be decided.

Receiver Board - RX 64

13 Maintenance Aids

13.1 Test Points

TP*n*	Signal Name	Description
TP1	TSIG	Buffered test signal
TP2	XVCTL	Buffered TGC control voltage
TP3	XVREF	2.5V Reference voltage

13.2 Test Connectors

P*n*	Signal Name	Description
P6	TESTSIG	Analog test signal

13.3 Configuration PROM

The configuration PROM U109 has a hard-wired address of 010. Refer to the Master Control Document (MCD) for information about its contents.

Patient I/O

14 Maintenance Aids

14.1 Patient I/O Main Board

14.1.1 Test Points

TP*n*	Signal Name	Description
TP1	MCLK	Master clock
TP2	AVDD	Isolated digital +5 V supply
TP3	AVCC	Isolated analogue +5 V supply
TP4	AVEE	Isolated analogue -5 V supply
TP5	VDD	Non-isolated +5 V supply
TP6	RFS	Receive frame sync from A/D convertor

Front Panel

15 Test features

A local self test of the front panel is started by pressing ALT-SHIFT-1 after power has been turned on and “VINGMED SOUND” has been displayed in the upper display. (Note that the button ’1’ must be released first). By pushing the buttons A2, A3 and A4 different tests can be executed.

15.1 Address Decoder

Two PALs, ADDEC (U1) and DISPL (U3) provide the chip select signals to the different devices.

15.2 Revision Detection

The board part number and revision is written into a PAL, FPREV (U6). This information can be read by the uP and transferred to the system.

15.3 Serial Interface

There are two asynchronous RS-232 serial ports based upon a MC68681 DUART. One port is for communication with the system (Graphics board) and another (not currently used or shown on block diagram) can be used for VCR control.

15.4 VIA

The Versatile Interface Adapter (VIA) contains two 8 bit parallel I/O ports used to control the below described devices.

15.4.1 Beeper

The beeper can be activated by pulling the BEEP_L signal low.

15.4.2 LED activators / backlighting

The keys are lit in two steps: Backlighting is provided by enabling a BLEN_L signal, giving a quit dim light. This signal is automatically turned low when the ambient light is low, sensed by a light dependant resistor (RL1).

Whenever a button is depressed, the LED_EN_L signal (specific for each LED) is enabled, causing the current through the LED to increase, again increasing the light strength.

15.4.3 Trackball

The trackball interrupts the uP through the VIA when moved. Both it's X, Y and two quadrature outputs are connected to the VIA.

15.4.4 Toggle switches

The state of both toggle switches are sensed through the VIA.

15.4.5 Infrared (IR) Remote Control

The remote control interface has provisions for 32 different keys. The receiver and amplifier located on the Rotary/display board sends serial data to a receiver chip on the Main board. This device is connected to the VIA with five data signals and a IRDR_L (data ready) signal.

15.5 TGC slide potentiometers

The center tap of each of the 8 slide pot's are buffered and fed to a multiplexing 8 bit A/D converter giving out a digital value every 9 ms. The uP reads the TGC values independently of the conversion rate from a dual port RAM built into the A/D converter.

15.6 QWERTY keyboard and switch decoding

The overall keyboard matrix is 23 rows by 8 columns giving a maximum of 192 keys. One part of the matrix is used for the QWERTY keyboard, the rest is used for the other push-button keys. The matrix is address mapped. All columns are pulled high with resistors, and pushing a button causes that particular line to go low.

15.7 Rotary / displays board

15.7.1 Rotary decoding

The rotary switches are address mapped and read in pairs. They have 16 positions per revolution, and each position represents a four bit gray code which can be read by the uP.

15.7.2 Displays

The two displays (DP1, DP2) are character LCD units, with built-in control LSI. They operate under control of the uP, and displays alphanumeric characters and symbols. Two control signals (EN0 and EN1) from the address decoder, enables the displays.

16 Test features

A local self test of the front panel is started by pressing ALT-SHIFT-1 after power has been turned on and “VINGMED SOUND” has been displayed in the upper display. (Note that the button ’1’ must be released first). By pushing the buttons A2, A3 and A4 different tests can be executed.

Your Notes:

17 Power-up Test

17.1 Description of Test

Not yet implemented.

(The only board which is tested during power-up is the IMPORT board, which answers “*Image board present!* if it is ok”).

17.2 Power-up Verification of Hardware Configuration

During power-up the hardware configuration of the system is verified. If incorrect Part Numbers of e.g. RX and BF has been installed, the system will recognize this and print an error message on the terminal while booting.

Macintosh HD:User:James:@i-ath:Service:S5_ServiceMan:S5_serv_files:K10_PowerUpTest.12.
Printed: December 5, 2000.

Your Notes:

18 Performance Test (System Test) Procedure

18.1 Introduction

18.1.1 Abstract

This document is made to ensure that all systems are tested according to the specifications. Most of the specifications are not objective and require live scanning on yourself or an image phantom.

This Performance Test Procedure is based on the Internal System Test Procedure,
GEVU doc. no.: FA010050, used prior to shipment from the factory.

18.2 Scope

This procedure concerns Advantage, Performance and Premium, there may, therefore, be some deviations in functions between systems.

18.3 Initial Checks

18.3.1 Software

1.) Turn the system on and display the Software Revision Menu (Setup:Configuration & Test:Software Config:)
2.) Verify that the sw version is at the level stated in the Device History Record (DHR).
3.) Check also that the sw is correct according to the Packing List.

18.3.2 Hardware

1.) Display the Hardware Revision Menu (Setup:Configuration & Test:Hardware Config:).
2.) Verify that it matches the printed configuration data in the Device History Record.

18.3.3 User Interface

1.) Verify that the monitor is operational and properly adjusted (refer to Service Note).
2.) Verify that the Front Panel backlighting and LEDs are working. Ref. "Front Panel Test" on page K11-2.

18.4 Automatic Tests

18.4.1 Tests via SysTest Menu

1.) Connect a FPA probe in connector 1.
2.) Press the Setup button.
3.) Enter the Configuration & Test menu
4.) Start the Automatic Test in the Diagnostic Test and verify that all tests pass.

18.4.1.1Analog BF Test

(Only if the dummy connector is available)

To do this test you need a dummy connector GEVU Part Number AA200190.

1.) Put the dummy connector in connector 1 and start “analog BF test” in set up, system test menu.
2.) Do this test with all connectors.

18.4.2 FE Calibration of DC Offset

- Please refer to the FE "Calibration" Procedure, starting on page K16-1

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K11_SysTest.13.
Printed: December 5, 2000.

18.5 Motherboard Hardware Configuration

(Only if the settings have been lost or corrupted)

1.) Connect a terminal or PC with terminal program to a debugger board, connected on the FEC.
2.) Put a dipswitch on the FEC to enable configuration.
3.) Boot the system and look at the terminal.
4.) When «FEC Appl» applies, write: m, and press «enter».
5.) To enable configuration write: hw -set -m mb.
   a.) Enter s/n equal to system serialnumber,
   b.) correct module rev.,
   c.) name,
   d.) p/n,
   e.) MCD rev.,
   f.) date
6.) See that the transaction is done.
7.) Turn off the system and remove the debugger board and the dipswitch.
8.) Enter Setup Menu and check that the Hardware revisions, in System Test, is updated.

18.6 Front Panel Test

18.6.1 Start of test

1.) When system is fully booted, push down **ALT**, **SHIFT** and **1** after "VINGMED/SYSTEM FIVE" is displayed. (Release **1** first, then the other two buttons).
2.) Verify that you now have the following text in the two LCD displays:
   - **Upper display**
     * SW VER
     * DATE
     * OK
     * CONN
   - **Lower display**
     * EXIT
     * TEST
     * CLEAR
     * REBOOT

DESCRIPTION

* SW VER is the current local front panel software version.
* DATE is the date of software release.
* OK is the status of a serial communication test. Otherwise ERROR will be displayed.
* CONN
* EXIT test mode.
* TEST enters test mode.
* CLEAR
* (REBOOT is used during in-house module test of serial communication.)

3.) Enter test mode.
You will now have the following text in the Lower LCD Panel Display:
* DONE
* DOTS

* LEDS
* KEYS

18.6.2 Display test

- Press **DOTS**: All dots in the display should light up.

18.6.3 LED test

- Press **LEDS**: The backlighting LEDs for all keys should be lit.

18.6.4 Key test

1.) Press **KEYS** (the LED will blink):
2.) Pressing each of the keys will result in a beep and the hex code for that particular key will be displayed in the Upper Keyboard.

18.6.5 Rotary knob test

- Turn the rotary knobs. A 4-digit code in the upper display shows up.

The first two digits is a code for the 8 rotaries.

> 00-03 are the knobs between the display.
> 04 is the ACTIVE MODE knob,
> 05 is the 2D GAIN knob,
> 06 is the ZOOM knob and
> 07 is the DEPTH knob.

The last two digits indicates the direction of rotation:

> low numbers clockwise and
> high numbers counterclockwise.

18.6.6 Paddle Stick test

- Move the paddle sticks. Another 4-digit code in the upper display shows up.

The two left digits indicate the paddlestick number:

> 00 is the upper and
> 01 is the lower.

The two right digits indicate the position of the paddlesticks:

> 00 is up (or left),
> 01 is center and
> 02 is down (or right).

18.6.7 TGC Slidepot. test

- Move the TGC slide pot.'s. A 16 digit code (divided in eight 2-digit sections) in the upper display shows up. The position of the upper slide pot. is displayed in the upper left section of the display code field, and the lower slide pot. is displayed in the lower right code field.

Values range from:

> 00 (slide pot. left) to
> 1A (slide pot. center) may vary from 18 to 1C
> 33 (slide pot. right).

18.6.8 Trackball test

- Move the trackball up and down, left and right and verify the corresponding position of the arrow on the upper display.

18.7 Peripheral and I/O Tests

18.7.1 PAL/NTSC Setting

Selection of PAL/NTSC must be done in the Video Settings menu (password: setfive).

- Set both Video Standard and External Video Input to the appropriate video standard.

(USA: NTSC, Europe: PAL, For other countries/territories: Contact the local GE Vingmed dealer for info.)

18.7.2 Record and Playback

1.) Record 2D and Color Flow alternately and then Doppler with audio.

2.) Play back the recorded tape and verify the quality of the playbacked picture. (Expect some degeneration of the picture, compared to the recorded one.)

3.) Verify clean unsaturated Doppler audio.
If necessary, adjust the AUDIO LEVEL potentiometers on the VCR to avoid saturation.

If Remote Control is installed, use the assignable keys to operate the VCR functions.

18.7.3 Printer Test

1.) Connect a B/W printer to the Video Output connector.

2.) Enter 2D and obtain an image.

3.) Press print on frontpanel, and verify quality of the print. If necessary, adjust the printer controls.

4.) Connect a color printer to the RGBS output connector.

5.) Enter color flow and obtain an image.

6.) Press Print(Alt.) on frontpanel, and verify quality of the print. If necessarry, adjust the printer controls.

18.7.4 Footswitch

- Test the footswitch interface (use 2D mode for the test).

Default setup:

> Left:Rec/Pause,

> Middle: Full Freeze,

> Right: Image Store.

18.8 External I/O Tests

18.8.1 Video out

- With an oscilloscope, verify presence of video signal. Typical signal level: 2.2 Vpp.

18.8.2 S-VHS Out

- With an oscilloscope, verify presence of S-VHS signal. Typical signal level: 2.0 Vpp

18.8.3 RGBS Out

- With an oscilloscope, verify presence of RBG signals.Typical signal level: 1.8 - 1.9 Vpp

18.8.4 MAC Interface Test - Stand Alone MAC only

- If a Stand Alone MAC with EchoPAC is to be used with the system, test that Data Transfers work properly when using the Transfer Data Kit.
- Try both short-cut tests (with the F9 key) and transfers from the clipboard. If Standalone Mac has Continuous Capture option, refer to "Macintosh with Continuous Capture" on page K11-5.

18.8.5 ECG

1.) Connect ECG simulator or electrodes.
2.) Turn traces on.
3.) Verify an ECG trace on the monitor.

18.8.6 Phono

(Optional Test)

1.) Connect a Heart microphone and turn Phono on.
2.) Verify quality and presence of phono trace.

18.8.7 Respiration

(Optional Test)

1.) Connect a Respiration transducer and turn Respiration on.
2.) Verify quality and presence of respiration trace.

18.8.8 Pressure

(Optional Test)

1.) Connect a Pressure transducer and turn Pressure on.
2.) Verify quality and presence of pressure trace.

18.9 Integrated Mac

18.9.1 Setup Check

1.) Exit EchoPAC,
2.) Select EchoPAC Application in HD A and choose «Get Info» in the File-menu.
3.) See that EchoPAC has the correct preferred size of memory.
4.) When starting EchoPAC, verify that the EchoPAC modules specified on the packing list, are enabled with the password delivered.
5.) If systems is going to be used in USA:
    - Check that Ob/Gyn is not an option in the application menu.

18.9.2 Macintosh with Continuous Capture

You need the EchoStress option installed for this test to work.

1.) Select FPA probe
2.) Select Video Stress Application
3.) Enter live 2D tissue scanning mode on S5, make sure that there is an ECG signal to the scanner while doing the test.
    a.) Switch to EchoPAC mode.
    b.) Enter stress-test mode in EchoPAC.
    c.) Turn 'Continuous capture' on.
    d.) Step on the middle footswitch. Verify that EchoPAC starts grabbing a new window with the live 2D scan pops up in the middle of the EchoPAC - screen.
    e.) Verify that no lockups occurred when filling the hole memory, and verify that all the ECG traces are transferred during the capture.
    f.) Finish Procedure and Delete Capture (Right footswitch)

18.9.3 Communication with Scanner

Use System Front Panel (not external keyboard) when doing this test to be sure communication is ok.

1.) Choose Patient IO on Scanner, verify screen switches to EchoPAC and create a new Patient.
2.) Enter some patient data, and click the «save» button.
3.) Verify screen switches to scanner and make sure the info window is updated with the same information you entered in EchoPAC.
4.) Transfer data by selecting Image Store key when;
    a.) Scanner is running or replaying a cineloop,
    b.) A frozen 2D tissue scan is present.
5.) Also transfer data from:
    a.) Color Flow mode (CFM),
    b.) M-mode,
    c.) Doppler mode.

18.9.4 Hardware Check

1.) Connect a mouse or keyboard to the keyboard port, and make sure it works properly.
2.) Connect a Stylewriter (printer) to the printer port and print a report from the patient archive. If proper printer-driver is missing, install it from disk and delete it after the printertest is done (if necessary).
3.) Verify ability to save and recall to/from the MO-disk to verify proper functionality.
4.) Verify the eject function by pushing «Fn» and «E».

18.9.5 Screen Switching

1.) Switch to EchoPAC with the 'EchoPAC' button.
2.) See that the entire screen is used to display EchoPAC, and that track-ball works.
3.) See that help is displayed in EchoPAC when the 'HELP' button is used.
4.) Switch back to S5, and verify placement /image quality.

18.9.6 VCR Recording

1.) Start recording with VCR
2.) Switch between S5 and mac via EchoPAC key.
3.) Stop recording, rewind and play back the tape. See that the recorded data is the same that was shown on screen. Verify quality of recording.

18.9.7 EchoPac-3D

If EchoPAC-3D is installed, perform this test to make sure it works properly.

1.) According to EchoPAC-3D User Manual, FA292617, perform a 3D acquisition on a non-metallic phantom, make a cineloop and transfer it to the Macintosh through EchoPAC. The acquisition should be done with a slowly translated and/or tilted movement along the top of the phantom and by using the Long Acquisition application on System FiVe.
2.) Exit EchoPAC and start EchoPAC-3D.
3.) Open the loop in EchoPAC-3D and verify correct representation by;
    a.) Looking at the geometry window and see that the acquisition geometry looks correct.
    b.) Measure a distance (5-10 cm) between two strings (horizontally) in the phantom in the plane normal to the middle scanning plane (select lower left window, use 2D M&A) and verify that it is correct (+/- 10 %). This is to ensure that Bird System reports correct positions of each scanplane relative to each other
    c.) Select the upper right window and select "Raw Path" in the left dialog bar. By grabbing the slidebar in

the window, it is possible to browse through the original 2D scan planes while looking at their positions in the geomtry window. Verify that the movement of the scanplanes is smooth like the movement that was done with the probe during acquisition. This is to ensure that there is no noise affecting the position sensor system (which would make the 3D data look "jumpy").

18.10 Monitor Setup

- If neccesarry, adjust monitor according to "Monitor Setup Procedures" on page K18-1.

18.11 Functional Test

1.) Connect a 2.5 or 3.5 PA probe to the system.
2.) Reselect probe to obtain default settings.

18.11.12D Controls

1.) In 2D mode, set 2D Gain and the TGC knobs to get even signal distribution for all depths when measuring on a phantom.
2.) Vary depth from minimum to maximum and verify that the field of view changes accordingly.
3.) Vary Angle/Width and verify that there is no distortion for any combination of depth and width.
4.) The Freq. control.
    a.) Turn Freq counterclockwise and verify that the penetration increases.
    b.) Turn Freq clockwise and verify that the resolution increases. Pay special attention to the Octave settings.
5.) Turn Focus and verify improved image sharpness within the focused area.
6.) The Zoom control
    a.) Press Zoom once,
    b.) Adjust proper zoom span,
    c.) Press Zoom once more and verify a proper zoomed image.
    d.) Press Zoom a third time to exit.
7.) Change Reject and verify how low level echoes are rejected when Reject is increased.
8.) Change Compress and verify increased contrast for low compress settings and softer image for high compress settings. Verify functionality in Freeze.
9.) Change Dynamic Range and verify “soft” images for high settings and “harder” (increased contrast) images for lower settings.
10.) Verify performance of DDP on a moving target, no averaging at minimum DDP and increasing averaging with increasing DDP.
11.) Freeze the image, then use the trackball to scroll back into the memory.
12.) Press the Image Store button to store a frozen image to the harddisk clipboard. Press Image Recall to restore this image: (Must select this configuration in EchoPAC clipboard)
13.) Connect a 10 MHz FLA probe, press Compound and verify increased resolution (not available on FA000410).

18.11.2Doppler Controls

1.) If necessary, reselect the probe to bring it to default settings, and select PW.
2.) Increase Gain to maximum and change the Horizontal sweep from minimum to maximum, and verify 1, 2, 3, 4, 6, 8, 12 and 16 seconds of data across the TM field. Freeze and check the scrolling memory using the trackball.
3.) Obtain a good Doppler spectrum measuring on yourself or on a flow phantom. Change Velocity Range and verify that the vertical scaling of the spectral display changes accordingly.
4.) Move Baseline up and down and verify proper response.
5.) Decrease LV Reject and verify that low velocities are displayed. Increase LV Reject and verify that the low velocities are rejected.

6.) Increase Compress and verify increased brightness in the spectrum.
7.) Increase Reject and verify that the low level signals (noise) are rejected.
8.) Increase Sample Volume from minimum to maximum and verify that the sensitivity increases.
9.) Obtain a strong and good signal. Increase Tracking and verify that the signal is getting weaker but the quality of the spectrum is getting better (not available on FA000410).

18.11.3Color Flow controls

1.) If necessary, reselect the probe to bring it to default settings. Then obtain a good 2D image while scanning yourself or a flow phantom.
2.) Decrease PRF to minimum and verify that the Nyquist limit is decreased (aliasing) and that low flow filling is improved. With PRF to maximum, Nyquist is increased, but sensitivity appears to be less.
3.) With medium PRF, decrease LVreject and verify that the low flow signals are visible. With high LVreject settings, the low flow velocity components are rejected.
4.) Increase Gain and toggle Variance on and off. With Variance on the noise should be green.
5.) Increase Radial averaging from minimum to maximum and verify the effect of the averaging.
6.) Change Sample Volume from minimum to maximum and verify that the sensitivity increases and the axial resolution decreases.
7.) With maximum Tissue Priority, observe tissue priority over color (no color at max), and the opposite for minimum Tissue Priority.
8.) Increase Lateral averaging and observe increased averaging in the lateral direction.

18.11.4MPTE Test (PAMPTE)

1.) Connect a MPTE-probe (KN100007/KN100006) or simulator (KZ206319).
2.) If probe, hold your hand on the probe tip and verify that the temperature increases.
If simulator, adjust temperature potentiometer and verify that the system enter freeze at 41.1ºC.
3.) Verify that the system's display of the scanplane, tracks the position of the wheel on the endoscope.

18.12 M-Mode Tests

18.12.1Linearity

1.) With the system in 2D and the probe positioned on the phantom, press the add mode / cursor button to show the M-mode cursor.
2.) Position it so that it covers the reflectors that are found in the center of the standard phantom image.
3.) Adjust TGC and gain to get a good image of the reflectors, both in the 2D sector and in the TM field.
4.) Vary the depth setting and verify that the image changes accordingly.
5.) With the probe in the standard position, place the cursor on the string target found at 8 cm depth, 4 cm to the right of center.
6.) Enter M-mode and verify that the target is displayed in the TM field.

18.12.2Color M-mode Test

1.) If necessary, reselect the probe to bring it to default settings.
2.) Obtain a proper 2D image, then enter Color M-Mode.
3.) Increase M-Mode gain and see how signal/noise is increased.
4.) Check that there are no signs of coherent noise.
5.) Switch to Color Flow settings and adjust color gain to verify response. The color noise intensity (in the color flow window) will increase when the color gain is increased. Look for color spots with higher intensity and size than the rest. If you find any, decrease the color gain slowly, until the color noise fades away. If the spot you noticed fades away after the rest of the color noise, you may have a noise problem in Color Flow.

6.) Vary depth span and see how the size of the color section can be altered.
7.) Increase sample volume and verify increased sensitivity.
8.) Verify all sweep speeds.

18.13 Image Quality and Noise

Image quality and noise tests must be done in all modes, with the probes listed below (if available).

- KG100001 2,5 FPA 1C
- KK100001 3,5 FPA 1C
- KK100004 3,5 CLA 1A
- KN100001 5,0 FPA 1A
- KN100002 5,0 FPA 2B
- KW100001 10 FLA 1A
- TE100024 PEDOF (non imaging probe)

18.13.12D Mode

1.) In 2D mode, set 2D gain and the TGC knobs to get even signal distribution for all depths when measuring on a phantom.
2.) Pay careful attention to both axial and lateral resolution, as well as penetration.
3.) Note the shape and quality of density patches, ability to resolve nearby blips, far field blips.
4.) There should be no visible zone transitions.
5.) With maximum 2D gain, check the noise level when coupling the probe in your hand. Pay special attention to noise straight down through the image. With no external devices connected to the I/O panels, there should be no excessive coherent noise patterns.

18.13.2Doppler Mode

1.) With default setup of each probe (not Pedof), obtain a good 2D image, enter CFM, press active mode / cursor and position the sample volume within an area with flow. Then enter Doppler.
2.) Verify good sensitivity and no excessive noise bands when velocity range is changed.
Check both with and without 2D frozen. This applies to both PW and CW (not FLA and CLA).

18.13.3Color Flow Mode

1.) With default setup of the actual probes, obtain a good 2D image on the appropriate anatomy and enter CFM mode.
2.) Verify good sensitivity and acceptable noise level (no coherent noise nor excessive white noise). A little noise straight down is currently normal, especially if external cables (e.g. ethernet) is connected to the system.

18.14 Apat Probes

If an Apat Probe Support kit, FA200536, is installed, and an 3.25 MHz Apat probe (TK100104 A) is available, this test is to be performed.

1.) Test the apat probe in different modes as described for phased array probes in Section 18.13. It may be some miner deviations, and some noise may occur in doppler modes.
2.) Check also M-mode and CFM.

18.14.1AA MPTE Mechanical Probe (or Simulator)

1.) Connect a TE-Probe (TE100053) or simulator (ML200366).
2.) Adjust the temperature and verify that it updates. Verify that the system freezes when the temperature exceeds 41.1ºC.
3.) Verify that the multiplane rotation can go from 0 to 180 degrees.

18.15 Options

- Check and confirm proper functionality on ordered options, listed on the packing list.

18.16 Hardware Revision Level

1.) Press the Setup button
2.) Select the SysTest menu
3.) Select Hardware Config.
4.) Verify that there is a match between the read-out of the hardware revision numbers and the information on the Configuration sheets.

19 Lock-ups and Bus Errors

19.1 VME Address Map

Below is a list of the VME address map. It may be useful when troubleshooting bus errors. After a bus error has occured, some addresses are printed to the RS-232-CPU port on the EXT I/O panel. If a terminal is connected, this information can be read. The addresses shown below are what is called the **access address** on the terminal.

Board	Start Address	Address Size (MB)
IMAGE MEM.	0x08000000	64
IMAGE Port2	0x80000000	
GRAPH	0xd0000000	8
SCONV	0xd4000000	4
IMAGE PORT	0xd5000000	4
FEC (Cache)	0xd6000000	7
CFP	0xf0000000	1
SDP	0xf0100000	1
RFT	0xf0300000	1
FEC (Local)	0xf0700000	1
IOP	0xf0800000	1

If the access address listed in a bus error printout, is within one of the above address areas, the accessed board is likely to cause the bus error, and replacing it is worth a try.

19.2 Task Trace

After a system lock-up it may be useful to "go back" to see what happened right before the system locked. That can be done if the PC/terminal is connected to the RS-232-CPU connector (however, on some lock-ups even the communication over this port is dead). By writing **tt tSuperv** after the prompt (>) followed by return, the CPU will print the last code that was executed, thus giving you an idea of what boards that where accessed. (If the system is dead, either nothing or "syntax error" will be printed).

Macintosh HD:User:James:@I-ath:Service:S5_ServiceMan:S5_serv_files:K12_Lock-ups.15.
Printed: December 5, 2000.

Your Notes:

20 System FiVe Noise Guide

20.1 Noise Sources/ Fixes

20.1.1 External Noise Conducted via Mains Line.

A standard mains ferrite filter is installed into the AC Power. If additional filtering is required, an external ferrite may be added.

20.1.2 External Noise Conducted via External I/O Connectors.

Connecting equipment to the EXT I/O board, most often will introduce common mode noise into the system.

The most typical noise problem is coherent noise patterns straight down in the image field. Usually the noise is only picked up when coupling the probe to your body.

Disconnect all external cables to the EXT I/O board (if mounted) to establish whether the noise is due to interference from external devices. There are possible ferrite solutions to most of the cable connections, including the ethernet connection.

- On the cable harness between System-5 and a the MAC: Wind the cable three times trough a ferrite ring, 038X0028.
- On video cables: Wind the cable 5-6 times through a ferrite ring, 038X0028.
- On RS232 cables: Wind the cable 5-6 times trough a ferrite ring, 038X0028.
- When installed in LAN network: Use the VMS ethernet noise filter cable, p/n FA200460 between the system connector and the AUI adapter box.

Macintosh HD:User:James:@k-arb:Service:S5_ServiceMan:S5_serv_files:K13_NoiseGuide.12.
Printed: December 5, 2000.

20.1.3 External Noise Radiated Into the Probe Tip.

If none of the above ferrite fixes helps, the noise could be radiated.

Depending on the frequency and the field strength, radiated noise may be picked up by the probe. The best way to avoid this is to have a properly shielded cable and probe house, and to have good connection to ground via the system connector.

It is very important that the metal plate in front of the RLY board is properly screwed into the frame. All screws around the PA connectors as well as the AA connectors must be in place.

20.1.4 Green Noise Straight Down in CF

In the V1.2 SW, noise is mapped to more green than previously. This makes coherent noise (straight down with FPA probes) more visible.

- RX128 test signal fix. See V1.2 upgrade. Reduces straight down noise.
- FPA2.5 probe, KK100001 rev.A (1A on label). These probes are poorly shielded and easily pick up noise. Rev.B are much better (6-7 dB) with respect to noise immunity.

20.1.5 Green Random Dots in CF or White Dots in 2D

Random color dots within the color ROI are in 95% caused by bad Focusor chips on the BF boards. This is usually a heat related problem, that's been improved by put-

ting heat sink plates on the BF boards. There is now a solution for this (a fix in the BF Focusor asic), but there are many boards out in the field that exhibit this problem.

20.1.6 Color Noise Artifacts with FLA and CLA Probes

Color Flashes:

Quite often there are narrow (1-2 mm) flashes going through the whole color ROI in the steering direction. Reason and source is unknown.

Near field noise:

Within the first 0-3 mm, there may be some flickering noise with some FLA probes. Easiest seen when steering straight down and having color ROI at the very top.

Color “sectors”:

With the FLA probes, you may see narrow sectors of noise originating at the top spreading down trough the color ROI. However, at default gain setting, these sectors should not be visible. They are usually due to excessive noise on a specific channel. Could be caused by the probe, TX, RX or BF boards. There are techniques to narrow this down.

20.1.7 Doppler Noise Bands

FPA and AA probes:

PW: It is currently normal with noise bands in PW whenever sample gates are positioned close to the probe inside a strong tissue signal. This saturates the receiver and for some reason causes bands at frequencies changing with the prf.

CW: Some noise bands (typ. below 2 m/s) may be present with some probes. System dependent. usually when focusing far out and straight down. May be improved by grounding of shield boards, see below.

20.1.8 DC Power Supply

Switching noise from the DC Power Supply may cause noise straight down in 2D. If such noise is present also after having removed the XDBUS boards, it may origin from the power supply.

DC Power supplies have caused excessive noise on ECG, but only on 128-channel systems and only when ECG disconnected.

20.1.9 TX Power Supply (HV Supply)

Some down rev. TX Power Supplies have been found to have severe banding in Doppler at maximum Power setting. If the noise is disappeared if Power is reduced one or two clicks, the noise is likely to be caused by the TX Power. All supplies should be upgraded per the V1.2 upgrade procedure.

20.1.10Grounding

- Grounding of shield boards to chassis, both up and down. Otherwise there may be noise in 2D (white noise straight down), Color Flow (green noise straight down) and/or Doppler (horizontal bands).
- Make sure that the shield for the Patient I/O cable is connected to ground. Otherwise you may have flashes of noise straight down.

21 Fuses and Circuit Breakers

For location of the different fuses, see the Assembly Drawings section of the service manual.

Location	Fuse Type	ID	GEVU P/N	Description
AC Power box, mains switch	10 A (15A) circuit breaker (recovery)		220V: 052H2010 (110V): 052H0003	Located on mains lines going into the system. Breaks all AC currents to the system.
AC Power box	Current limiter	R1	"Old": 046M0140 "New": FA200558	Located on the mains lines. Prevents current surges from tripping the hospital fuses.
Inside Isolation Transformer	Thermal recovery fuses (130°C)		038D1313 (transformer)	In series with the mains lines. Breaks all AC currents to the system if the temp. inside the transformer exceeds apprx. 105°C (current dependant). **Note:** Not used in systems with new current limiter p/n FA200558.
AC Controller board	10 AT/220V 15AT/115V glass fuse	F1, F2	10A: 046A9000 15A: 046A9500	In series with the 115V/230VAC mains lines to internal distribution. **Note:** Does not break power to the STBY ON/OFF switch.
AC Controller board	4 AT glass fuse	F50	046A4000	In series with tone of the 12VAC lines to the local stand-by power supply on the board. Breaks power to the STBY ON/OFF switch
AC Controller board	Relays	K1, K2		In series with the 230VAC mains lines to internal distribution. Controlled by the STBY ON/OFF switch on the front of the system, and by a thermal fuse on the Temp Sense board, see below.
Temperature Sense board	72°C thermal non-recovery fuse	TF1	046T6202	In series with the coil for relays K1 and K2 on AC Ctrl board. Will blow if temperature exceeds 72 ^{o}C. In that case it will be impossible to turn the system on before the fuse has been replaced.
Temperature Sense board	60°C thermal recovery fuse	TF2	046T6205	High Temp alarm. Will cause fans to run at full speed if the temperature exceeds 60 ^{o}C.
Temperature Sense board	NTC (thermistor)	NTC	002N2202	Senses air temperature above CPU. Controls fan speed.
DC Power Supply	6.25 AT non recovery glass fuse	F101	(6.3 * 32)	In series with one of the mains lines inside the DC Power. (In the bottom). If blown, there will be power in STBY ON/OFF switch, fans and peripherals, but not in the card rack.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K14_Fuses.12.
Printed: December 5, 2000.

Location	Fuse Type	ID	GEVU P/N	Description
Rev.A and onwards TX Power Supply	200mAT non recovery glass fuse	F1	046A0200 (5 * 20)	In series with one 220VAC mains line on primary side of local transformer. If blown, there will be no high voltage.
TX (HV) Power Supply	200mAT non recovery glass fuses	F2, F3	046A0200 (5 * 20)	In series with both 110VAC lines on secondary side of transformer. If blown, there will be no HV1 (0 - +/- 80VDC). HV 2 will be ok.
TX (HV) Power Supply	1.6AT non recovery glass fuses	F4, F5	046A0200 (5 * 20)	In series with both 55VAC lines on secondary side of transformer. If blown, there will be no HV2 (0 - +/- 40VDC). HV 1 will be ok.
Relay Board	200mA (changed to 1.1A) recovery multifuse (PTC)	F1	200mA: 046U0200o r 1.1A: 046U0110	In series with +15VDC line to Cannon connectors (and to 5 chips on RLY). Will only affect the 192 element linear probes.
Probe Control Board	3 AT (changed to 5AT) non recovery subminifuses	F1, F2	3A: 046P3000 or 5A: 046P5000	In series with the +/- 15VDC lines to the power amplifier driver for AA probes. If blown, will cause AA probes not to run.
Internal I/O	4 AT recovery multifuse (PTC)	F401 F403 F404	046U0500	In series with +12V (F401), +15V (F403) and -15V (F404) to the DC power connectors on INT I/O.
Internal I/O	1.1 AT recovery multifuse (PTC)	F402	046U0110	In series with -12V to the DC power connectors on INT I/O.
Internal I/O	6 AT recovery multifuse (PTC)	F400	046U0800	In series with +5V to the DC power connectors on INT I/O.

22 Voltage Distribution Overview

This is a list of the power distribution in the system. On each board the voltages are labelled vcc, avdd etc. on the schematics. These labels are filled in the table below. An x is filled in where there is no label or where the voltage is regulated down.

Board	+5D	+5A	-5A	+10	+12	-12	+15	-15	HV	+/- 80
LA probes							x			x
RLY		avcc	avee				avdd			(x)
TX128/ TX128-2		vdd	avee	vdd1					x	
RX128 RX64		avcc	avee				x	x		
PRC		vdd	vee				vdd1	vee1	x	
BF1-4	vdd	avcc	avee							
FEC	vdd	avcc	avee				avdd	avss		
PAT I/O	vdd									
RFT	vdd		avee							
SDP	vdd		avee							
CFP	vdd		avee							
IM PORT IP2	vdd		avee							
GRAPH	vdd		avee		x	x				
SCONV	vdd		avee							
MEM	vdd									
CPU	vdd				x	x				
INT I/O	vdd	avcc	avee		vdd1	vee1	avdd1	avee1		
EXT I/O	vdd				vdd1	vee1	avdd1	avee1		
FP	vdd						avdd	avss		
Harddisk	x				x					
TX Supply		avcc	avee				avcc1	avee1	x	x
MBD	vdd									
AC Ctrl	The board has a local power supply with +5V and +12V.									

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:K15_VoltageDistr.13.
Printed: December 5, 2000.

Your Notes:

23 FE "Calibration" Procedure

23.1 Introduction

Each A/D converter on the BF boards has an offset error (i.e. gives an output code different from 00 Hex with an input voltage of 0V). This offset error may cause artifacts in some modes of operation (2D and TVI) due to inaccuracy in the demodulation process. In order to deal with this problem, the software V1.2 has support for cancelling of these offset errors. This is done by first reading the offset error and then accounting for these numbers later during the normal processing.

23.2 Setup

The only requirement when doing this procedure, is that a probe must be inserted in connector 1.

23.3 When to Use This Procedure

This procedure should be performed on all systems after sw. upgrade to V1.2 and beyond, and;

- whenever a BF board is replaced or
- whenever BF boards are interchanged or
- whenever the hard disk is replaced.
- when installing a System FiVe scanner at end user's site

23.4 Procedure

1. Press the Setup button on the keyboard.
2. Select Configuration & Test.
3. Select GE Service
4. At the password prompt, enter service
5. Select Calibration.

   Each A/D converter will get 0V input (by setting ATGC to minimum). One by one channel will be digitized and the result put in the IQ buffer on the RFT board. The CPU will then read the IQ buffer and compare these numbers with a known "good" limit. In order to verify that the numbers read are correct, a verification reading is done: The A/Dsz are read once more, the previously read numbers are subtracted from the recently read numbers and the result should now be 0 (or +/-1).

   If all read values are ok, the message PASSED will appear. If values exceeding the preset limit are read, the system will prompt you with FAILED and a message telling which BF board that is bad.

   The resulting offsets for each channel is stored in a file on the harddisk on the directory */hd0/usr/app/acquis/etc*.
6. From SW V1.3, the values can be plotted in a diagram.

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:K16_FE_Calibr.12.
Printed: December 5, 2000.

Your Notes:

24 Debug Commands

The following is a list of debug commands that can be written on the PC/terminal when connected to the CPU RS-232 serial line. The commands must be written at the > prompt:

Debug Command	Description
modSetupDebug=0x2	This command lists the high voltages output from the HV Supply and the estimated peak voltage applied across the probe elements. Note that you must alter parameters affecting the power in order to get this information listed out (e.g. Power).
probeReport	This command lists the connected probes which are recognized by the system.
reboot	This command will reboot the system.
bootChange	With this command you will enter the CPU configuration PROM.
tt tSuperv tt<space>tSuperv	This is a so-called task trace command, used to print error messages after a system bus error has occurred.

Macintosh HD:User:James:@:+arb:Service:S5_ServiceMan:S5_serv_files:K17_DebugCommands.12

Your Notes:

25 Monitor Setup Procedures

25.1 Monitor Setup Procedure

This procedure applies to the Eizo 562 and 563 model monitors.

1. Press the select button surrounding the adjustment wheel in the front of the monitor.
2. Select Color using the wheel and the select button.
3. Set sub-contrast to 100%. Then rotate the wheel until the arrow in the bottom right side is highlighted. Then press the select button to save the sub-contrast level at maximum.
4. In the main menu, select Screen and set Contrast to maximum.
5. In the main menu, select Image and set Moire Reduction ON.

Macintosh HD:User:James:@I-arb:Service:S5_ServiceMan:S5_serv_files:K18_Monitor_Setup.02.
Printed: December 5, 2000.

25.2 Monitor Setup Procedure, (from sw. 1.5 and up)

25.2.1 Preface.

These are procedures for the EIZO Color Display Monitors to be used as part of the V1.5.x System Software upgrade.

25.2.2 EIZO FlexScan T57S and TX-C7 models

The setup of this monitor is completely changed compared to what it was before. Before the color intensity and background was adjusted using the RGB Gain and Cut-off adjustments. Now, a color temperature of 10.000K is used. This simplifies and standardises the setup, and it also improves the presentation of color images in particular. This procedure is written specifically for field used. (The system production procedure uses an optical color balance meter to make the final adjustment of the color balance).

Screen Manager Initial settings

- Press the MIDDLE switch to enter the Screen Manager. Select Color, Color Mode and then Standard.
- Exit back to Screen Manager, select Screen, Contrast and select 50% brightness and 90% contrast levels.

Getting into the Service Menu

- Press the MIDDLE switch to enter the **SCREEN MANAGER** menu.
- Select **Information** menu.
- In **Information menu** (page 1 of 4) press gently (not too hard) down to mid position on the DOWN arrow .
- While holding the DOWN arrow, press and hold AUTO. (The monitor will beep and blank out after a few seconds). At this time release both keys.
- Press the MIDDLE switch. You are now in the SERVICE menu.
- Verify that the menu is not identified as **screen manager** menu.

Color Menu Setups in Service Menu

- Select **COLOR** menu.
- Select **Temperature.**
- Set temperature to **10000K**.
- Press middle select button to set.

- Select **GAIN** menu.
- Set sub contrast (the black half moon) to **250**. (NOTE: This is a preset. Final contrast level is set later).
- Press middle select button to set.

- Select **CUT OFF** menu.
- There will appear a red sun, green sun, blue sun and black sun.
- Set sub brightness (black sun) to a value where the sector edge is just visible.
- Press middle select button to set.
- Select **Save** menu.
- Exit **COLOR** menu.
- Exit Service menu.
- Power monitor off and on again.

Allow 5 minutes warm up time before continuing.

Contrast and Brightness setup in Screen Menu

Press middle select button to enter **Screen Manager menu.**
Select Screen.
Select Contrast.
Set **CONTRAST** (black half moon) to somewhere between 80 -100 %, depending on desired intensity level .
Set all TGC slide pots to minimum.
Fine adjust **BRIGHTNESS** (red sun) so that the sector edge is just visible.
Press middle switch to set.
Exit **SCREEN** menu.

Moire Reduction Setup

Select **screen** menu.
Select **moiré reduction**.
Select **ON.**
Set **moiré reduction** to 50%.
Press middle switch to set.
Exit **Screen** menu.
Exit **Screen manager** menu.

25.2.3 - EIZO FlexScan T62A and T63S

The GRAPH changes and software change in V1.5.x should only affect the contrast and brightness level. Thus, these controls are adjusted in this procedure. The color balance and other settings should be as before.

- Enter the *Color* Menu.
- Set *Sub Contrast* (black half moon) to 100%.
- *Save* and exit this menu.
- Enter the *Screen* Menu.
- Adjust *Contrast* to somewhere between 80 and 100%, depending on desired intensity level.
- With all TGC pot's to minimum, adjust *Brightness* so that the sector edge is just visible.
- Exit

SYSTEM FIVE Replacement Procedures

Overview

Introduction

This part of the Service Manual holds the Replacement Procedures
for SYSTEM FIVE .

Table of Contents

The table gives you an overview for this part of the Service Manual:

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AC Power Replacement Procedure - rev. 01	L1-3
DC Power Replacement Procedure - rev. 01	L1-5
External I/O Replacement Procedure - rev. 01	L1-7
Fan Replacement Procedure - rev. 01	L1-9
Front Panel Assembly Replacement Procedure - rev. 01	L1-11
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Internal I/O Replacement Proc. - rev. 01	L1-15
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Patient I/O Replacement Procedure - rev. 01	L1-19
Relay Board Assembly Replacement Procedure – rev. 03	L1-21
Temperature Sense Board Replacement Procedure - rev. 01	L1-23

Macintosh HD:User James:@i-art:Service:S5_ServiceMan:S5_serv_files:L1-01-hmh.02.
Printed: December 5, 2000.

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AC Power Replacement Procedure

1 Introduction

1.1 Abstract

This procedure describes how to replace the AC Power Supply assembly.

1.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_02_ac_power.
Printed: December 5, 2000.

2 Tool requirements

- Phillips screwdriver, size 2.
- Flat screwdriver, any size.

3 Description

The AC Power supply is located in the back of the system, on the right side viewed from the rear. In order to replace it, the lower rear cover must be removed.

1. Disconnect the mains connector from the wall outlet.
2. From the back of the system, unscrew the 4 screws holding the lower side panels and the lower rear panel.
3. Also unscrew the 4 screws holding the upper side panels and the upper rear cover. Remove all covers.
4. Pull both lower side panels slightly out sidewards. It’s not necessary to fully remove them.
5. Unscrew the 3 screws holding the bottom part of the rear cover.
6. Disconnect all cables from the External I/O panel.
7. Pull the rear cover straight out.
8. Unscrew the one screw on the bottom of the AC power, and remove the AC power cover by lifting the cover out and up.

9. Press a flat screwdriver underneath the flange on the lower part of the AC power, and loosen it.
10. Disconnect the power cables plugging into the top connectors on the power. Pay attention to where the connectors are plugged in.
11. Lift the AC power partly out, and disconnect the power connectors and the two D-connectors. Then lift the AC power fully out.
12. Install the new AC power supply partly, and connect the power cables and the two D-connectors. Then install it fully paying attention to the hooks on the bottom of the supply fitting the slots in the frame.
13. Install the AC power cover, and mount the AC power with one screw (the left one).
14. Mount the upper rear cover, then the lower rear cover and finally the side panels. Before pushing the lower rear cover all the way in, make sure the power cable to the DC power is properly secured.
15. Connect the mains cable to the wall outlet.

DC Power Replacement Procedure

4 Introduction

4.1 Abstract

This procedure describes how to replace the DC Power Supply module.

4.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document

Macintosh HD:User:James:@:arb:Service:S5_ServiceMan:S5_serv_files:L1_03_dc_power.
Printed: December 5, 2000.

5 Tool requirements

- Phillips screwdriver, size 2.
- Flat screwdriver, any size.
- Allen wrench (umbraco/hex screw wrench), size 5 mm.

6 Description

The DC Power supply is located in the back of the system, on the left side viewed from the rear. In order to replace it, the lower rear cover must be removed.

1. Turn off the power switch on the rear panel.
2. From the back of the system, unscrew the 4 screws holding the lower side panels and the lower rear panel.
3. Pull both side panels slightly out sidewards. It’s not necessary to fully remove them.
4. Unscrew the 3 screws holding the bottom part of the rear cover.
5. Disconnect all cables from the External I/O panel.
6. Pull the rear cover straight out.
7. Unscrew the two allen screws holding the +5V power terminals to the current rails on the rack.
8. Disconnect the AC power cable plugged into the DC power supply.

9. Press the flat screwdriver underneath the flange on the lower part of the DC power supply, and loosen it.
10. The power supply can now be lifted out and replaced.
11. Install the new power supply. Pay special attention to hooks on the bottom of the power supply fitting the slots in the frame. Align the connectors and push until the angled bracket is flush with the frame.
12. Screw the +5V terminals into the current rails.
13. Connect the AC power plug.
14. Mount the rear cover. The top part of the cover should slide into the slot in the plate between the DC power and the AC power. Before pushing it all the way in, make sure the power cable to the DC power is properly secured.
15. Mount the side covers.
16. Turn on the power switch.

External I/O Replacement Procedure

7 Introduction

7.1 Abstract

This procedure describes how to replace the External I/O subassemby.

7.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_04_ext_io.
Printed: December 5, 2000.

8 Tool requirements

- Phillips screwdriver, size 2.

9 Description

The External I/O subassembly is located on the left side of the system, in the rear. In order to replace it, the lower rear cover must be removed.

1. From the back of the system, unscrew the 4 screws holding the lower side panels and the lower rear panel.
2. Pull both lower side panels slightly out sidewards.
3. Unscrew the 3 screws holding the bottom part of the rear cover.
4. Disconnect all cables from the External I/O panel.
5. Pull the rear cover straight out.
6. Unscrew the three countersunk screws holding the External I/O subassy to the vertical frame bar. The assembly is now loose.
7. Pull the subassy out towards the back, and lift it away from the system.
8. Install the new External I/O subassembly by pushing it into the Internal I/O connectors.
9. Mount it with the three countersunk screws.

10. Mount the rear cover. The top part of the cover should slide into the slot in the plate between the DC power and the AC power. Before pushing it all the way in, make sure the power cable to the DC power is properly secured.
11. Connect all cables to the External I/O panel.
12. Mount the lower side panels.

Fan Replacement Procedure

10 Introduction

10.1 Abstract

This procedure describes how to replace fans.

10.2 Document History

Rev.	Date	Sign.	Description
01	28 Apr. 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_05_fan.
Printed: December 5, 2000.

11 Tool requirements

- Phillips screwdriver, size 2.

12 Description

The fans are located in the bottom of the system.

1. Turn the system mains power off with the circuit breaker in the rear.
2. Loosen the 3 screws holding the air filter cover. This cover is located on the right lower side below the lower side panel.
3. Remove the cover.
4. Pull out the air filter. You have now full access to the fans from underneath the system.
5. Replace the bad fan(s).

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Front Panel Assembly Replacement Procedure

13 Introduction

13.1 Abstract

This procedure describes how to replace the Front Panel Assembly.

13.2 Document History

Rev.	Date	Sign.	Description
01	18 April 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_06_fp_assy.
Printed: December 5, 2000.

14 Tool requirements

- Phillips screwdriver, size 2.
- Flat screwdriver, size 2.
- Adjustable wrench.

15 Description, Front Panel replacement

1. Unscrew the two screws holding the upper left side panel.
2. Disconnect the audio cable (phono jacks) to the front panel.
3. Loosen and partly unscrew the two M4 screws in each (diagonal) corner up underneath the front panel console (front right side and rear left side). It is not necessary to unscrew any of the other screws.
4. Push the two screws to lift the panel up, then put something between the keyboard and the console to hold it up before fully unscrewing the two screws.
5. Lift the front panel slightly up in the front. Disconnect the cable between the QWERTY keyboard and the main board. Note that the front panel is hinged on top, by two angles fitting two slots in the frame.
6. Pull the front panel carefully and slightly out also in the top. Turn it on the edge and let it rest on the metal compartment. Disconnect the ribbon cables and the power cables before lifting it fully out.

7. Replace the whole front panel assembly or parts of the assembly, depending on nature of problem. See exploded view drawing for the front panel in the Mechanical Assemblies chapter. Remember to connect the ribbon cables cables and power cables.
8. When installing the keyboard, first insert the top hinges into the slot, then carefully lower the front part down. On the first systems, pay special attention to the interconnection between the QWERTY keyboard and the front panel keyboard. A guide pin should ensure that the connectors mate properly. On newer systems, connect cable between QWERTY keyboard and main board.
9. Connect the audio cable.
10. Mount the front panel with the two screws from underneath.
11. Install the side panel.
12. In order to test the new front panel, see Front Panel Test Procedure in the Troubleshooting Guide.

16 Description, QWERTY keyboard replacement

1. Unscrew the four M4 screws holding the QWERTY keyboard up underneath the front panel assembly.
2. Pull the assembly straight down. Note that on the first systems this assembly plugs into the front panel main board. On the later systems, there is a cable between the QWERTY assembly and the main board.
3. Replace the QWERTY keyboard assembly. Remember to connect the cable / make sure the connectors mate properly (on first systems).
4. Mount the new QWERTY keyboard assembly with the four M4 screws.
5. In order to test the new QWERTY keyboard, see Front Panel Test Procedure in the Troubleshooting Guide.

Hard Disk Replacement Procedure

17 Introduction

17.1 Abstract

This procedure describes how to replace the harddisk.

17.2 Document History

Rev.	Date	Sign.	Description
01	17 April 1995	GRL	First version of document
02	2 October 1996	LHS	Included x-ref to section N - “Software Overview”
03	Nov.2000	JB	Added Hard Disk handling Warning

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_07_hd.03.
Printed: December 5, 2000.

18 Tool requirements

- Phillips screwdriver, size 2.
- Flat screwdriver, size 2.

19 Description

1. Unscrew the two screws holding the lower left side panel. Remove the panel to get to the lower peripheral compartment.
2. Loosen the screws holding the bracket around the harddisk.
3. Disconnect the SCSI cable and power cable from the harddisk.
4. Replace the harddisk.
5. Connect the cables, tighten the cover and mount the side plate.

For configuration of the hard disk, see Software Overview on page *N-1*.

Warning: Handle Hard Disk with Care!!!

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Internal I/O Replacement Proc.

20 Introduction

20.1 Abstract

This procedure describes how to replace the Internal I/O subassembly.

20.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document

21 Tool requirements

- Phillips screwdriver, size 2.

22 Description

The Internal I/O subassembly is located on the left side of the system, in the rear, inside the peripherals compartment. In order to replace it, the left side cover must be removed.

1. From the back of the system, unscrew the 2 screws holding the left lower side panel.
2. Remove the side cover.
3. Disconnect all cables from the Internal I/O panel. Pay attention to where they were mounted in case labelling is unclear.
4. Unscrew the three panhead phillips screws holding the Internal I/O subassy to the vertical frame bar. The assembly is now loose in the sense that it is connected to both the motherboard and the External I/O subassembly via connectors.
5. Pull the subassy slightly forward to get it clear the External I/O connectors. Then pull it straight out of the motherboard.
6. Install the new Internal I/O subassembly by first pushing it into the motherboard, then into the External I/O connectors.
7. Mount it with the three panhead screws.
8. Connect all cables. See Internal Wiring Diagram if uncertain where to connect.
9. Mount the left lower side panel.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_08_int_io.
Printed: December 5, 2000.

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Monitor Replacement Procedure

23 Introduction

23.1 Abstract

This procedure describes how to replace the monitor.

23.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document
02	November 2000	JB	Edited one description and wrote another

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_09_monitor_assy_01.
Printed: December 5, 2000.

24 Tool requirements

- Phillips screwdriver, size 2.
- 7mm ring spanner
- 8mm ring or jaw spanner

25 Description (Older Systems)

1. From the back of the system, unscrew the 2 screws on the top attaching the small rear top cover.
2. Unscrew the 4 countersunk screws holding the monitor mounting plate to the top of the fram.
3. Disconnect the cables to the monitor.
4. Pull the mounting plate (incl. the monitor/pedestal) backwards until you can lift the whole assembly off the top of the system.
5. Replace the monitor.
6. Install the assembly in the opposite sequence.

26 Description (newer Systems)

1. At the rear of the monitor, unscrew the 2 screws at each side of the cover protecting the Power and Signal cable connections .
2. Disconnect the Power and Signal cables from the monitor.
3. Disconnect the GN/YE ground wire using the 7mm Allen wrench.
4. Unscrew the Monitor fastening screw with the 8mm Allen wrench
5. Pull the Monitor backwards to free it from the pedestal
6. Replace the new monitor by placing it onto the Pedestal and pushing it forwards and into it . If Using other than factory replacement Monitors a metal mounting plate found under the old Monitor will have to be dismounted from it and mounted onto the new Monitor

Install the assembly in the opposite sequence.

Patient I/O Replacement Procedure

27 Introduction

27.1 Abstract

This procedure describes how to replace the Patient I/O assembly.

27.2 Document History

Rev.	Date	Sign.	Description
01	17 April 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_10_pat_io.
Printed: December 5, 2000.

28 Tool requirements

- Phillips screwdriver, size 2.

29 Description

1. Unscrew the four screws holding the lower side panels.
2. Remove the side panels and the lower front plate.
3. From inside the lower peripheral compartment, loosen the two screws holding the Patient I/O box.
4. Disconnect the cable from the Int I/O board.
5. Pull the Patient I/O box out through the front of the system, and replace it.
6. Insert the new box through the front, mount the screws and connect the cable.
7. Install the panels.

Empty page.

Relay Board Assembly Replacement Procedure

30 Introduction

30.1 Abstract

This procedure describes how to replace the Relay Board subassembly, i.e. the assembly with the probe connectors.

30.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document
02	27 Feb 96	GRL	Updated due to EMC fixes (with Burndy shield box).
03	9 Feb 98	GRL	Updated due to changes .

Macintosh HD:User:James:@:arb:Service:S5_ServiceMan:S5_serv_files:L1_11_rly_assy03.
Printed: December 5, 2000.

31 Tool requirements

- Phillips screwdriver, size 2.
- Flat screwdriver, size 2.
- Adjustable wrench.

32 Description

From January 1. 96 all systems have been shipped with RLY board with EMC-fixes. These boards have a shield box around the APAT Burndy connectors. This box makes it awquard to disassemble the RLY board from the card rack.
The points which are specific to boards with EMC fixes are labelled EMC.

The Relay Board subassembly is located in the front side of the system, on the right side. In order to replace it, the lower front cover must be removed.

1. From the back of the system, unscrew the screws holding the lower and upper side panels.
2. Remove the side covers.
3. Disconnect all cables from the probe connector panel.
4. Pull the front cover straight forward.

5. Unscrew the shield plate in front of the boards.
6. Unscrew the M3-screws (12) holding each 260 pin connector (except 2 on the left spare/parking connector, upper right and lower left).
7. EMC: Unscrew the M3-screws through the APAT connectors.
8. Unscrew the M4 phillips panhead screws attaching the front plate to the frame.
9. Unscrew the nuts on the Doppler (and Catheter if mounted) connector.
10. Disconnect the two XDBUS boards between RLY/TX/RX/PRC.
11. EMC: Unscrew the screws holding the small IV&DP connector board onto the RLY board.
12. The RLY assembly is now only connected to the motherboard. In order to loosen it, slide the whole assembly out of the MBD connector to the right. Then, when it's loose, slide it out leftward.
13. EMC: Install the IV&DP connector board.
14. Install the new Relay Board subassembly in the opposite sequence. Mount the upper connector (IV/DP first, then position the lower RLY board connector).
15. Connect the two XDBUS boards between RLY/TX/RX/PRC.
16. First screw the M3 screws into the 260 pin connectors. (For noise purposes, it is very important that these screws are mounted). Then screw the M4 screws and mount the connector nuts.
17. Install the front cover, then the side covers.
18. Reconnect all cables to the connectors.
19. Good job, you deserve a cup of coffee.

Temperature Sense Board Replacement Procedure

33 Introduction

33.1 Abstract

This procedure describes how to replace the Temperature Sense board controlling the fan speed (it has nothing to do with the TE probe temperature reading).

33.2 Document History

Rev.	Date	Sign.	Description
01	6 April 95	GRL	First version of document

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:L1_12_temp_sense.
Printed: December 5, 2000.

34 Tool requirements

- Phillips screwdriver, size 1.

35 Description

The Tempsense board is located above the CPU and MEMORY boards, mounted up underneath the peripheral plate.

1. Unscrew the two screws holding the right side panel and remove it.
2. Disconnect the cable plugging into the Tempsense board.
3. Unscrew the two screws holding the board to the peripheral plate. To get to the inner screw you might have to pull out the CPU and the MEMORY boards (which are screwed in place).
4. Replace the Tempsense board and attach in the opposite sequence.

Your Notes:

Board Assembly Drawings

Overview

Introduction

This part of the Service Manual gives you the Board Assembly Drawings for some of the boards in SYSTEM FIVE.

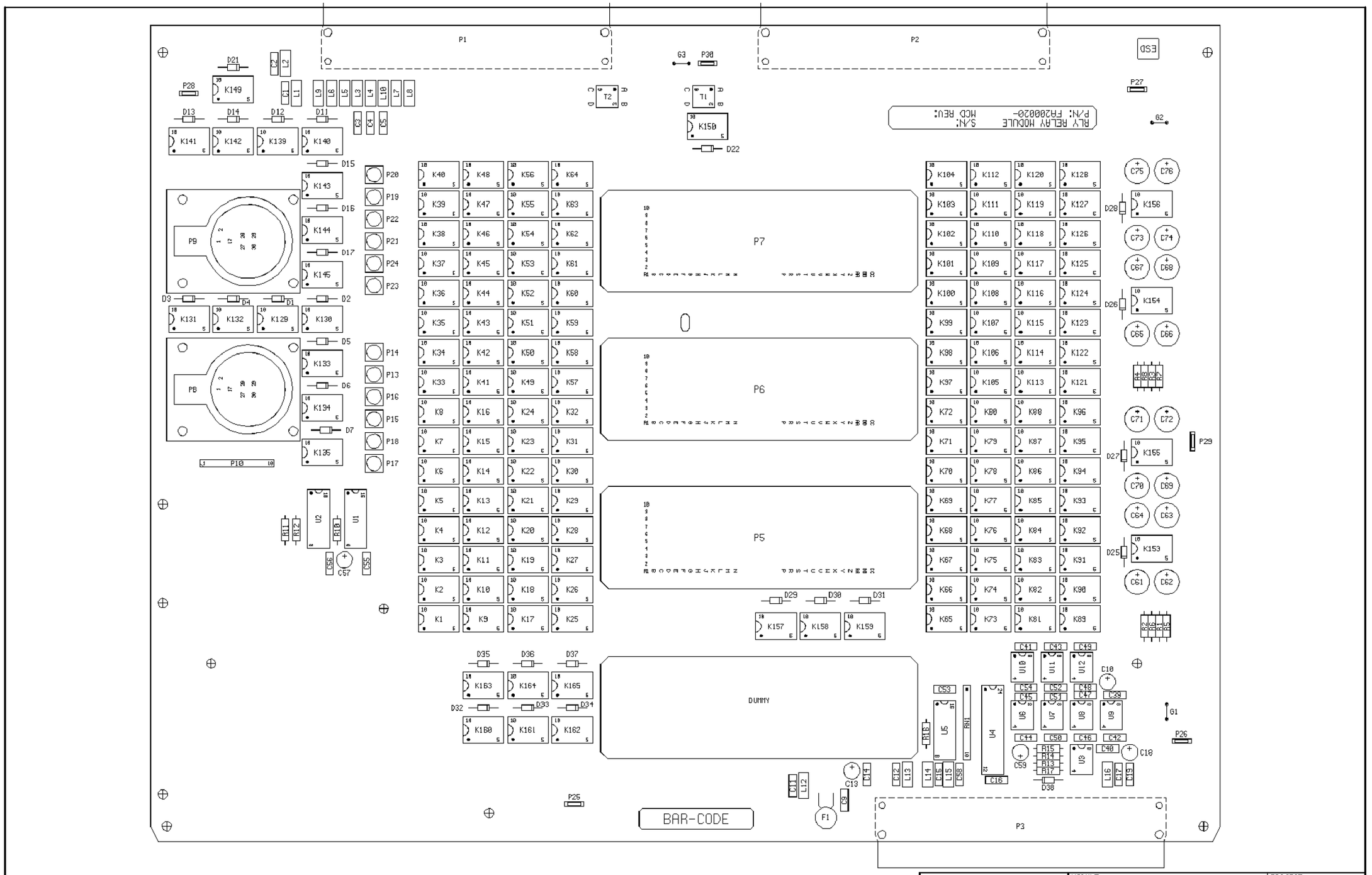
Table of Contents

The table gives you an overview for this part of the Service Manual:

Contents	Page
Relay Module — Component Side	M-2
Probe Controller — Component Side	M-3
Probe Controller — Solder Side	M-4
Internal I/O — Component Side - rev. E	M-5
Internal I/O — Solder Side - rev. B	M-6
External I/O — Component Side	M-7
AC Controller — Component Side	M-8
High Voltage (HV) Supply — Component Side	M-9
High Voltage (HV) Supply — Solder Side	M-10

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:M_01_Innh.
Printed: December 5, 2000.

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:M_02_Relay.01.
Printed: December 5, 2000.



Note 1

The revision marked on the label has to be the MODULE REV.
Ref. MCD.

Note 2

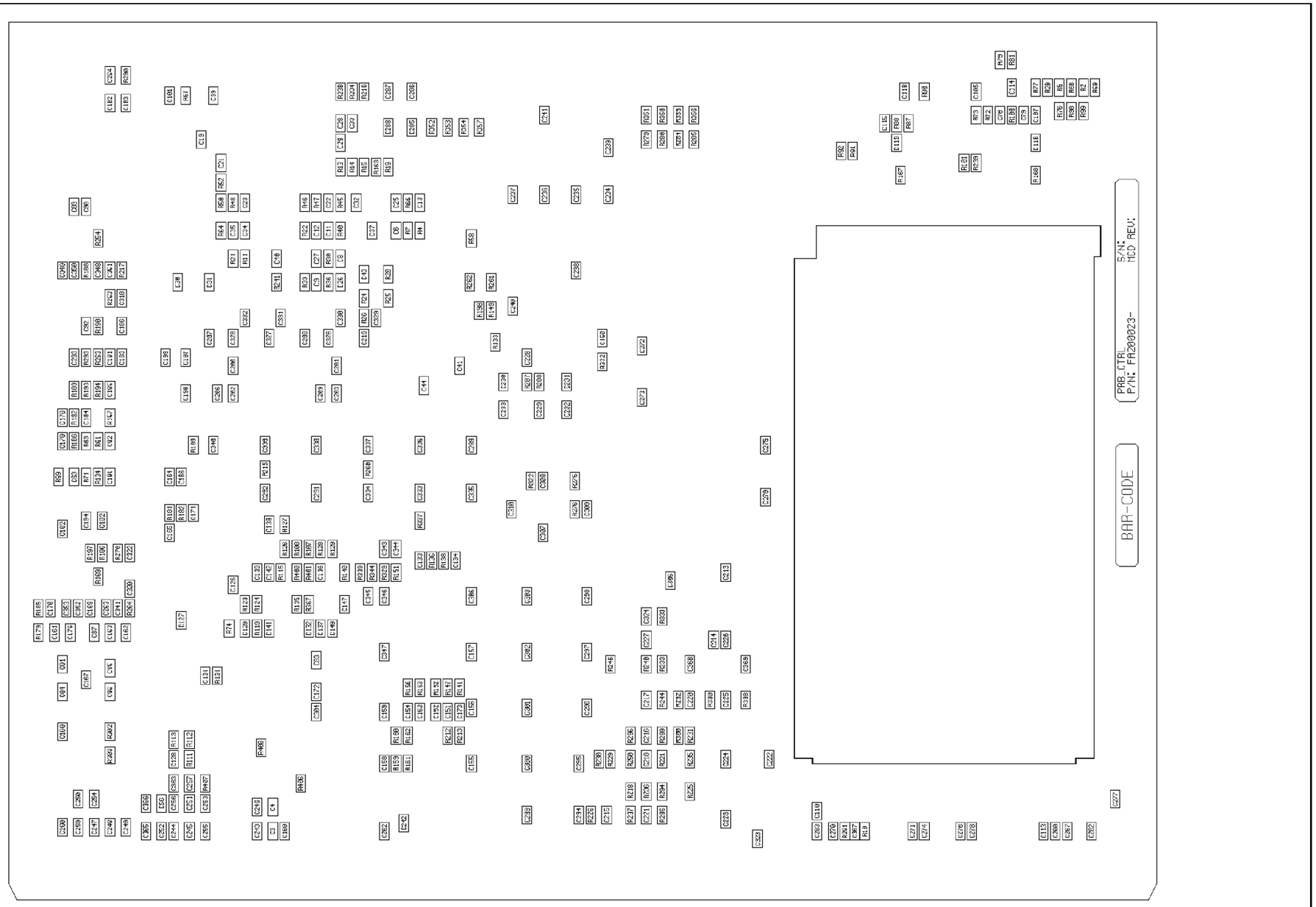
P1 - P3 and P13 - P24 are mounted on solder side.

VINGMED SOUND			MODULE: RLY RELAY MODULE	PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 12.sep.95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION
CHECKED: WL	DATE	SIGN	PART NO: 330 FA200020	REV: B
APPROVED: HH	DATE	SIGN		
SCALE: 1.2	FILE: j4510.re		SHEET: 1 OF 1	

Macintosh HD:User:James:@i-ab:Service:S5_Service:Service:S5_ServiceMan:S5_serv_files:M_03_Probe_C_1.01.
Printed: December 5, 2000.

VINGMED SOUND			MODULE: PROBE CONTROLLER		PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 21. aug. 95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION	
CHECKED: GRL	DATE	SIGN	PART NO: 330 FA200023		REV: 03
APPROVED: HH	DATE	SIGN			
SCALE: 1.2	FILE: u22\cad\pcad\x\fa\j4515.rc				SHEET: 1 OF 2

Macintosh HD:User-James:@i-arb:Service:S5_Service\Man:S5_serv_files:M_04_Probe_C_2.01.
Printed: December 5, 2000.

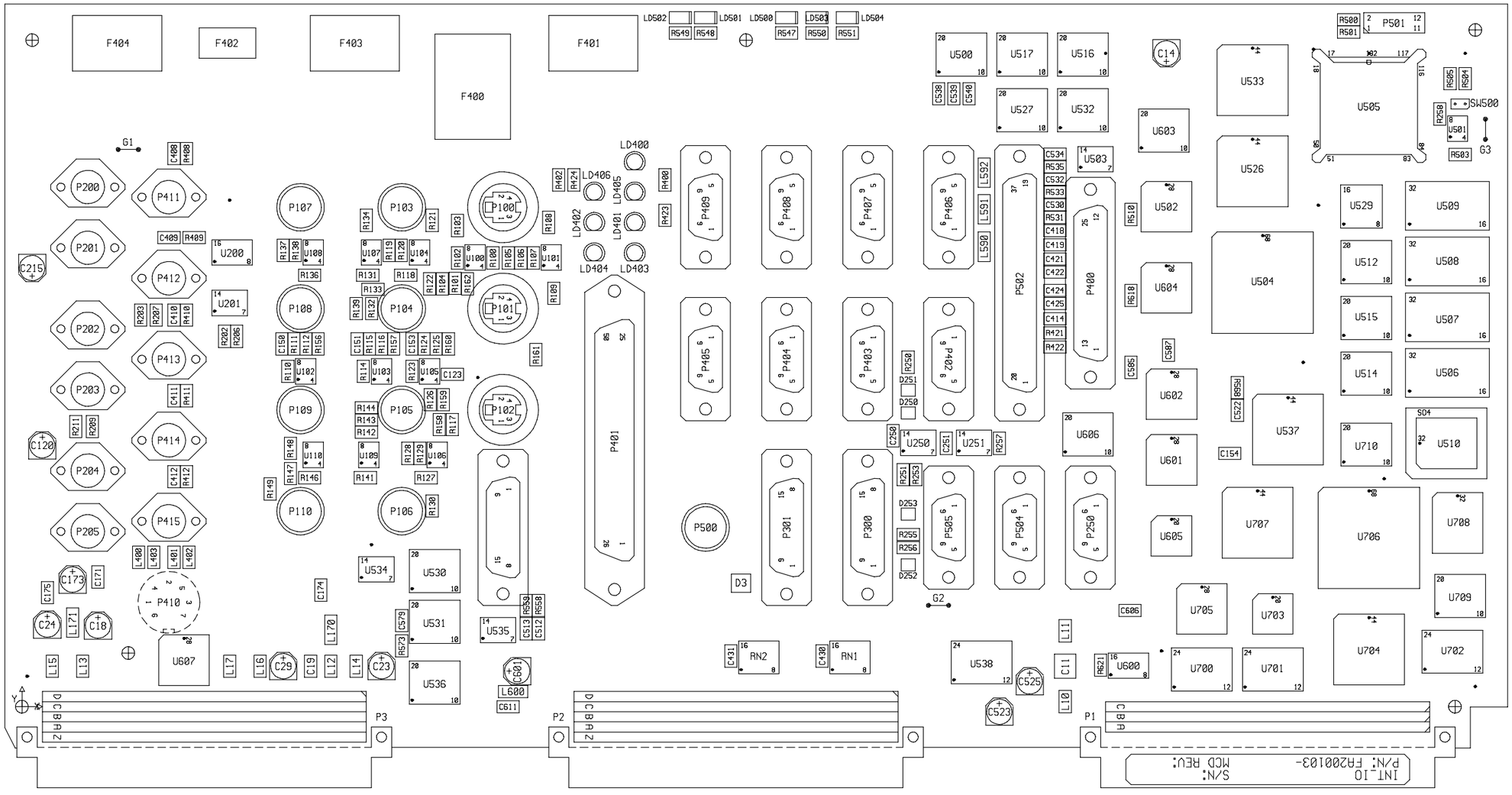


Note!

The revision marked on the label
has to be the MODULE REV.
Ref. MCD.

VINGMED SOUND			MODULE: PROBE CONTROLLER		PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 21.aug.95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION	
CHECKED: GAL	DATE	SIGN	PART NO: 330 FA200023		REV: 03
APPROVED: HK	DATE	SIGN			
SCALE: 1.2	FILE: u22\cad\pcad\x\fa\j4515.rc				SHEET: 2 OF 2

Macintosh HD:User:James:@i-art:Service:S5_ServiceMan:S5_serv_files:M_05_Int_1.02.
Printed: December 5, 2000.



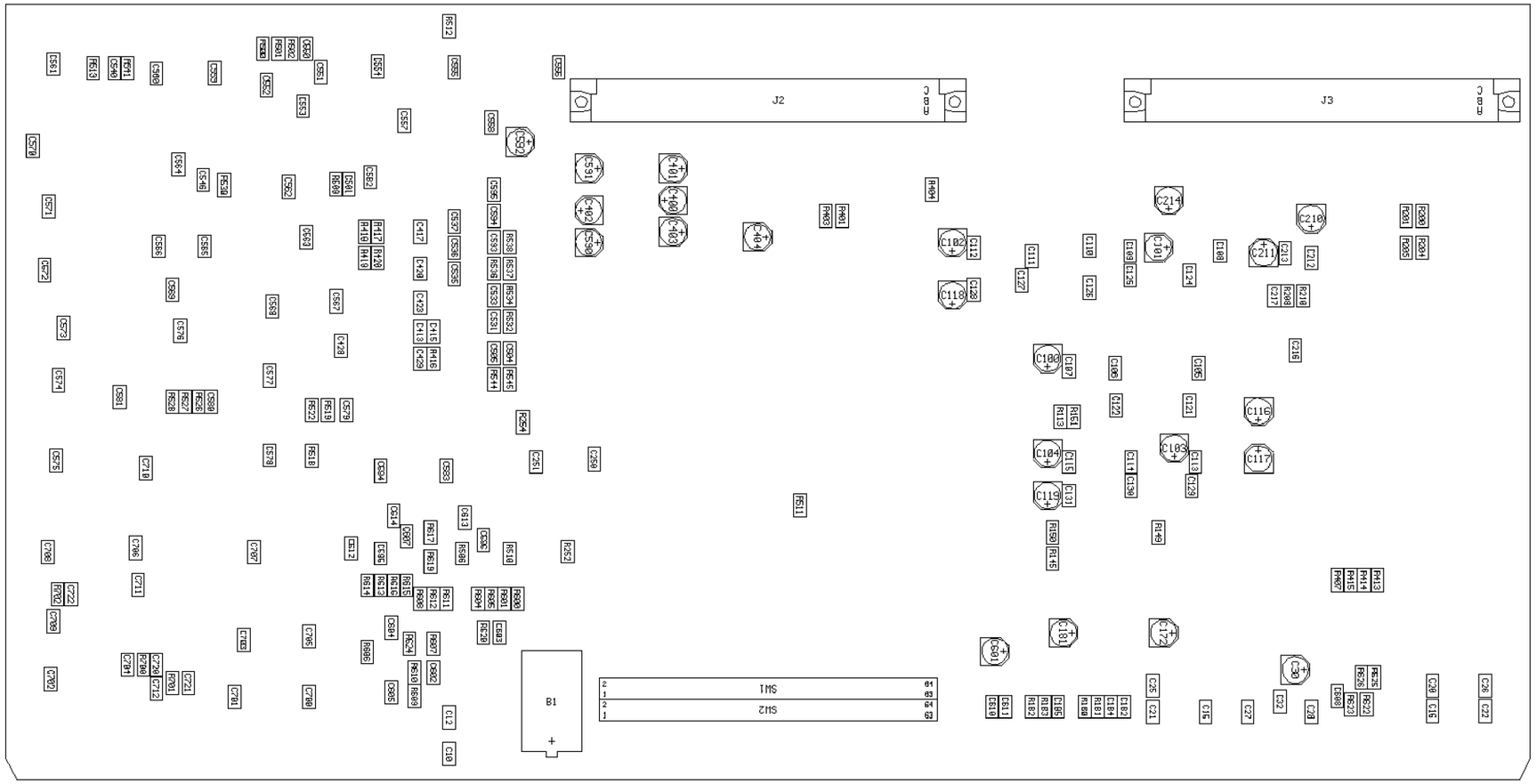
Note!

The revision marked on the label has to be the MODULE REV.
Ref. MCD.

Mounting instructions:

Orientation of P103-P110 and P500 as shown.

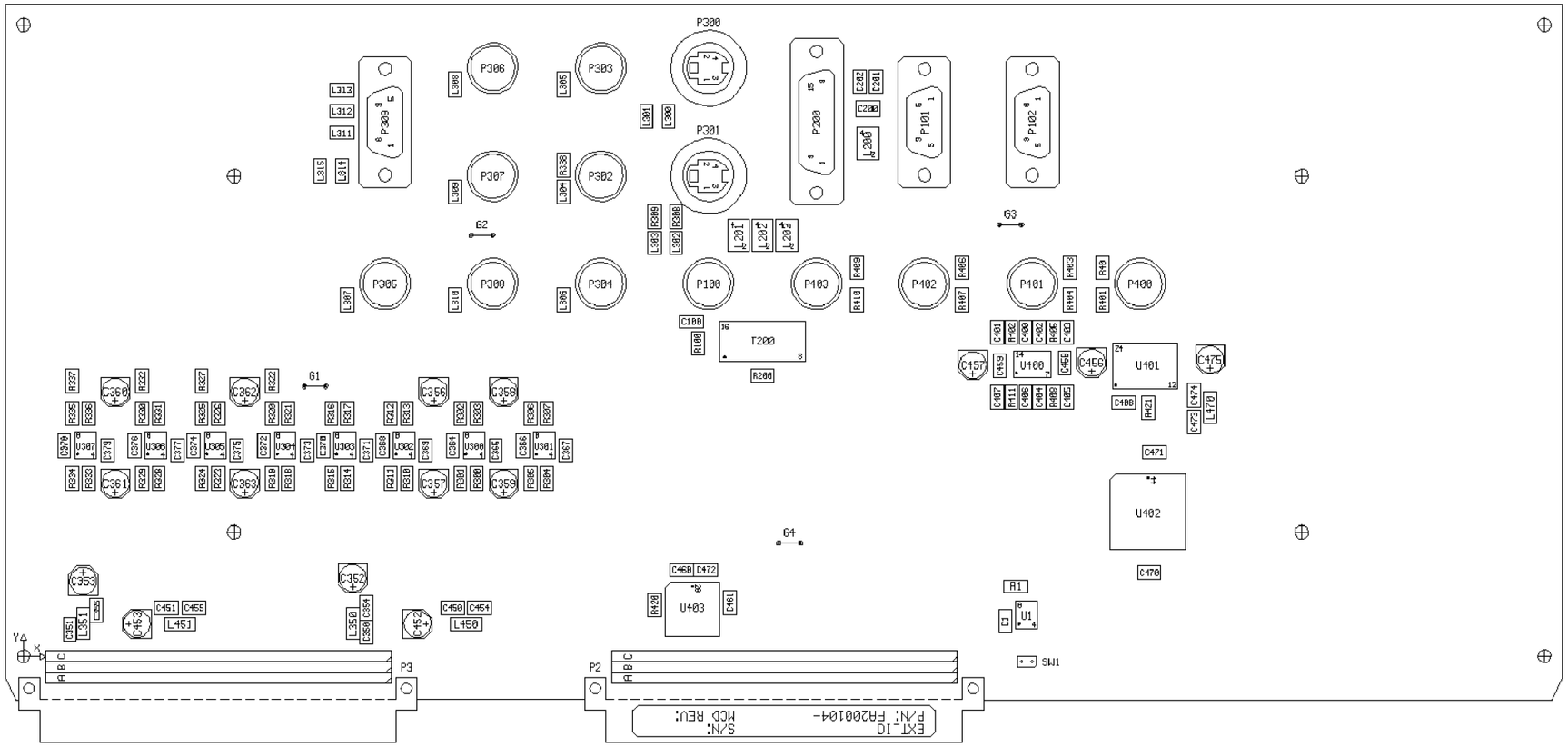
VINGMED SOUND			MODULE: INT_IO	PROJECT: SYSTEM 5
DESIGNER: IR	DATE: 21.Feb.97	SIGN:	TYPE OF DOC: ASSEMBLY	CLASSIFICATION:
CHECKED: GJ	DATE:	SIGN:	PART NO: FA200103	REV: E
APPROVED: KB	DATE:	SIGN:		
SCALE: 1.5	FILE: j4520.re			SHEET: 1 OF 2



VINGMED SOUND			MODULE: INT_IO	PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 11.sep.95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION
CHECKED: GJ	DATE	SIGN	PART NO: 330 FA200103	REV: B
APPROVED: KB	DATE	SIGN		
SCALE: 1.5	FILE: j4520.rc			SHEET: 2 OF 2

Macintosh HD:User:James:@i-arb:Service:S5_Service:Man:S5_serv_files:M_06_Int_2.01.
Printed: December 5, 2000.

Macintosh HD:User James:@i-arb:Service:S5_service:Man:S5_serv_files:M_07_Ext01.
Printed: December 5, 2000.

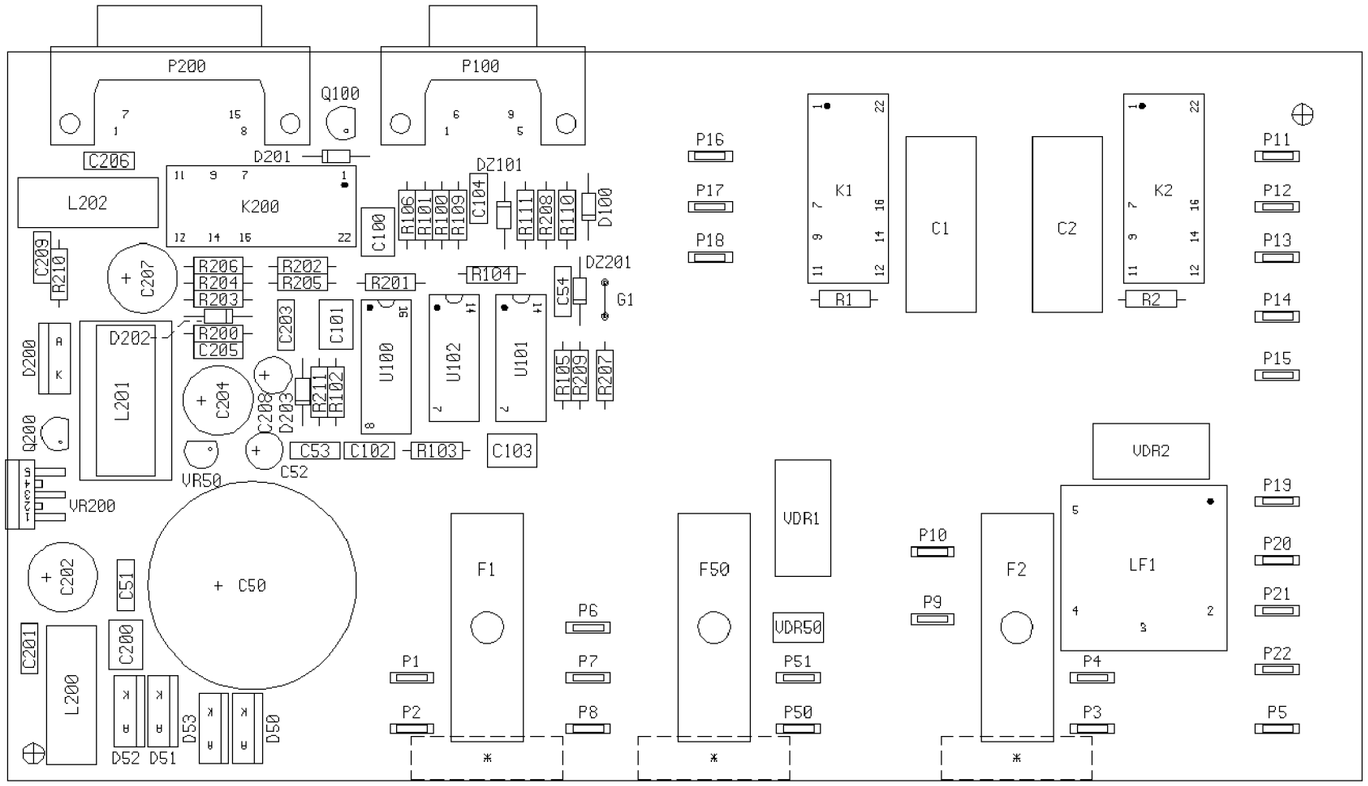


Note!

The revision marked on the label has to be the MODULE REV.
Ref. MCD.

VINGMED SOUND			MODULE EXT_IO		PROJECT SYSTEM 5
DESIGNER EI	DATE 11.sep.95	SIGN	TYPE OF DOC ASSEMBLY	CLASSIFICATION	
CHECKED GJ	DATE	SIGN	PART NO 330 FA200104		REV A
APPROVED KB	DATE	SIGN			
SCALE 1.5	FILE j4521.rc			SHEET 1 OF 1	

Macintosh HD:User:James:@I-arb:Service:S5_Service:S5_serv_files:M_08_ACctrl.01.
Printed: December 5, 2000.

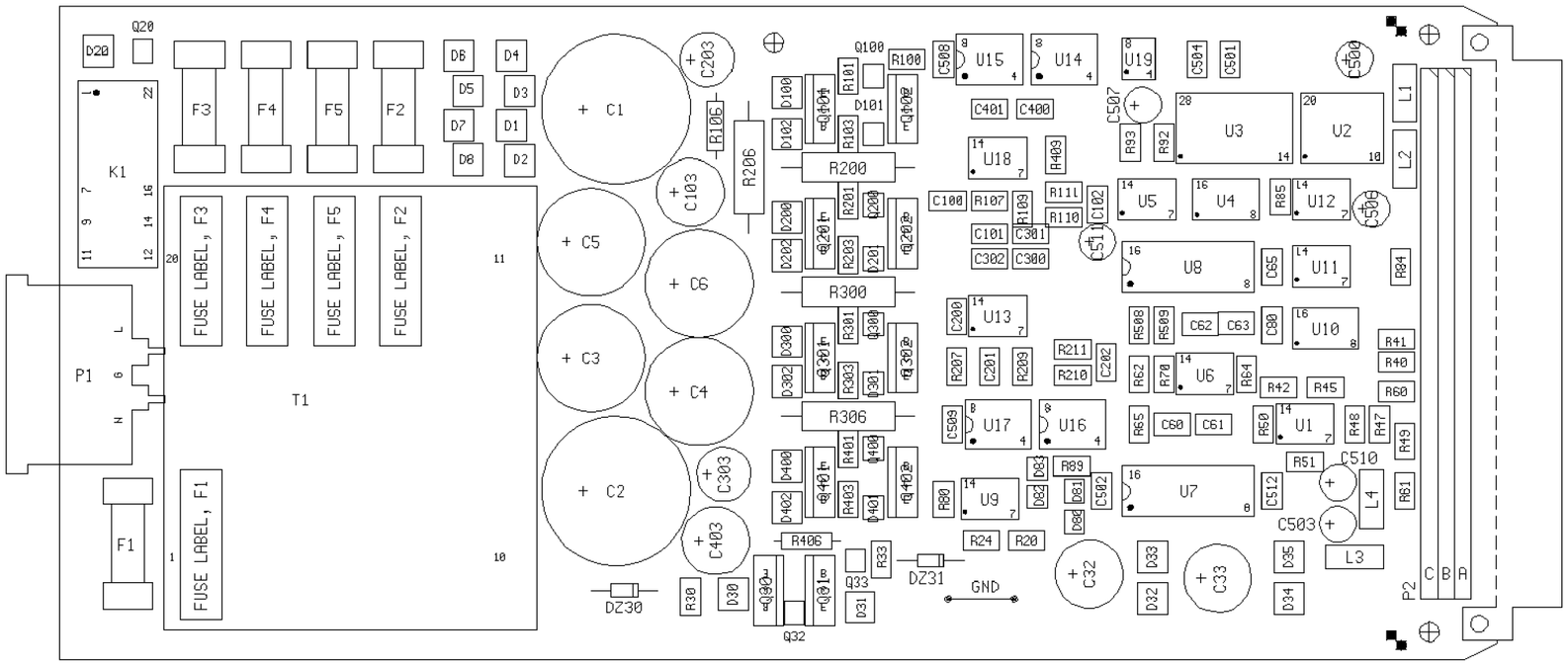


NOTE!

The revision marked on the label has to be the module rev. Ref. MCD.

* Custom specified fuse label.

VINGMED SOUND			MODULE ACCTRL		PROJECT SYSTEM 5
DESIGNER EI	DATE 15.nov.95	SIGN	TYPE OF DOC ASSEMBLY	CLASSIFICATION	
CHECKED GJ	DATE	SIGN	PART NO 330 FA200107		REV A
APPROVED KB	DATE	SIGN			
SCALE 1.5	FILE j4514.rd				SHEET 1 OF 1



NOTE!

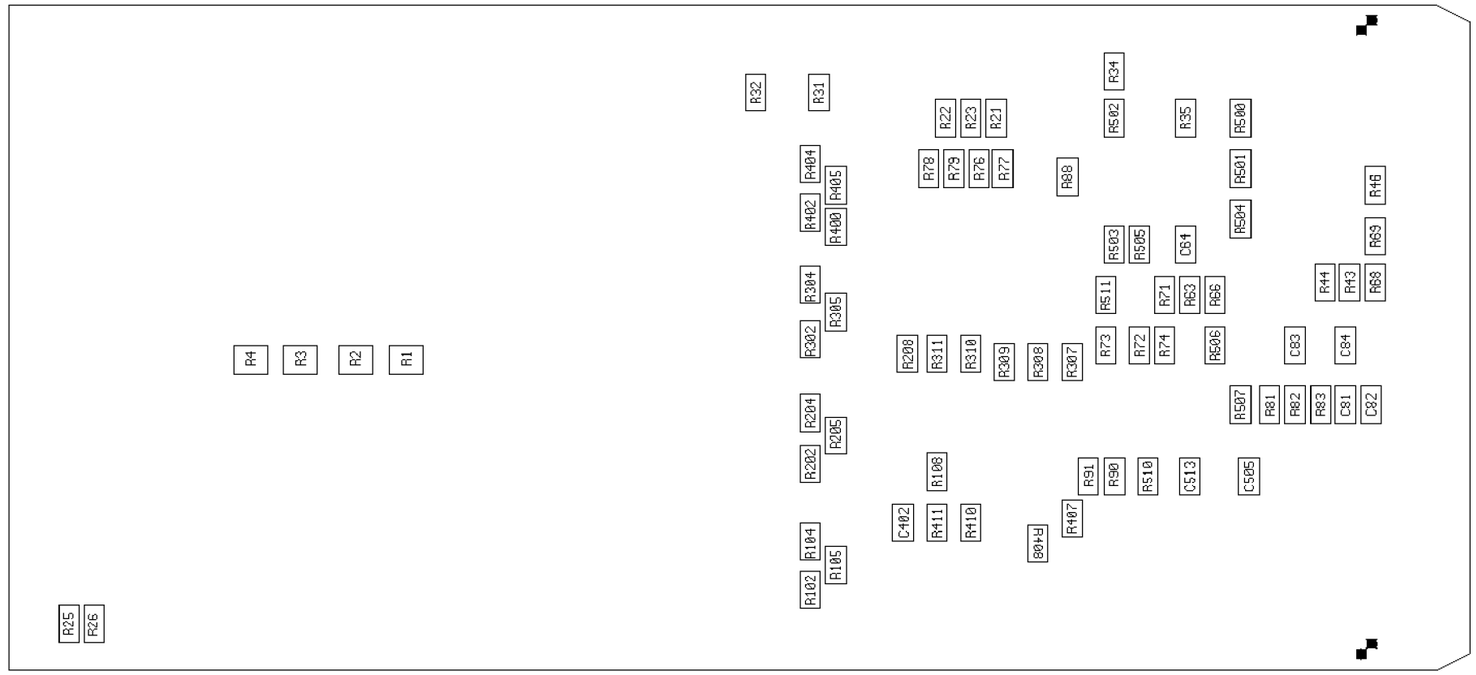
The revision marked on the label has to be the module rev. Ref. MCD.

Q30, Q31, Q101, Q201, Q301 and Q401 must be mounted on heatsink FA307113 before soldering.

* FUSE LABEL 1: Ref. FA314391
* FUSE LABEL 2: Ref. FA314392
* FUSE LABEL 3: Ref. FA314393
* FUSE LABEL 4: Ref. FA314394
* FUSE LABEL 5: Ref. FA314395

VINGMED SOUND			MODULE: HV SUPPLY	PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 20.mar.95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION:
CHECKED: GJ	DATE	SIGN	PART NO: 330 FA200063	REV: 04
APPROVED: KB	DATE	SIGN		
SCALE: 1.5	FILE: u4\pc\cad\pcad\x\fa\j4509.rb			SHEET: 1 OF 2

Macintosh HD:User:James:@i-ab:Service:SS_ServiceMan:SS_serv_files:M_09_HVs_1.01.
Printed: December 5, 2000.



VINGMED SOUND			MODULE: HV SUPPLY		PROJECT: SYSTEM 5
DESIGNER: EI	DATE: 20.mar.95	SIGN	TYPE OF DOC: ASSEMBLY	CLASSIFICATION	
CHECKED: GJ	DATE	SIGN	PART NO: 330 FA200063		REV: 04
APPROVED: KB	DATE	SIGN			
SCALE: 1.5	FILE: u4\pc\cad\pcad\x\fa\j4509.rb				SHEET: 2 OF 2

Macintosh HD:User:James:@i-arb:Service:SS_ServiceMan:SS_serv_files:M_10_HVs_2.01.
Printed: December 5, 2000.

Software Overview

Overview

Introduction

This part of the Service Manual gives you an overview of the software in SYSTEM FIVE.

Table of Contents

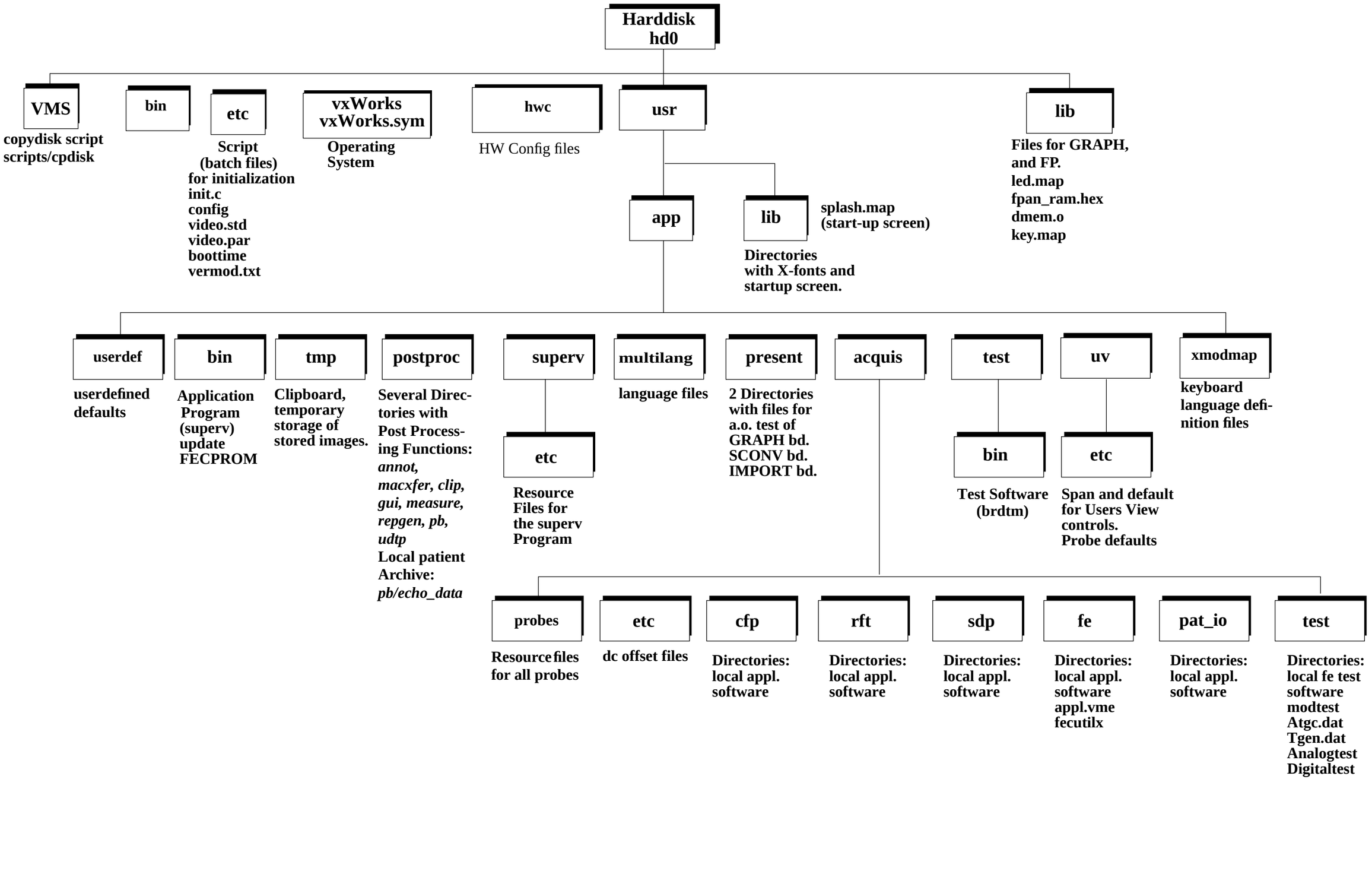
The table gives you an overview for this part of the Service Manual:

Contents	Page
Block Schematic, S5 Harddisk, sw v.1.5.x, v.1.6, v.1.7 & 1.7.1 - rev. 06	N-3
Block Schematic, System FiVe Harddisk, sw v.1.8 & v.1.9 - rev. 02	N-4
Software Upgrade Procedure – 01	N-5
System FiVe Software Upgrade to v.1.8	N-8
System FiVe Software Upgrade to v.1.9	N-25

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:N_01_Innh.05.
Printed: December 5, 2000.

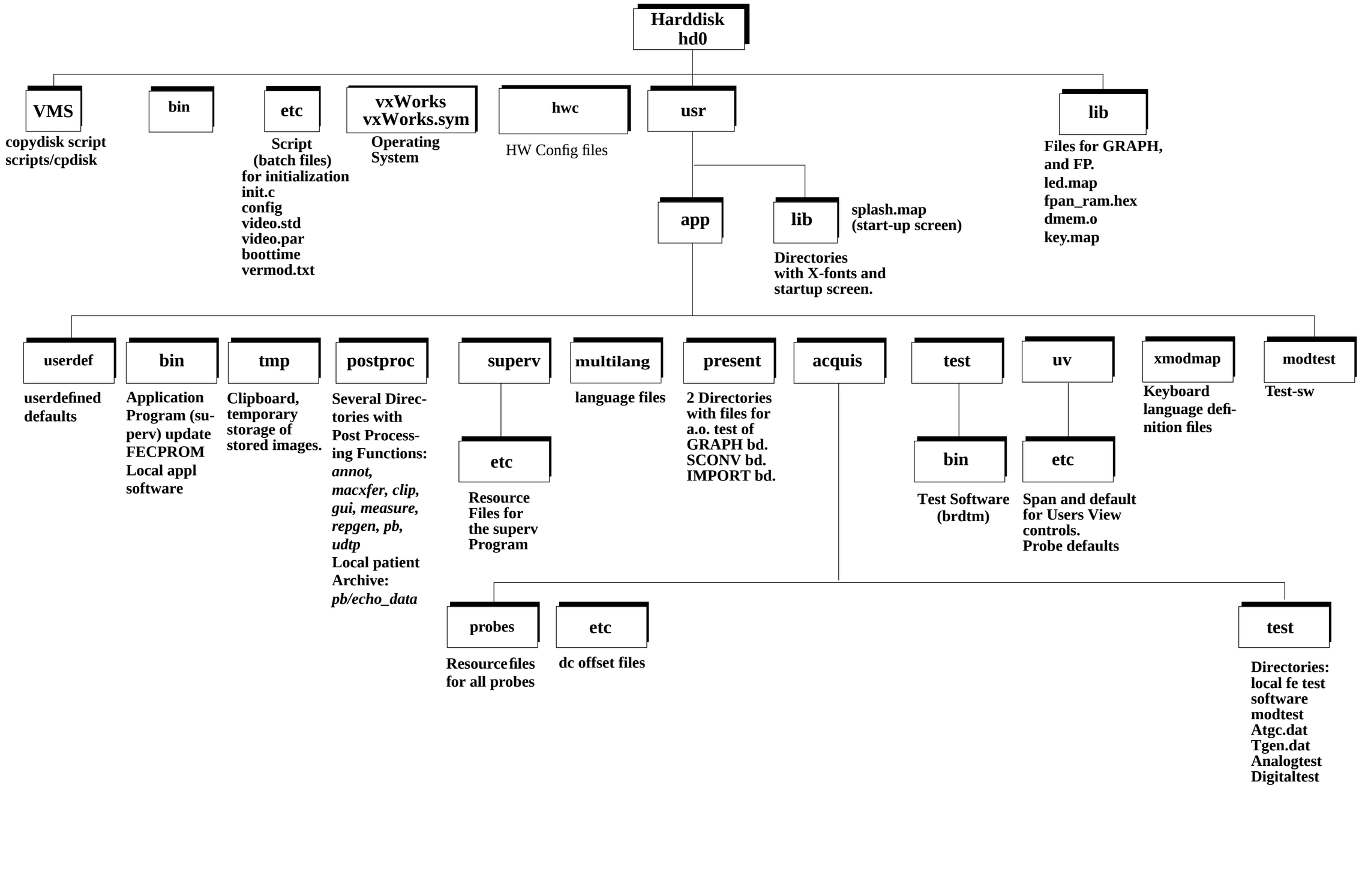
Your Notes:

Block Schematic, S5 Harddisk, sw v.1.5.x, v.1.6, v.1.7 & 1.7.1 - rev. 06



Macintosh HD:User:James:@-ath:Service:S5_ServiceMan:S5_serv_files:N_02_HD_bloc.06.
Printed: December 5, 2000.

2 Block Schematic, System FiVe Harddisk, sw v.1.8 & v.1.9 - rev. 02



Macintosh HD:User:James:@:ath:Service:SS_ServiceMan:SS_serv_files:N_021_HD_blkc.02.
Printed: December 5, 2000.

Software Upgrade Procedure

3 Introduction

3.1 Abstract

This document contains two procedures for copying the contents of one harddisk (master) onto a second harddisk (slave).

3.2 Parts Requirements:

- SCSI cable with two 40 pin flat cable connectors; one for the master disk and one for the slave.
- An extra power cable to connect from the INT I/O board to the slave harddisk.
- PC/terminal to connect to EXT I/O RS232-CPU port via a crossed RS232 serial cable.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:N_03_HD_copy:01.
Printed: December 5, 2000.

4 Copying from a masterdisk onto a disk with old software

(i.e. a software update):

1. The masterdisk must be configured with address 1 instead of 0. This is done by installing a jumper on the A0 address line on the disk. Position of this jumper varies from one manufacturer to another. (The slave disk already has address 0).
2. Turn the system on and let it boot until it is up and scanning in 2D. The system now boots from the old harddisk.
3. Push the Freeze button.
4. Press the return key on the PC/terminal to get the prompt >.
5. Enter *dosVolMount 1*. This is done to mount the master disk, hd1. If you want to ensure yourself that the disk is mounted, enter *devs*, and the system will print the disks which are mounted on the SCSI bus.
6. Enter *cd "/hd1/VMS/scripts"*. This command will move to the scripts directory on the master disk, hd1. Enter *ls* to list the files. Make sure that there is a file called *cpdisk* on this directory. Otherwise, copying will be impossible, and the process must be aborted.
7. Enter *diskInit ("/hd0")*. This is done to initialize the slave disk, hd0.

8. Enter <*cpdisk*. This will copy the contents of the masterdisk, hd1, onto the slave disk, hd0. This process takes a few minutes, and must not be interrupted.

Remove the masterdisk and the extra cables and boot the system with the slave disk.

5 Copying from a masterdisk onto a brand new disk:

1. The masterdisk must be configured with address 1 instead of 0. This is done by installing a jumper on the A0 address line on the disk. Position of this jumper varies from one manufacturer to another. (The slave disk must have address 0).
2. In order to boot from the master disk, hd1, the following must be done:
3. Turn the system on and interrupt the boot process from the terminal by pressing any key right after power-on.
4. Enter c to get into the CPU configuration menu.
5. Change the *boot device* from *scsi=0,0* to *scsi=1,0*
6. Press return 3 times until you come to *file name*. Change the file name from */hd0/vx040.st* to */hd1/vx040.st*
7. Press return a few times until you come to [VxWorks boot]: .
8. Turn the system on and let it boot until it is up and scanning in 2D. It will now boot from the master disk, hd1.
9. Push the Freeze button.
10. Press the return key on the PC/terminal to get the prompt >.
11. Enter *dosVolMake 0.* This is done to “format”, mount and initialize the new hd0 disk.
12. Enter *cd “VMS/scripts”*. This command will move to the scripts directory on the master disk, hd1. If you want to verify what’s on this directory, enter *ls* to list the files. A file called *cpdisk* should (must) be present on this directory. Otherwise, copying will be impossible, and the process must be aborted.
13. Enter <*cpdisk*. This will copy the contents of the masterdisk, hd1, onto the slave disk, hd0. This process takes a few minutes, and must not be interrupted.

6 Booting from the new disk:

After the copy process is finished and you wish to boot from the new disk, hd0:

- Remove the masterdisk and the extra cables and boot the system with the newly copied disk.
- Turn power on and interrupt the boot process.
- Enter c to get into the CPU configuration menu.
- Change the *boot device* from *scsi=1,0* to *scsi=0,0*
- Press return 3 times until you come to *file name*. Change the file name from */hd1/vx040.st* to */hd0/vx040.st*
- Press return a few times until you come to [VxWorks boot]: .
- Turn the system off and on and let it boot until it is up and scanning in 2D. It has now booted from the new disk, hd0.

System FiVe Software Upgrade to v.1.8

This document describes how to upgrade System FiVe's system software using an FTP procedure.

Section 1.0 - Effectivity

This prosedure may be used for updating all GE Vingmed System FiVe Ultra-sound units.

Section 2.0 - Purpose

This System FiVe Software Upgrade's sole purpose is for the installation of v.1.8 software.

Section 3.0 - Pre-requisite

The system software must be on v.1.7 level.

Section 4.0 - Related FMI's

None

Section 5.0 - Furnished Materials

BT'99 System FiVe Software Upgrade kit, GEVU P/N: FB200081, consists of the following:

ITEM #	GEVU PART NO.	DESCRIPTION	QTY	NOTE
1	FB200084	v1.8 CD, System SW	1	
2	512G4100	64 MB RAM	1	(Piggyback)
3	FA040050	Release Notes	1	
4	FB094038	BT '99 Upgrade Manual	1	(This manual)

Table 1: Furnished Materials

Section 6.0 - Introduction

6.1 Tools and Test Equipment

- Standard GE Vingmed Field Service Tool Kit, please see "Test Equipment and Tools Required" on page Intro-9 for details.
- Ethernet cable (crossed twisted pair) (GE part # 2244684)
- Optional direct hub connect cable.A non crossed twisted pair cable must be used.
- Optional direct hub connect with coax, 2 terminators (50 ohm) and 2 BNC-T adapters are required.
- Ethernet adapter 10 base – T, (GE part # 2195664)
- PC/Laptop with Ethernet card support.
- Ethernet card with PC Card Lan cable adapter for 10 Base-T and Coax
- Null modem cable (GE part # 2117638-3).

6.2 Software Requirements for PC/ Laptop

To install System FiVe software from PC/Laptop, the PC/Laptop must meet the following requirements:

1.) Operating system: Windows 95 or NT.

2.) Terminal Emulation software (e.g. Hyperterminal, setup: baudrate-9600, 8 bits-no parity – 1 stopbit).

3.) A FTP program that can function as a FTP Server. (Note :Chameleon FTP server software, can be downloaded from the GEMS Home Page.)

6.3 Compatibility vs. EchoPAC software

The System FiVe's system software v.1.8 is compatible with EchoPAC sw.6.2 and above.

Section 7.0 - Test and Verification Prior to Upgrade

1.) Run an automatic test prior to starting the upgrade. See "Performance Test (System Test) Procedure" on page K11-1 for detailed instructions. Correct any problems reported or observed before proceeding.

2.) Since there is currently no automatic way of saving and restoring setups and user defaults, the following manual procedure should be used. Please ensure the customer is aware of this!

Note: **All probe presets will be lost !**

3.) Press Setup on the keyboard, select each menu item in the setup menu and note down the specific details on a piece of paper.

4.) Press the Application menu and verify if there are specific user setups, make a note of them. (verify all available probes).

5.) Enter Setup menu on the Front Panel.

a.) In the menu that appears on screen, select System Test menu button.

b.) In the System Test menu, choose Module SW version.

c.) Write down the System Software Name listed in the Module Software Revisions List

	File name/ date	(System/options)
System FiVe :	_____	(_____)
Options :	_____	_____

Table 2: System Software Name listed in the Module Software Revisions List.

Note: **Membership and Advantage will need a password for all functions covered by the introducing offering on Advantage:**

Functions:

-
-
-
-
-
-

6.) Select the Applications menu when having the 2.5 FPA probe connected, The following software options must be verified and noted for:
   - RF,
   - Contrast,
   - TVI,
   - or any combination of these options.

Section 8.0 - Install Memory Upgrade

1.) Turn of the power (rear of system).
2.) Remove both the Upper and the Lower Covers on the left side.
3.) Un-screew the retaining screews used for fastening the System Processor Board and pull out the board.
4.) Un-screew the screews holding the RAM piggyback and remove the piggyback.
5.) Gently install the new memory piggy back and fasten it with the screewsthat were used for the old piggy back.
6.) Insert the Processor board in the board rack, in the same position it was before. Be sure that it is seated properly. Fasten the retaining screews.
7.) Turn on the power and boot the scanner.
8.) Verify that all the boards starts (the red LEDs are turned off) and that the system boots compleatly.
9.) Turn off the system and mount the panels you removed earlier.

Section 9.0 - Copy System FiVe Software from CD to PC

9.1 Create file structure on root directory (C:)

Note: **If the laptop has an Auto–sleep feature it needs to be turned off during this procedure. Make sure you have more than 20 MByte of free space on your harddisk.**

1.) On the windows desktop, open the My Computer icon (by double clicking on it), then open the (C:) icon.

2.) On the C: Window, click File, then New, then Folder.

3.) Name the new folder: hd0 .

4.) Repeat steps 1 thru 3 to create another new folder and name it: S5NetInstall – Do not create the second new folder in the first one, create it on the root directory (C:).

5.) Open the two new folders.

6.) In the windows for the two new folders, click View then details. – Do not close the windows at this time.

9.2 Transfer files from the CD ROM, GEVU Part Number FB200084

1.) On the windows desktop, return to the My Computer icon, then open the CD Rom icon (D:). On the CD there are two folders: hd0, S5NetInstall and Documents.

2.) Open hd0 folder. The hd0 folder only contains the vx040.st file. Highlight it and drag and drop it in the new hd0 folder on your root directory (C:).

3.) Open S5NetInstall folder, the folder contains these files : (See the tables below.)

Filename	Module Software Revision	Poles
bt99_a.tar.gz	1.8 (Advantage, Membership)	Europe and Asia
bt99_p.tar.gz	1.8 (Performance, Elite & Premium)	Europe and Asia
bt99_us.tar.gz	1.8 (us)	Americas

Table 0-1 Basic software alternatives.

Filename	System model	Module software revision	Poles	Note
svision_bt99_a.tar.gz	All System FiVe with Integrated EchoPAC	Integrated EchoPAC	Europe and Asia	For System FiVes w/ integrated EchoPAC ONLY.
svision_bt99_p.tar.gz	All System FiVe with Integrated EchoPAC	Integrated EchoPAC	Europe and Asia	
svision_bt99_us.tar.gz	All System FiVe with Integrated EchoPAC	Integrated EchoPAC	Americas	

Table 0-2 Option files.

4.) It is important to install the correct software file onto the System FiVe harddisk (recorded in Section 7.0 - Test and Verification Prior to Upgrade**, step 5**).

a.) Highlight the required software files on drive **D:.**

b.) **Remember:**
If the system has an integrated MAC (Supervision), highlight one of these files too:

* svision_bt99_a.tar.gz or svision_bt99_p.tar.gz (Europe/Asia) or
* svision_bt99_us.tar.gz (Americas).

c.) Drag and drop them into the new **S5 NetInstall** folder on root directory (**C:**).

5.) Record in the spaces below the names of all the files copied. Also note which of the copied files is the largest (about 17 MB) ending with **.tar.gz** of the software version being loaded.

Note: The name of these files will be entered in later during the software load.

Filenames	Size
_____	_____
_____	_____

Note: Throughout this procedure you will be instructed to enter information into the laptop, pay strict attention to how it is shown in the procedure and type the information in exactly as it is presented (bold type). If for instance if it shows quotes, use quotes. Most errors in performing this procedure occur when the information is entered incorrectly.

Section 10.0 - Connect VT220 Terminal Emulator to System FiVe

1.) Connect the Ethernet adapter 10 base-T to external I/O port CPU1 connector
2.) Connect the crossed ethernet cable between the PC Card Lan cable adapter, (connected to your ethernet card in your laptop) and the System FiVe Ethernet adapter connector.
3.) Connect COM1 of VT220 Terminal Emulator (laptop) to System FiVe's External I/O port RS232 CPU connector using null modem cable.

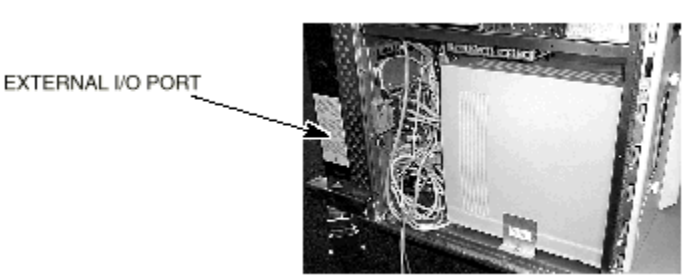


Figure 0-1 System FiVe External I/O

Section 11.0 - Set Up VT220 Terminal Emulator

Note: **This procedure uses a diagnostic PC with HyperACCESSq (HA) software to serve as a VT220 Terminal Emulator, but any VT220 Terminal Emulator can be used as long the settings from** Table 0-3 on page N- 14 **are entered correctly into the alternative terminal.**

1.) On the diagnostic PC, start HyperACCESSq software.
2.) Click on the New button to create a new System FiVe entry or click on the Settings button to review or modify an existing entry

Figure 0-2 HyperACCESSq Controls

3.) Enter the settings shown in Table 0-4 on page N- 15 for the System FiVe entry.

Phone No.:	leave empty
Settings:	8–none–1 (Click arrow to show choices)
Terminal Emulation:	VT220 (Click arrow to show choices)
Terminal Setup...	[Enter] select Terminal keys, not Windows; Rest of the choices are all off or default
Baud Rate:	9600 (click on nearby arrow to get choices)
Priority:	Normal
Port type:	Standard Com Port
Port name:	COM1 (if this is the laptop port you will use)
Port Setup...	HW handshake RTS/CTS on; turn SW handshaking off by clicking on the x's to get rid of it.
Modem:	Direct Connect (Cabled)

Table 0-3 Settings required for terminal communication

4.) Click on the square button with the down arrow to see/select from choices.

5.) Click on the OK button to accept and close screens

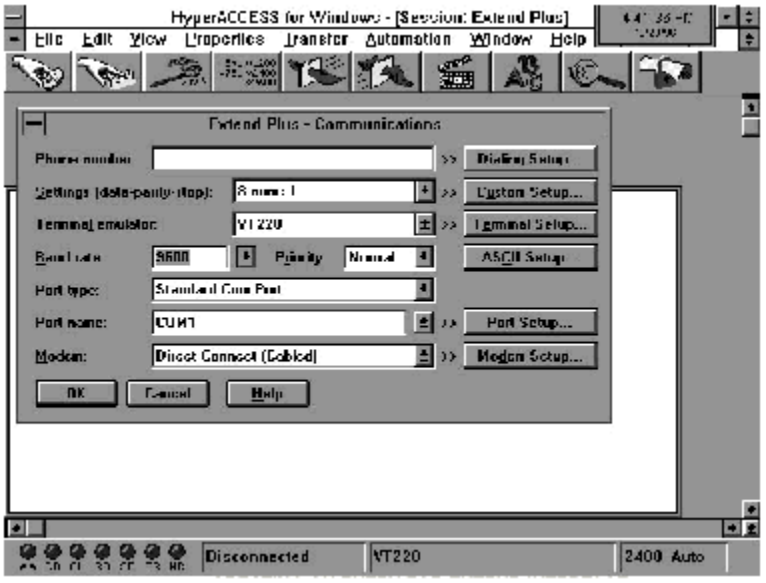


Figure 0-3 Creating an entry for extended interface

6.) 0nce the settings from Table 3 have been entered, click File then Save and save this setup as: system five.has.

7.) If necessary, double click the system five icon on the laptop to start HyperACCESS Terminal emulation program.

Section 12.0 - Record System FiVe Settings

Refer to "Booting Sequence" starting on page K07-1

1.) Once the boot sequence has completed, type bootChange on the laptop window and the following will be displayed on the laptop:

–> bootChange
" . " = clear field; " _ " = go to previous field; ^D =quit

2.) Hit Enter on the laptop and record the following information:

Note: Continue pressing Enter on Laptop to Scroll from one entry to the next.

Entry Name	Possible Entry-(Example)	Actual Entry	Comments
Boot device	scsi=0,0		
Processor number	0		
Host name			
File name	/hd0/vx040.st		
Inet on ethernet (e)	3.222.21.232:fffffc00		If in network, this IP address will be different
Inet on backplane (b)			
Host inet (h)			
Gateway inet (g)			
User (u)	s5_rack		
Ftp password (pw) (blank=use rsh)			
Flags (f)	0x8		
Target name (tn)	wind8		
Startup script (s)	etc/init		
Other (o)	ei		

Table 0-4 Default Bootsettings

3.) Once the laptop has scrolled through the above information it will display:

value=0=0X0
–>

Section 13.0 - Set Laptop IP Address

1.) On the windows desktop, open My Computer, then Control Panel, then Network –>TCP/IP, then 3 Com Ether Link III LAN PC Card (3C589D – some laptops may have a different card) record old settings, then enter an IP address from the following choices:

Note: **If it is unclear as to whether the system you are loading with the new soft-**

ware is an old system, a new system, or a networked system, reboot the system (See "- Record System FiVe Settings" on page 15.**) and record the Backplane Address during the Boot Sequence. The Backplane address will be a 193.... series number, a 3.222.... series number, or if networked any possible XXX.XXX.XXX.XXX series number.**

a.) In old systems enter: 193.69.49.5 (the range is 193.69.49.0–193.69.49.255, but don't use 193.69.49.232, 193.69.49.233 or 193.69.49.234 which are used by System FiVe). Subnetmask must be set to: 255.255.255.0 .

b.) In new systems enter: 3.222.21.5 (the range is 3.222.21.0–3.222.21.255, but don't use 3.222.21.232, 3.222.21.233 or 3.222.21.234 which are used by System FiVe). Subnetmask must be set to: 255.255.252.0 .

c.) In networked systems enter: XXX.XXX.XXX.5 (network IP address), except use X's for 1st three segments.

2.) After IP address has been changed, reboot the Laptop.

Section 14.0 - System FiVe Software Upgrade

14.1 Loading Software Using Laptop as an FTP Server

Note: **This procedure uses the laptop as an FTP server and boots System FiVe from the PC over the ethernet connection. The new software will be transferred and unpacked in one command. The procedure can be used on brand new disks or disks that are corrupted (but not destroyed). There are several FTP servers on the marked, but this procedure will only refer to the two most known FTP servers used by GE service personnel: serv-u32 and Chameleon FTP.**

14.2 Starting Serv-u32 FTP Server

1.) Start the serv-u32.exe file.
2.) Choose Setup. Click User then New
3.) At the User Name prompt type: s5_rack
4.) Password: is displayed on laptop.
5.) At the Password prompt type: s5
6.) Homedirectory : c:\
7.) Enable "Enable account"
8.) Select Add, write c.\

(See illustration on next page)

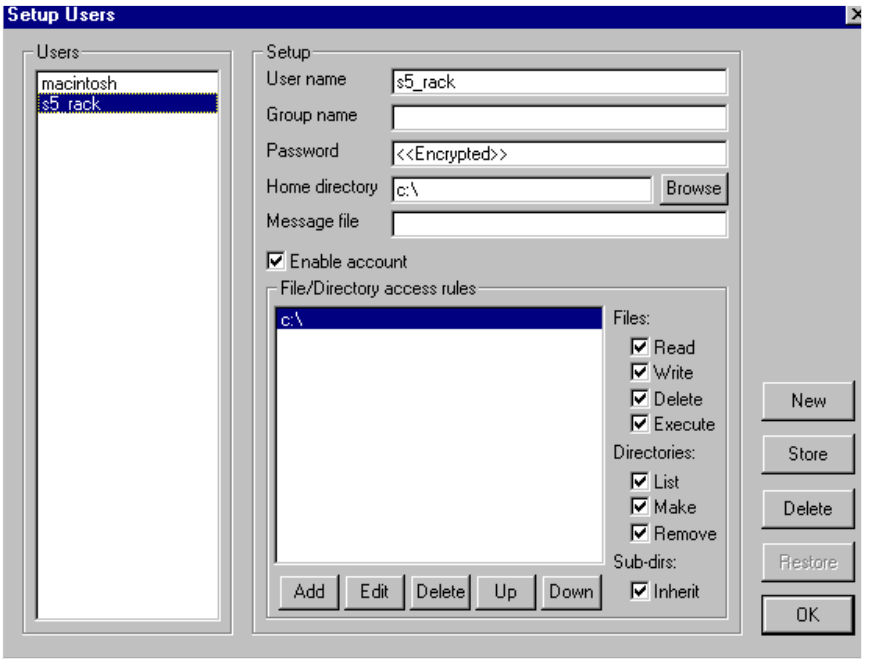


Figure 0-4 Serv-u32 Setup-window

14.3 Starting Chameleon FTP Server

1.) On the Laptop windows desktop, click Start then Programs then Chameleon then FTP Server.
2.) Click Users then Add.
3.) User Name: is displayed on laptop.
4.) At the User Name prompt type: s5_rack
5.) Password: is displayed on laptop.
6.) At the Password prompt type: s5
7.) Access prompt is displayed on laptop.
8.) Click OK then click OK again.

Note: The server is now up and running and it can just run in the background.

14.4 Change the Boot Configuration on the System FiVe

1.) Enable the hyperaccess terminal window, located on your Desktop
2.) Type bootChange to change the boot change sequence at the hyperaccess terminal prompt.

The following entry name items in Table 0-5 on page N- 18 will be displayed on the laptop:

Note: Continue to press Enter on Laptop to Scroll from one entry to the next. For each new entry the "Change to" must be entered (Do not backspace !!)

Entry Name	Original data	Default entry	Change to	Comments
Boot device	scsi=0,0	scsi=0,0	ei	Boots over ethernet interface
Processor number	0	0		Just hit return
Host name				Just hit return
File name	/hd0/vx040.st	/hd0/vx040.st		Just hit return
Inet on ethernet (e)	3.222.21.232:ffff fc00	3.222.21.232:ff fffc00		Just hit return
Inet on backplane (b)				Just hit return
Host inet (h)			3.222.21.5	
Gateway inet (g)			. (period)	
User (u)	s5_rack	s5_rack		Just hit return
Ftp password (pw) (blank=use rsh)			s5	Same password as you entered in your FTP server
Flags (f)	0x8	0x8		Just hit return
Target name (tn)	wind8	wind8		Just hit return
Startup script (s)	etc/init	etc/init	. (period)	
Other (o)	ei	ei	. (period)	

Table 0-5 Bootchange entries

After the last entry in the Bootchange table this message will appear:

value=0=0X0
–>

14.5 Installation of the System FiVe Software

1.) Type reboot at the hyperaccess terminal prompt and hit Enter. The following is displayed on the laptop:

boot device : ei
processor number : 0
hostname :
file name : /hd0/vx040.st
inet on ethernet (e) : 3.222.21.232:fffffc00
inet on backplane (b) :
host inet (h) : 3.222.21.5
gateway inet (g) :
user (u) : s5_rack
ftp password (pw) : (blank = use rsh):s5
flags (f) : 0x8
target name (tn) : wind8

Attaching network interface ei0... done.

Attaching network interface lo0... done.

Loading... 606464 + 110204 + 28264
Starting at 0x20000...

Host Name: bootHost

Attaching network interface ei0... done.
Initializing backplane net with anchor at 0x600... done.
Backplane anchor at 0x600... Attaching network interface sm0... done.
Backplane address: 3.222.21.233
Creating proxy network: 3.222.21.233
Attaching network interface lo0... done.
Attaching shared memory objects at 0x600... done
–>

Note: If an error occurs and you do not have a prompt, refer to Appendix E for trouble-shooting

14.6 Formatting the Harddisk

1.) Type dosVolMake 0 at the hyperaccess terminal prompt. (Separate dosVolMake and 0 with a space)

The following is displayed on the laptop:
value = 847828 = 0xcefd4 followed by the command prompt
–>

2.) Type diskInit "/hd0" at the hyperaccess terminal prompt.

The following is displayed on the laptop:

"/hd0" initialized.
value = 0 = 0x0

The largest software "tar.gz" file must be installed prior to all other software files.

3.) Type netinstall "filename.tar.gz" (where filename.tar.gz is a software file from Table 1.), then Enter at the hyperaccess terminal prompt. The following is displayed on the laptop :

Connecting.... done.
Receiving.... _++] 39
13.4 351
Expanding.... _++]
126 48.2 391
Expanding.... _++]
215 46.8 223
Installation completed in 381 seconds (1740f/264d).
value=0=0X0
–>

Note: **The "svision_v1.8.tar.gz" file only has to be unpacked if system has an integrated MAC.**

4.) Type netinstall "svision_v1.8.tar.gz", then Enter at the hyperaccess terminal prompt.

The following is displayed on the laptop :
Connecting.... done.
Receiving.... _++]
Expanding.... _++]
Expanding.... _++]
Installation completed in 381 seconds (1740f/264d).
value=0=0X0
–>

14.7 Change The Boot Configuration Back To Normal

1.) Type bootChange at the hyperaccess terminal prompt and hit Enter. The boot configuration is displayed in Table 0-6 on page N- 20:

Note: Continue to press Enter on Laptop to Scroll from one entry to the next. For each new entry the "Change to" must be typed entered (Do not backspace !!)

Bootconfiguration	Original data	Default entry	Change to	Comments
Boot device	scsi=0,0	ei	scsi=0,0	Boots over ethernet interface
Processor number	0	0		Just hit return
Host name				Just hit return
File name	/hd0/vx040.st	/hd0/vx040.st	/hd0/vx040.st	Just hit return
Inet on ethernet (e)	3.222.21.232:fffffc00	3.222.21.232:fffffc00	3.222.21.232 :fffffc00	Address recorded in step 2, page 15
Inet on backplane (b)				Just hit return
Host inet (h)		3.222.21.5	. (period)	
Gateway inet (g)				Just hit return
User (u)	s5_rack	s5_rack		Just hit return
Ftp password (pw) (blank=use rsh)		s5		Enter period to erase password
Flags (f)	0x8	0x8		Just hit return
Target name (tn)	wind8	wind8		Just hit return
Startup script (s)	etc/init	. (period)	etc/init	
Other (o)	ei	. (period)	ei	

Table 0-6 BootConfiguration restoration

After the last entry in the bootChange table this message will appear :
value=0=0X0
–>

14.8 Finishing the Upgrade

1.) Exit the server by closing the Chameleon FTP server. Failure to close the FTP server may corrupt the drivers for your LAN card preventing you from doing upgrades in the future.

2.) Shut the System Five down using the power switch.

3.) Remove the twisted pair cable used for the FTP transfer. (Leave the null–modem RS–232 cable installed to observe the boot). If required, reconnect network cable and/or transceiver.

4.) Turn the system ON again. Verify boot up sequence is similiar as shown in section Section 12.0 on page 15.

5.) Verify system functionality in all scanning modes.

Section 15.0 - Completion of the Upgrade

15.1 Enable the Password Controlled Functions

To get access to the Password Controlled Functions, the correct password is needed. These Password Controlled Functions are available as separate options.

Follow these instructions to enable the Password Controlled Functions:

1.) Press the SETUP key once to display the Setup menu on the screen.

2.) Select the Configuration & Test submenu.

3.) In the Configuration/Test submenu, select Options to view the System FiVe Installed Modules window.

4.) Highlight the Password field, type the correct password for this scanner and press Enter.

5.) Verify that the correct options are turned on (yellow color).

15.2 Restoring System Setups

1.) Where applicable, restore system presets written down prior to the upgrade.

2.) Verify that correct video standard (PAL/NTSC) is selected in the Setup -> Video Settings menu (password is setfive). Verify that different setting is the same as recorded inittially in section 1-5. If the system has an integrated MAC with full screen RGB option (MUX-BOX'es), verify that Switchbox is selected. If the system does not have an integrated MAC with this option, deselect the option Switchbox installed.

3.) In the Setup -> Location menu, verify that correct date format is selected. Enter hospital specific information per site.

4.) In Measure -> CONFIG SP -> Caliper Config, restore setting of "Spectrum Caliper button as point".

15.3 Storing/Restoring System Setups by using FTP

Note: This procedure is only valid for sytem sw. v.1.8 and above.

One of the new features in this sw version (v.1.8) is the ability to store and restore System Setups by using FTP.

Follow the procedure below if you wants to store/restore system setups after v.1.8 has been installed.

15.3.1 Store Setups.

1.) Choose from the frontpanel:
   a.) Setup
   b.) Configuration & Test
   c.) GE Service, Password: setfive
   d.) User Defaults
   e.) Compact Files
2.) Connect Crossed Ethernet cable and Serial cable to External I/0
3.) Establishing FTP Client Connection To System FiVe
   a.) Start Chamelon FTP Client
   b.) Select Settings.
   c.) Select Preferences.
   d.) Verify that the choice Retrieve Detailed File Listing is switched OFF.
   e.) Close preferences window.
   f.) Select Connect to
   g.) Under Host write the scanners IP address recorded in step 2, page 15.
   h.) Under Password write s5
   i.) Select OK
4.) In the Remote window the files on root level of System FiVe will be listed.
   a.) Copy the file udd.tar.gz to the pc by using the copy button in the FTP Client window.
   b.) Use the arrow that point's to the left, i.e from the scanner to the pc.

15.3.2 Restore Setups

1.) Connect Crossed Ethernet cable and Serial cable to External I/0
2.) Establishing FTP Client Connection To System FiVe
   a.) Start Chamelon FTP Client
   b.) Select Settings.
   c.) Select Preferences.
   d.) Verify that the choice Retrieve Detailed File Listing is switched OFF.
   e.) Close preferences window.
   f.) Select Connect to
   g.) Under Host write the scanners IP address recorded in step 2, page 15.
   h.) Under Password write s5
   i.) Select OK
3.) In the Local window the files on your PC will appear. In the Remote window the files on root level of System FiVe will be listed.
   - Copy the file udd.tar.gz from the pc to the scanner by using the copy

button in the FTP Client window. Use the arrow that point's to the right, i.e from the pc to the scanner.

4.) Choose from the frontpanel:

a.) Setup
b.) Configuration & Test
c.) GE Service, Password: setfive
d.) User Defaults
e.) Extract Files
f.) Reebot the scanner and verify that the user defaults have been restored.

15.4 Restoring Laptop Settings

- Restore TCP/IP settings previously modified under the laptop's network control panel, previously recorded in "- Set Laptop IP Address" on page Intro-15.

15.5 FE Alignment

1.) Install a FPA probe in connector 1.
2.) Perform FE alignment, refer to "FE "Calibration" Procedure" on page K16-1
3.) If the FE alignment fails, reboot the scanner and try again.
4.) Reboot system after FE alignment is finished and verify proper operation.

15.6 Setup of EchoPAC and System FiVe for Continuous Capture

Note: For Integrated systems that run Continuous Capture.

1.) On System FiVe, press Setup,
2.) Reenter the setup settings saved in "- Record System FiVe Settings" on page Intro-15.
3.) Under footswitch settings in setup menu reserve footswitch for EchoPAC for all probes.

15.7 System Test

Note: Not all tests are applicable for all system configurations (with/without MAC, with/without Continuous Capture).

Note: You may refer to the "Performance Test (System Test) Procedure" on page K11-1 **when you perform these tests.**

1.) Verify all System FiVe modalities (2D, CFM, Doppler, M–mode etc.)
2.) Verify full–screen switching between Mac and System when depressing EchoPAC key.
3.) Verify VCR record and playback of both System FiVe RGB and EchoPAC RGB.
4.) Verify Color print and B/W print when applicable. (NOTE: It is not possible to print EchoPAC pictures to these printers, unless during playback from the VCR).
5.) Verify System FiVe to EchoPAC digital and video transfer.

15.8 PAMPTE Probe Test Procedure (if site has one)

1.) Power on system (if it isn't already on). Select the PAMPTE probe. It will after selection calibrate the second scan plane position by going to 180 degrees and then back to zero.

2.) Verify that the temperature reading is reasonable (there is no need to do an exact temperature calibration).

3.) Verify that the scan plane can be rotated using the two scan plane control buttons (fast and slow left rotation, fast and slow right rotation).

4.) Verify that the scan plane indicator on the screen is updated when these controls are manipulated.

15.9 Password Options

1.) Enter System Menu

2.) Select Configuration & Test -> Options.

- Yellow indicates *Enabled* Password,
- Grey indicates *Not Enabled* Password.

3.) Verify that the supplied Password coresponds to the System's Serial Number, listed on the screen.

Note: For systems with motherboard Serial Numbers up to 290, the Serial Number must be typed in manually.

4.) Enter the given password to enable the options for the system.

15.10 Paperwork Completion

1.) Complete and return the Product Locator Card.

2.) Leave the Password paper sheets with the customer.

3.) Leave the BT'99 CD with the customer.

4.) Hand the Release Note (FA040050) and User Manual Update, supplied with the kit, to the customer.

System FiVe Software Upgrade to v.1.9

This document describes how to upgrade System FiVe's system software using an FTP procedure.

Section 1.0 - Effectivity

This procedure may be used for updating all GE Vingmed System FiVe Ultrasound units.

Section 2.0 - Purpose

This System FiVe Software Upgrade's sole purpose is for the installation of v.1.9 software.

Section 3.0 - Pre-requisite

The system software must be on v.1.7.x or v.1.8 level.

Section 4.0 - Related FMI's

None

Section 5.0 - Furnished Materials

See "Detailed Parts List" in the Installation Procedure, GEVU Part Number FB094178.

Section 6.0 - Introduction

6.1 Time to Complete

One person 8 hour labor plus travel.

6.2 Tools and Test Equipment

- Standard GE Vingmed Field Service Tool Kit, please see "Test Equipment and Tools Required" on page Intro-9 for details.
- Ethernet cable (crossed twisted pair) (G.E. part # 2244684)
- Optional direct hub connect cable.A non crossed twisted pair cable must be used.
- Optional direct hub connect with coax, 2 terminators (50 ohm) and 2 BNC-T adapters are required.
- Ethernet adapter 10 base – T, (G.E part # 2195664)

- PC/Laptop with Ethernet card support.
- Ethernet card with PC Card Lan cable adapter for 10 Base-T and Coax
- Null modem cable (G.E part # 2117638-3).

6.3 Software Requirements for PC/ Laptop

To install System FiVe software from PC/Laptop, the PC/Laptop must meet the following requirements:

1.) Operating system: Windows 95 or NT.

2.) Terminal Emulation software (e.g. Hyper terminal, setup: baud rate 9600, 8 bits-no parity – 1 stopbit). See *Table 0-4 on page 30* for details.

3.) A FTP program that can function as a FTP Server. (

Note: Chameleon FTP server software, can be downloaded from the GEMS Home Page.

6.4 Compatibility vs. EchoPAC software

The System FiVe's system software v.1.9 is compatible with EchoPAC sw.6.2 and above.

Section 7.0 - Test and Verification Prior to Upgrade

1.) Run an automatic test prior to starting the upgrade. See "Performance Test (System Test) Procedure" on page K11-1 for detailed instructions. Correct any problems reported or observed before proceeding.

2.) Storing setups and User defaults

a.) When upgrading from sw.v.1.8 only:

1.) Store the System Setups as described in 15.3.1 Store Setups.on page 40.

2.) Then jump to section Section 9.0 on page 28 (- Copy System FiVe Software from CD to PC).

b.) When upgrading from sw.1.7.x, proceed on the next step.

3.) [Sw.1.7.x only] Since there is currently no automatic way of saving and restoring setups and user defaults, the following manual procedure should be used. Please ensure the customer is aware of this!

Note: All probe presets will be lost!

4.) [Sw.1.7.x only] Press Setup on the keyboard, select each menu item in the setup menu and note down the specific details on a piece of paper.

5.) [Sw.1.7.x only] Press the Application menu and verify if there are specific user setups, make a note of them. (verify all available probes).

6.) [Sw.1.7.x only] Enter Setup menu on the Front Panel.

a.) In the menu that appears on screen, select System Test menu button.

b.) In the System Test menu, choose Module SW version.

c.) Write down the System Software Name listed in the Module Software Revisions List

	File name/ date	(System/options)
System FiVe :	_____	(_____)
Options :	_____	_____

Table 0-1 System Software Name listed in the Module Software Revisions List.

Note: **Membership and Advantage will need a password for all functions covered by the introducing offering on Advantage:**

Functions:

-
-
-
-
-
-

7.) [Sw.1.7.x only] Select the Applications menu when having the 2.5 FPA probe connected, The following software options must be verified and noted for:
   - RF,
   - Contrast,
   - TVI,
   - or any combination of these options.

Section 8.0 - Install Memory Upgrade

[Sw.1.7.x only]

1.) Turn of the power (rear of system).
2.) Remove both the Upper and the Lower Covers on the left side.
3.) Un-screw the retaining screws used for fastening the System Processor Board and pull out the board.
4.) Un-screw the screws holding the RAM piggyback and remove the piggyback.
5.) Gently install the new memory piggy back and fasten it with the screws that were used for the old piggy back.
6.) Insert the Processor board in the board rack, in the same position it was before. Be sure that it is seated properly. Fasten the retaining screws.
7.) Turn on the power and boot the scanner.
8.) Verify that all the boards starts (the red LEDs are turned off) and that the system boots completely.
9.) Turn off the system and mount the panels you removed earlier.

Section 9.0 - Copy System FiVe Software from CD to PC

9.1 Create file structure on root directory (C:)

Note: **If the laptop has an Auto–sleep feature it needs to be turned off during this procedure. Make sure you have more than 20 MByte of free space on your hard disk.**

1.) On the windows desktop, open the My Computer icon (by double clicking on it), then open the (C:) icon.

2.) On the C: Window, click File, then New, then Folder.

3.) Name the new folder: hd0 .

4.) Repeat steps 1 to 3 to create another new folder and name it: S5NetInstall – Do not create the second new folder in the first one, create it on the root directory (C:).

5.) Open the two new folders.

6.) In the windows for the two new folders, click View then details. – Do not close the windows at this time.

9.2 Transfer files from the CD ROM

1.) On the windows desktop, return to the My Computer icon, then open the CD Rom icon (D:). On the CD there are two folders: hd0, S5NetInstall and Documents.

2.) Open hd0 folder. The hd0 folder only contains the vx040.st file. Highlight it and drag and drop it in the new hd0 folder on your root directory (C:).

3.) Open S5NetInstall folder, the folder contains these files: (See the tables below.)

Filename	Module Software Revision	Poles
1.9_a.tar.gz	1.9 (Advantage, Membership)	Europe and Asia
1.9_p.tar.gz	1.9 (Performance, Elite & Premium)	Europe and Asia
1.9_us.tar.gz	1.9 (us)	Americas

Table 0-2 Basic software alternatives.

Filename	System model	Module soft-ware revision	Poles	Note
svision_v1.9_a.tar.gz	(Advantage, Membership)	Integrated EchoPAC	Europe and Asia	For System FiVes w/ inte-grated Echo-PAC ONLY.
svision_v1.9_p.tar.gz	(Performance, Elite & Premium)	Integrated EchoPAC	Europe and Asia	
svision_v1.9_us.tar.gz	(US)	Integrated EchoPAC	Americas	

Table 0-3 Option files.

4.) It is important to install the correct software file onto the System FiVe hard disk. (Recorded in Section 7.0 - Test and Verification Prior to Upgrade, step 5). Highlight the required software files on drive D:.

(Remember: If the system has an integrated MAC (Supervision), highlight the respective svision file too). Drag and drop them into the new S5NetInstall folder on root directory (C:).

5.) Record in the spaces below the names of all the files copied. Also note which of the copied files is the largest (about 17 MB) ending with .tar.gz of the software version being loaded.

Note: The name of these files will be entered in later during the software load.

Filenames	Size

Note: **Throughout this procedure you will be instructed to enter information into the laptop, pay strict attention to how it is shown in the procedure and type the information in exactly as it is presented (bold type). If for instance if it shows quotes, use quotes. Most errors in performing this procedure occur when the information is entered incorrectly.**

Section 10.0 - Connect VT220 Terminal Emulator to System FiVe

1.) Connect the Ethernet adapter 10 base-T to external I/O port CPU1 connector

2.) Connect the crossed ethernet cable between the PC Card Lan cable adapter, (connected to your ethernet card in your laptop) and the System FiVe Ethernet adapter connector.

3.) Connect COM1 of VT220 Terminal Emulator (laptop) to System FiVe's External I/O port RS232 CPU connector using null modem cable.

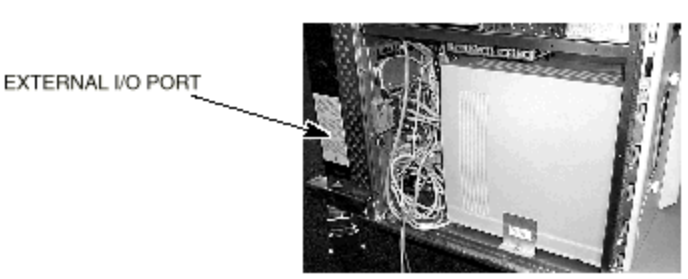


Figure 0-1 System FiVe External I/O

Section 11.0 - Set Up VT220 Terminal Emulator

Note: **This procedure uses a diagnostic PC with HyperACCESSq (HA) software to serve as a VT220 Terminal Emulator, but any VT220 Terminal Emulator can be used as long the settings from** Table 0-4 on page 30 **are entered correctly into the alternative terminal.**

1.) On the diagnostic PC, start HyperACCESSq software.

2.) Click on the New button to create a new System FiVe entry or click on the

Settings button to review or modify an existing entry

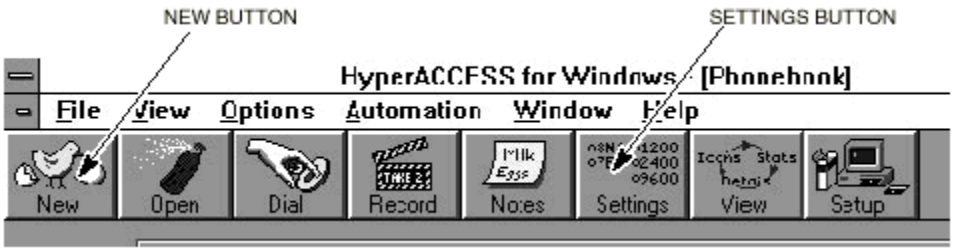


Figure 0-2 HyperACCESSq Controls

1.) Enter the settings shown in Table 0-5 on page 34 for the System FiVe entry.

Phone No.:	leave empty
Settings:	8–none–1 (Click arrow to show choices)
Terminal Emulation:	VT220 (Click arrow to show choices)
Terminal Setup...	[Enter] select Terminal keys, not Windows; Rest of the choices are all off or default
Baud Rate:	9600 (click on nearby arrow to get choices)
Priority:	Normal
Port type:	Standard Com Port
Port name:	COM1 (if this is the laptop port you will use)
Port Setup...	HW handshake RTS/CTS on; turn SW handshaking off by clicking on the x's to get rid of it.
Modem:	Direct Connect (Cabled)

Table 0-4 Settings required for terminal communication

1.) Click on the square button with the down arrow to see/select from choices.

2.) Click on the OK button to accept and close screens

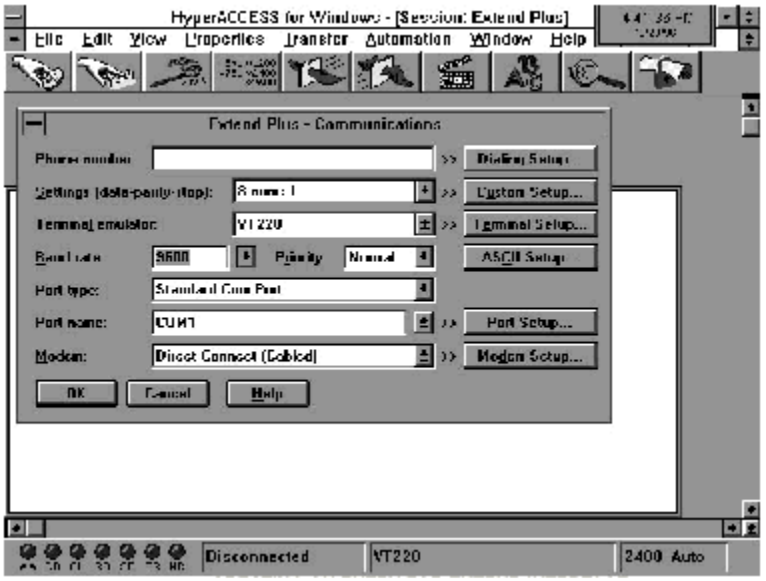


Figure 0-3 Creating an entry for extended interface

2.) 0nce the settings from Table 3 have been entered, click File then Save and save this setup as: system five.has.

3.) If necessary, double click the system five icon on the laptop to start HyperACCESS Terminal emulation program.

Section 12.0 - Record System FiVe Settings

1.) Boot system.

Note: The following boot sequence example is shown in its entirety for reference purposes only and the actual boot sequence may differ slightly.

VxWorks System Boot

Copyright 1984–1993 Wind River Systems, Inc.

CPU: Motorola MVME167
Version: 5.1.1
BSP version: 1.0
Creation date: Tue May 24 11:24:05 MET DST 1994

Press any key to stop auto–boot...
0
auto–booting...
Waiting for disk to spin up..... done.
Attaching to scsi device... done.

Loading /hd0/vx040.st...655308 + 112484 + 64852
Starting at 0x20000...

Host Name: bootHost
Attaching network interface ei0... done.

Initializing backplane net with anchor at 0x600... done.
Backplane anchor at 0x600... Attaching network interface sm0...

done.

Note: Backplane address indicates whether system is an old system or a new system. 3.222.... series addresses are new systems and 193.69.... series addresses are old systems or Network systems.

```
Backplane address: 3.222.21.233
Creating proxy network: 3.222.21.233
Attaching network interface lo0... done.

Attaching shared memory objects at 0x600... done

Adding 3447 symbols for standalone.

CPU: Motorola MVME167. Processor #0.
Memory Size: 0x2000000.BSP version 1.0.

Executing startup script etc/init ...
cintStartupScript (”etc/init.c”, 0x10000, 0, 0, 101)
value = 0 = 0x0

Done executing startup script etc/init

Executing C startup script etc/init.c...
Mounting ”/hd0”... nfs export... done.
Loading ”lib/dmem.o”... done.
dmem: Allocated memory pool of 31593372/0 bytes

Starting dynamic memory garbage collector... done.
Today is MON JAN 11 18:17:39 1999
Verifying graph5... data path test... done.
Loading ”lib/g5.img” onto graph5... dmem: GCTask waiting ticks to
start
done.
Loading ”usr/lib/X11/fs/fs.o”... dmem: Free memory at 0x01F82578
not allocated tt
dmem: Free memory at 0x01F73124 not allocated by dmem – lost
dmem: Free memory at 0x01FAD780 not allocated by dmem – lost
dmem: Free memory at 0x01F79DE0 not allocated by dmem – lost
dmem: Free memory at 0x01F728A8 not allocated by dmem – lost
dmem: Free memory at 0x01FA4F6C not allocated by dmem – lost
dmem: Free memory at 0x01F71DCC not allocated by dmem – lost
dmem: Free memory at 0x01F71EFC not allocated by dmem – lost
dmem: Free memory at 0x01FA4F58 not allocated by dmem – lost
done.
Awaiting graph5 boot... done.
Awaiting X server start...dmem: Free memory at 0x01F86BC0 not
allocated by dmemtt
..... done.
Awaiting frontpanel start..... done.
Waiting for app to finish loading..... done.
Executing C++ config... done.
Calling static contructors...

All systems go...
dmem: Free memory at 0x01F17040 not allocated by dmem – lostd-
mem: Free memory at 0x01F37C58 not allocated by dmem – lost

dmem: Free memory at 0x01F27048 not allocated by dmem – lost

spawning filecache update task...Done
–> Create dispatcher...done
Create Datamodule...
```

Exception task started....

ImagePort: Hardware present !!!,

Scan converter Functional revision: C software support level 6
tTdpSched id accb34 up and listening ...
tSdpSched id ad0cc4 up and listening ...
done
Create Displaymodule...done
Create Framebuffer...done
Create USParameters...done
Create DisplayParameters...done
Initialize ParameterDictionary...done
initialized supervisor
Connected to front panel
Create VideoOut View...

(6 seconds)filecache entries : 1033
dircache entries : 181
FileCache is up to date...
done
Initialize gaGui...done
Create Users View and slider...SONY VCR detected

Registering ProbeTempSource: pipe(/pipe/probeTemp)
Registering RackTempEventSource: pipe(/pipe/rackTemp)
Registering FootSwitchEventSource: pipe(/pipe/footSwitch)
Registering PowerDownEventSource: pipe(/pipe/powerDown)
Registering HeartRateEventSource: pipe(/pipe/heartRate)
Registering ProbeEventSource: pipe(/pipe/probeEvent)
Registering EventSource3D: pipe(/pipe/acq3D)
Registering ScanPlane2EventSource: pipe(/pipe/scanPlane2)

RFT_RPC::loadprogram()...ok.
FEC_RPC::loadprogram()...ok.

SYSTEM FIVE Version: High End
SDP_RPC::loadprogram()...ok.
CFP_RPC::loadprogram()...ok.
IOP_RPC::loadprogram()...ok.
done
Create Remote control...done
Create setup dialog...done
Create screen conf dialog...done
Create patient browser...PatientBrowser : readUDTData() failed!
done
Create macXfer...EchoPAC_talk successfully started ! Waiting for EchoPAC to con.
done
Create Clipboard...ClipboardDisplay::ClipboardDisplay : getObject failed. Name r
ClipboardDisplay::ClipboardDisplay : getObject failed. Name = mmode
ClipboardDisplay::ClipboardDisplay : getObject failed. Name = mmo-dec
done

Create report generator...Task VMSDiskWriter successfully started.
Ready to rec.
done
Create M&A...done
Create Annotation...done
Initialize VCR calibration...done

```
Initialize VideoScreen...done
started
initialized applications
states created
Entering running mode
Entering scanning mode
Entering users view mode
EchoPAC_talk::establishContact.....Contact established with Echo-
PAC !
dmem: GCTask started
–>
```

2.) Once the boot sequence has completed, type bootChange on the laptop window and the following will be displayed on the laptop:

```
–> bootChange
". " = clear field; "_ " = go to previous field; ^D =quit
```

3.) Hit Enter on the laptop and record the following information:

Note: Continue pressing Enter on Laptop to Scroll from one entry to the next.

Entry Name	Possible Entry-(Example)	Actual Entry	Comments
Boot device	scsi=0,0		
Processor number	0		
Host name			
File name	/hd0/vx040.st		
Inet on ethernet (e)	3.222.21.232:fffffc00		If in network, this IP address will be different
Inet on backplane (b)			
Host inet (h)			
Gateway inet (g)			
User (u)	s5_rack		
Ftp password (pw) (blank=use rsh)			
Flags (f)	0x8		
Target name (tn)	wind8		
Startup script (s)	etc/init		
Other (o)	ei		

Table 0-5 Default Boot settings

4.) Once the laptop has scrolled through the above information it will display:

```
value=0=0X0
–>
```

Section 13.0 - Set Laptop IP Address

1.) On the windows desktop, open My Computer, then Control Panel, then Network –>TCP/IP, then 3 Com Ether Link III LAN PC Card (3C589D – some laptops may have a different card) record old settings, then enter an IP address from the following choices:

Note: **If it is unclear as to whether the system you are loading with the new software is an old system, a new system, or a networked system, reboot the system (**See "- Record System FiVe Settings" on page 31.**) and record the Backplane Address during the Boot Sequence. The Backplane address will be a 193.... series number, a 3.222.... series number, or if networked any possible XXX.XXX.XXX.XXX series number.**

a.) In old systems enter: 193.69.49.5 (the range is 193.69.49.0–193.69.49.255, but don't use 193.69.49.232, 193.69.49.233 or 193.69.49.234 which are used by System FiVe). Subnetmask must be set to: 255.255.255.0.

b.) In new systems enter: 3.222.21.5 (the range is 3.222.21.0–3.222.21.255, but don't use 3.222.21.232, 3.222.21.233 or 3.222.21.234 which are used by System FiVe). Subnetmask must be set to: 255.255.252.0.

c.) In networked systems enter: XXX.XXX.XXX.5 (network IP address), except use X's for 1st three segments.

2.) After IP address has been changed, reboot the Laptop.

Section 14.0 - System FiVe Software Upgrade

14.1 Loading Software Using Laptop as an FTP Server

Note: **This procedure uses the laptop as an FTP server and boots System FiVe from the PC over the ethernet connection. The new software will be transferred and unpacked in one command. The procedure can be used on brand new disks or disks that are corrupted (but not destroyed). There are several FTP servers on the marked, but this procedure will only refer to the two most known FTP servers used by GE service personnel: serv-u32 and Chameleon FTP.**

14.2 Starting Serv-u32 FTP Server

1.) Start the serv-u32.exe file.
2.) Choose Setup. Click User then New
3.) At the User Name prompt type: s5_rack
4.) Password: is displayed on laptop.
5.) At the Password prompt type: s5
6.) Homedirectory : c:\
7.) Enable "Enable account"
8.) Select Add, write c.\

(See illustration on next page)

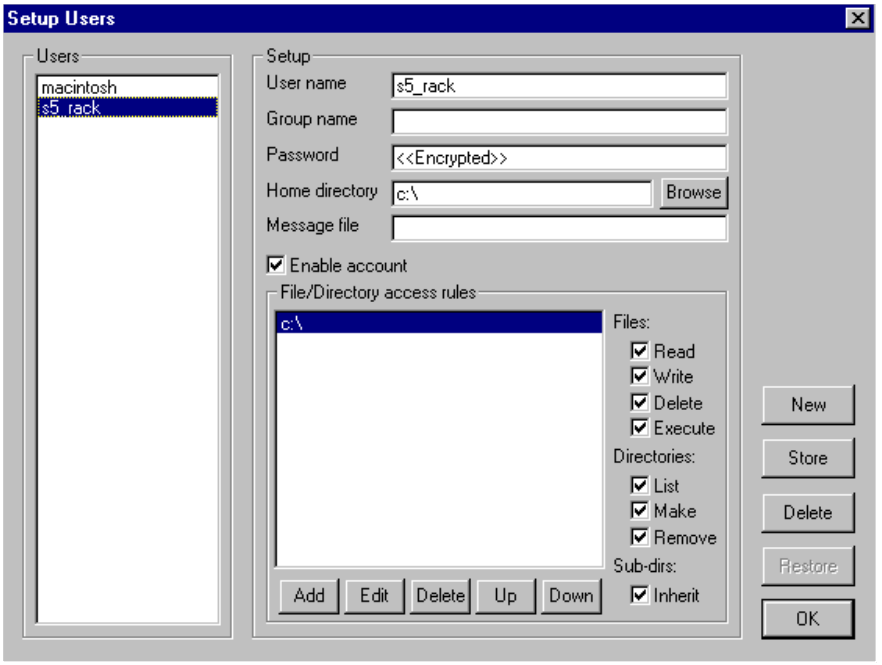


Figure 0-4 Serv-u32 Setup-window

14.3 Starting Chameleon FTP Server

1.) On the Laptop windows desktop, click Start then Programs then Chameleon then FTP Server.
2.) Click Users then Add.
3.) User Name: is displayed on laptop.
4.) At the User Name prompt type: s5_rack
5.) Password: is displayed on laptop.
6.) At the Password prompt type: s5
7.) Access prompt is displayed on laptop.
8.) Click OK then click OK again.

Note: The server is now up and running and it can just run in the background.

14.4 Change the Boot Configuration on the System FiVe

1.) Enable the hyperaccess terminal window, located on your Desktop
2.) Type bootChange to change the boot change sequence at the hyperaccess terminal prompt.

The following entry name items in Table 0-6 on page 37 will be displayed on the laptop:

Note: Continue to press Enter on Laptop to Scroll from one entry to the next. For each new entry the "Change to" must be entered (Do not backspace!!)

Entry Name	Original data	Default entry	Change to	Comments
Boot device	scsi=0,0	scsi=0,0	ei	Boots over ethernet interface
Processor number	0	0		Just hit return
Host name				Just hit return

File name	/hd0/vx040.st	/hd0/vx040.st		Just hit return
Inet on ethernet (e)	3.222.21.232:ffffc00	3.222.21.232:fffffc00		Just hit return
Inet on backplane (b)				Just hit return
Host inet (h)			3.222.21.5	Same address as PC/ laptop.
Gateway inet (g)			. (period)	
User (u)	s5_rack	s5_rack		Just hit return
Ftp password (pw) (blank=use rsh)			s5	Same password as you entered in your FTP server
Flags (f)	0x8	0x8		Just hit return
Target name (tn)	wind8	wind8		Just hit return
Startup script (s)	etc/init	etc/init	. (period)	
Other (o)	ei	ei	. (period)	

Table 0-6 Bootchange entries

After the last entry in the Bootchange table this message will appear:

value=0=0X0
–>

14.5 Installation of the System FiVe Software

1.) Type reboot at the hyperaccess terminal prompt and hit Enter. The following is displayed on the laptop:

boot device : ei
processor number : 0
hostname :
file name : /hd0/vx040.st
inet on ethernet (e) : 3.222.21.232:fffffc00
inet on backplane (b) :
host inet (h) : 3.222.21.5
gateway inet (g) :
user (u) : s5_rack
ftp password (pw) : (blank = use rsh):s5
flags (f) : 0x8
target name (tn) : wind8

Attaching network interface ei0... done.

Attaching network interface lo0... done.
Loading... 606464 + 110204 + 28264
Starting at 0x20000...

Host Name: bootHost

Attaching network interface ei0... done.

Initializing backplane net with anchor at 0x600... done.
Backplane anchor at 0x600... Attaching network interface sm0... done.
Backplane address: 3.222.21.233
Creating proxy network: 3.222.21.233
Attaching network interface lo0... done.
Attaching shared memory objects at 0x600... done
–>

Note: ! **If an error occurs and you do not have a prompt, refer to Appendix E for troubleshooting**

14.6 Formatting the Hard Disk

1.) Type dosVolMake 0 at the hyperaccess terminal prompt. (Separate dosVolMake and 0 with a space)

The following is displayed on the laptop:
value = 847828 = 0xcefd4 followed by the command prompt
–>

2.) Type diskInit "/hd0" at the hyperaccess terminal prompt.

The following is displayed on the laptop:

"/hd0" initialized.
value = 0 = 0x0

The largest software "tar.gz" file must be installed prior to all other software files.

3.) Type netinstall "filename.tar.gz" (where filename.tar.gz is a software file from Table 1.), then Enter at the hyperaccess terminal prompt. The following is displayed on the laptop:

Connecting.... done.
Receiving.... _++] 39
13.4 351
Expanding.... _++]
126 48.2 391
Expanding.... _++]
215 46.8 223
Installation completed in 381 seconds (1740f/264d).
value=0=0X0
–>

Note: The "svision_v.1.9._*.tar.gz" file only has to be unpacked if the System FiVe scanner has an integrated MAC.

4.) Type:
netinstall "svision_v1.9_a.tar.gz" or
netinstall "svision_v1.9_p.tar.gz" or
netinstall "svision_v1.9_us.tar.gz" and
then ENTER at the hyperaccess terminal prompt.

The following is displayed on the laptop :

Connecting.... done.
Receiving.... _++]
Expanding.... _++]
Expanding.... _++]
Installation completed in 381 seconds (1740f/264d).
value=0=0X0
–>

14.7 Change The Boot Configuration Back To Normal

1.) Type bootChange at the hyperaccess terminal prompt and hit ENTER.
The boot configuration is displayed in Table 0-7 on page 39:

Note: Continue to press ENTER on Laptop to Scroll from one entry to the next. For each new entry the "Change to" must be entered (Do not backspace !!)

Bootconfiguration	Original data	Default entry	Change to	Comments
Boot device	scsi=0,0	ei	scsi=0,0	Boots over ethernet interface
Processor number	0	0		Just hit return
Host name				Just hit return
File name	/hd0/vx040.st	/hd0/vx040.st	/hd0/ vx040.st	Just hit return
Inet on ethernet (e)	3.222.21.232:fffff c00	3.222.21.232:fffff c00	3.222.21.2 32:fffffc00	Address recorded in step 2, page 15
Inet on backplane (b)				Just hit return
Host inet (h)		3.222.21.5	. (period)	
Gateway inet (g)				Just hit return
User (u)	s5_rack	s5_rack		Just hit return
Ftp password (pw) (blank=use rsh)		s5		Enter period to erase password
Flags (f)	0x8	0x8		Just hit return
Target name (tn)	wind8	wind8		Just hit return
Startup script (s)	etc/init	. (period)	etc/init	
Other (o)	ei	. (period)	ei	

Table 0-7 Boot Configuration restoration

After the last entry in the bootChange table this message will appear:
value=0=0X0
–>

14.8 Finishing the Upgrade

1.) Exit the server by closing the Chameleon FTP server. **Failure to close the FTP server may corrupt the drivers for your LAN card preventing you from doing upgrades in the future.**
2.) Shut the System FiVe down using the power switch.
3.) Remove the twisted pair cable used for the FTP transfer. (Leave the null–modem RS–232 cable installed to observe the boot). If required, reconnect network cable and/or transceiver.
4.) Turn the system ON again. Verify boot up sequence is similar as shown in

section Section 12.0 on page 31.

5.) Verify system functionality in all scanning modes.

Section 15.0 - Completion of the Upgrade

15.1 Enable the Password Controlled Functions

To get access to the Password Controlled Functions, the correct password is needed. These Password Controlled Functions are available as separate options.

Follow these instructions to enable the Password Controlled Functions:

1.) Press the SETUP key once to display the Setup menu on the screen.
2.) Select the Configuration & Test submenu.
3.) In the Configuration/Test submenu, select Options to view the System FiVe Installed Modules window.
4.) Highlight the Password field, type the correct password for this scanner and press Enter.
5.) Verify that the correct options are turned on (yellow color).

15.2 Restoring System Setups

A.) When upgrading from sw.v.1.8 only: Restore the presets as described in section 15.3.2 Restore Setups on page 41.
B.) When upgrading from sw.v.1.7.x, please proceed on the steps below.

1.) Where applicable, restore system presets written down prior to the upgrade.
2.) Verify that correct video standard (PAL/NTSC) is selected in the Setup -> Configuration & Test -> GE Service -> Video Settings menu (two passwords may be used; service or setfive). Verify that different setting is the same as recorded initially in Section 7.0 on page 26. If the system has an integrated MAC with full screen RGB option (MUX-BOX'es), verify that Switchbox is selected. If the system does not have an integrated MAC with this option, deselect the option Switchbox installed.
3.) In the Setup -> Location menu, verify that correct date format is selected. Enter hospital specific information per site.
4.) In Measure -> CONFIG SP -> Caliper Config, restore setting of "Spectrum Caliper button as point".

15.3 Storing/Restoring System Setups by using FTP

Note: This procedure is only valid for system sw. v.1.8 and above.

One of the new features in this sw version (v.1.9) is the ability to store and restore System Setups by using FTP.

Follow the procedure below if you wants to store/restore system setups after v.1.9 has been installed.

15.3.1 Store Setups.

1.) Choose from the Front Panel:
   a.) Setup
   b.) Configuration & Test
   c.) GE Service, Password: two passwords may be used; service or setfive

d.) User Defaults
e.) Compact Files

2.) Connect Crossed Ethernet cable and Serial cable to External I/0
3.) Establishing FTP Client Connection To System FiVe

a.) Start Chamelon FTP Client
b.) Select Settings.
c.) Select Preferences.
d.) Verify that the choice Retrieve Detailed File Listing is switched OFF.
e.) Close preferences window.
f.) Select Connect to
g.) Under Host write the scanners IP address recorded in step 2, page 15.
h.) Under Password write s5
i.) Select OK

4.) In the Remote window the files on root level of System FiVe will be listed.

a.) Copy the file udd.tar.gz to the pc by using the copy button in the FTP Client window.
b.) Use the arrow that point's to the left, i.e from the scanner to the pc.

15.3.2 Restore Setups

1.) Connect Crossed Ethernet cable and Serial cable to External I/0
2.) Establishing FTP Client Connection To System FiVe

a.) Start Chamelon FTP Client
b.) Select Settings.
c.) Select Preferences.
d.) Verify that the choice Retrieve Detailed File Listing is switched OFF.
e.) Close preferences window.
f.) Select Connect to
g.) Under Host write the scanners IP address recorded in step 2, page 15.
h.) Under Password write s5
i.) Select OK

3.) In the Local window the files on your PC will appear. In the Remote window the files on root level of System FiVe will be listed.

- Copy the file udd.tar.gz from the pc to the scanner by using the copy button in the FTP Client window. Use the arrow that point's to the right, i.e from the pc to the scanner.

4.) Choose from the Front Panel:

a.) Setup
b.) Configuration & Test
c.) GE Service, Password: two passwords may be used; service or setfive
d.) User Defaults
e.) Extract Files
f.) Reboot the scanner and verify that the user defaults have been restored.

15.4 Restoring Laptop Settings

- Restore TCP/IP settings previously modified under the laptop's network control panel, previously recorded in "- Set Laptop IP Address" on page 35.

15.5 FE Alignment

1.) Install a FPA probe in connector 1.
2.) Perform FE alignment, refer to "FE "Calibration" Procedure" on page K16-1
3.) If the FE alignment fails, reboot the scanner and try again.
4.) Reboot system after FE alignment is finished and verify proper operation.

15.6 Setup of EchoPAC and System FiVe for Continuous Capture

Note: For Integrated systems that run Continuous Capture.

1.) On System FiVe, press Setup,
2.) Reenter the setup settings saved in "- Record System FiVe Settings" on page 31.
3.) Under footswitch settings in setup menu reserve footswitch for EchoPAC for all probes.

15.7 System Test

Note: Not all tests are applicable for all system configurations (with/without MAC, with/without Continuous Capture).

Note: You may refer to the "Performance Test (System Test) Procedure" on page K11-1 **when you perform these tests.**

1.) Verify all System FiVe modalities (2D, CFM, Doppler, M–mode etc.)
2.) Verify full–screen switching between Mac and System when depressing EchoPAC key.
3.) Verify VCR record and playback of both System FiVe RGB and EchoPAC RGB.
4.) Verify Color print and B/W print when applicable. (NOTE: It is not possible to print EchoPAC pictures to these printers, unless during playback from the VCR).
5.) Verify System FiVe to EchoPAC digital and video transfer.

15.8 PAMPTE Probe Test Procedure (if site has one)

1.) Power on system (if it isn't already on). Select the PAMPTE probe. It will after selection calibrate the second scan plane position by going to 180 degrees and then back to zero.
2.) Verify that the temperature reading is reasonable (there is no need to do an exact temperature calibration).
3.) Verify that the scan plane can be rotated using the two scan plane control buttons (fast and slow left rotation, fast and slow right rotation).
4.) Verify that the scan plane indicator on the screen is updated when these controls are manipulated.

15.9 Password Options

1.) Enter System Menu
2.) Select Configuration & Test -> Options.

- Yellow indicates *Enabled* Password,
- Grey indicates *Not Enabled* Password.

3.) Verify that the supplied Password corresponds to the System's Serial Number, listed on the screen.

Note: For systems with motherboard Serial Numbers up to 290, the Serial Number must be typed in manually.

4.) Enter the given password to enable the options for the system.

15.10 Paperwork Completion

1.) Complete and return the Product Locator Card.

2.) Leave the Password paper sheets with the customer.

3.) Leave the sw.1.9 CD and the Release Notes (FA040050) with the customer.

SYSTEM FIVE Spare Parts

Overview

Introduction

This part of the Service Manual describes spare-parts for use in SYSTEM FIVE .

Table of Contents

This table gives you an overview for this part of the Service Manual:

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Front Panel Parts	O1-6
Peripheral and MAC Devices	O1-6
Probes	O1-9
Misc. Parts	O1-10
Cables	O1-13

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:O1_01_Parts_i.mnh:03.
Printed: December 5, 2000.

Your Notes:.

Spare Parts – rev. 13

1 Introduction

1.1 Abstract

The purpose with this document is to give a listing of the different spare parts which can be ordered for repair of System FiVe.

1.2 Document History

Rev.	Date	By	Description
01	23 Nov.1994	GRL	First version of document
02	29 Feb.1996	GRL	Minor update
03	12 Apr 1996	GRL	Marked out unsupported probes in V1.1.
04	30 Apr 1997	GRL	Marked out unsupported probes in V1.2
05	30 May 1997	GRL	Added monitor p/n's. Corrected APA and Doppler probe p/n's. Added 128-ch. p/n's.
06	3 Nov 1997	GRL	Added parts for the Elite (low frame) systems
07	23 Dec 1997	GRL	Differenciated parts for Elite and Membership systems (128 ch. systems)
08	10 Jun 1998	GRL	Added some new p/ns
09	9 Nov 1998	GRL	Added parts per V1.5 release
10	7 Apr 1999	LHS	Added parts
11	30 Sep 1999	LHS	Added parts per v.1.8 release. Divided the Parts List in smaller tables. Sorted the descriptions alphabetically.
12	29. Oct. 1999	LHS	Updated per sw 1.7.1 release. Moved the "GEVU Part Number" column from left position to middle. Changed some of the descriptions so the table will be better sorted and easier to use. Some new entries.
13	22. Dec.1999	LHS	Added a Cable and some Covers to the lists. Corrected errors. Updated per sw. v.1.9 release.

Macintosh HD:User:James:@i-arb:Service:S5_ServiceMan:S5_serv_files:O1_02_partlist.13.
Printed: December 5, 2000.

2 Parts List

2.1 Card Rack Boards

Description	GEVU Part Number	Notes
Air Temp. Sense board	FA200255	
Beam Former Board, 2 MLA, BF	FA200001	Obsolete, used with RX, FA20022

Description	GEVU Part Number	Notes
Beam Former Board-2, 1 MLA, BF-2	FA200538	For 128 ch. systems. Use with RX FA522
Beam Former Board-2, 1 MLA, BF-2	FA200811	For 256 channel system Use with RX64-2, FA200777.
Beam Former Board-2, 2 MLA, BF-2	FA200382	For 256 channel systems. Use with RX, FA200638
Beam Former Board-2, 2 MLA, BF-2	FA200765	For 256 channel system Use with RX, FA200776.
Color Flow Processor board, CFP	FA200027	For 256 ch. system
Color Flow Processor board, CFP	FA200409	For 128 ch. system
CPU board	FA200109	
Front End Controller board, FEC	FA200009	For 256 ch. system
Front End Controller board, FEC	FA200669	For 128 ch. system
Front End Controller board, FEC	FA200764	For 128/256 ch. systems
Graphic 5 board, GRAPH	FA200030	
Image Port 2 board, Image Bd 2, IP2	FA200572	
Image Port board, IMPORT	FA200028	
Memory board, IMMEM	FA200110	
Motherboard, MBD	FA200046	
Pipelink Jumper board	AA200138	For test purposes only
Probe Control board, PRC	FA200264	
RF and Tissue processor board, RFT	FA200373	On 256 ch. system: Used with RFP FA200039 or FA200555. On 128 ch. system: Used alone.
RF and Tissue processor board, RFT1	FA200540	For 256 ch. system (p.b. implemented on main board). Replaces FA200373 + FA200039/ FA200555 from Jan 1998.
RF and Tissue processor board, RFT1	FA200574	For 128 ch. system. Replaces FA200373 from Jan. 1998.
RF processor board, RFP	FA200039	Obsolete, used with RFT, FA200373
RF processor board-1, RFP1	FA200555	Used with RFT FA373
RX128 board (AD602)	FA200022	Obsolete. Used with BF, FA200001
RX128 board (AD604)	FA200638	For 256 channel systems. Use with BF FA382
RX128-2 board	FA200907	Improved Power Supply filtering
RX128-2 board (AD604) with mux.	FA200776	For 256 channel system. Use with BF FA382 or FA765.

Description	GEVU Part Number	Notes
RX64 board	FA200522	For 128 ch. systems. Use with BF FA538
RX64-2 board	FA200777	Improved Power Supply filtering
Scan Converter board, SCONV	FA200029	
Spectrum Doppler Proc. board, SDP	FA200026	
Transducer Bus Board, XDBUS	FA200064	
Transducer Controller board, XDCTRL	ML200078	
TX128 board	FA200021	
TX128 v-2 board, TX128-2	FA200999	Replaces FA200021
VME BG/IACK Jumper Board, VME Jumper	FA200075	

2.2 I/O Boards

Description	GEVU Part Number	Notes
ECG/Phono module (Patient I/O Amplifier Board)	FA200194	
External I/O board, EXT I/O	FA200104	
External I/O subassembly	FA200116	
Internal I/O board, INT I/O	FA200103	
Internal I/O subassembly	FA200115	
IV & DP Connector Board	FA200248	
Patient I/O main board	FA200193	
Patient I/O subassembly incl. box	FA200105	
Relay board	FA200020	
Relay board	FA200434	From Mar.1998
Relay board	FA200870	Without APAT support
Relay-2 board	FA200890	Without APAT support
Relay-PAL-Piggyback-2, RLY-PAL-PB2	FA200799	ESD protection. Plugs into FA200870/FA200890

2.3 Power Supplies

Description	GEVU Part Number	Notes
AC Controller board	FA200107	
AC Power supply	FA200231	

Description	GEVU Part Number	Notes
AC Power supply (complete with box)	FA200040	220 V
Card Rack with motherboard subassy.	FA200112	
HV Power supply board	FA200063	
HV Power supply subassembly (box)	FA200114	

2.4 Front Panel Parts

Description	GEVU Part Number	Notes
3" LCD video screen, NTSC	FA200704	For int. MAC
3" LCD video screen, PAL	FA200695	For int. MAC
5.5" LCD RGB monitor, internal	FA200628	Obsolete. For int. MAC.
FP Audio Amplifier board	FA200076	
FP Main board-2	FA200191	
FP Rotary/Display board	FA200057	
FP Rotary/Display board	FA200682	For systems with int. MAC
FP Rotary/Display board-3	FA200989	Systems with 4” LCD screen
Front Cover F/MAC/PAS.I-O/B-W/MO	FB307067	
Front Panel Assembly, complete	FA200045	
Front Panel w/LCD 3”	FA200714	
Front Panel w/LCD 4”	FB200030	
Gooseneck Lamp	058B0060	
LCD Display	058Y4020	(For rotary knobs)
Speaker	160A0005	
Trackball	066C8338	

2.5 Peripheral and MAC Devices

Description	GEVU Part Number	Notes
ATI Card, S-VHS/Video for MAC	066E1043	For int. MAC with C.C.
Bird position sensor box	FA200512	Option.
Computer, Apple PowerMAC 7300, Internal	FA200863	
Computer, Apple PowerMAC G3, Internal	EP200110	Mac for Integrated Systems (-> Dec 1999)
Computer, Apple PowerMAC G4, Internal	EP200125	Mac for Integrated Systems (Dec 1999 ->)

Description	GEVU Part Number	Notes
Computer, Apple, PowerMAC 7300/200	066E0271	For int. MAC
Computer, Apple, PowerMAC 8500/180	066E0275	For int. MAC
Computer, Apple, PowerMAC, G3	066E0277	For int. MAC
Computer, Apple, PowerMAC, G3 350MHz (tower)	066E0278	For int. MAC (-> Dec 1999)
Computer, Apple, PowerMAC, G4	066E0279	For int. MAC (Dec 1999 ->)
Disk for MO-Drive 5.2 GByte	066E0519	
DRAM, 128MByte	512G3640	
DRAM, 32MByte	512G3320	
DRAM, 64MByte	512G4100	
EchoPAC CD	EP200009	
EMC Shield, Hard drive	FA307981	
Ethernet Isolation Box	EP200032	
Ethernet Media Converter	066E0708	
Ethernet TW.PAIR 4 Port HUB	066E0725	
Ethernet, Isolated Kit	EP200100	
Floppies DS/HD3 1/2” MAC	084D0545	
Frame grabber III board	MN200524	For int. MAC with C.C.
Graphic Bd. ATI XCLAIM-VR CV & S-Video Out	066E1043	From Jul 1998 To ---
Graphic Bd. TWIN TURBO 128 MV2 S-Video Out	066E0043	From -------- to Jul 1998
Hard Disk, SCSI, 3.5" Low Profile	066E0525	System software disk, specify SW version.
Hard Disk, SCSI. System-5	066E0526	
ISDN Board	066E0795	Harmonic
ISDN Manager	082B0016	SOFTWARE V4.3
Keyboard Overlay F/MAC G3, ENG	EP314161	
Keyboard Overlay F/MAC G3, FRE	EP314157	
Keyboard Overlay F/MAC G3, GER	EP314159	
Keyboard Overlay F/MAC G3, ITA	EP314158	
Keyboard Overlay F/MAC G3, POR	EP314160	
Keyboard Overlay F/MAC G3, SPA	EP314156	
Keyboard, Apple Design, French	066E0156	
Keyboard, Apple Design, French	EP192018	

Description	GEVU Part Number	Notes
Keyboard, Apple Design, German	066E0155	
Keyboard, Apple Design, Portug.	066E0158	
Keyboard, Apple Design, Spanish	066E0151	
Keyboard, Apple Design, Spanish	EP192073	
Keyboard, Apple Design, US.	066E0154	
MAC OS, English	EP200166	
MAC OS, French	EP200168	
MAC OS, German	EP200167	
MO disk, 2.3 GByte	066E0517	
MO Drive 1.3 GByte 3.5”	066E0672	
MO Drive 5.2 GByte Complete	066E0675	
MO Drive, 2.6 GByte, ext., 5 1/4"	066E0670	For int. MAC. (Inside MAC).
MO Drive, 3.5”	066E0672	
MO Drive, 5,25”	066E0675	
MO Drive, 5.2 GByte, internal., 5 1/4"	066E0671	For int. MAC. (Inside MAC).
Module MAC KEYB/LPT.EXT.	MN200081	
Module RGB Relay Mux	MN200569	
Module, RGB Mux Box	FB200101	
Monitor, 17" Eizo 562 (220V)	066E0017	
Monitor, 17" Eizo T57S (220V)	066E0019	
Monitor, 17" Sony GDM17SE1T (110V)	066E0018	
Printer UP890 MDG 110/220 V, Sony Video printer, B/W	FB108016 (066E0087)	120VAC/220-240VAC
Printer, B/W, Sony UP890CE	MN108454 (066E0089)	220 VAC Use FB108016 (/066E0087) as a replacement.
Printer, B/W, Sony UP890MD	MN108841 (066E0090)	110 VAC, UL approved Use FB108016 (/066E0087) as a replacement.
Printer, Color, Epson Stylus Color 740	066E0400	Stand Alone 220 VAC
Printer, Color, Epson Stylus Color 740	066E0406	Stand Alone 110 VAC, UL approved
Printer, Color, Sony, UP2800P	MN108775 (066E2800)	220 VAC
Printer, Color, Sony, UP2950MD	MN108778 (066E2950)	100-220 VAC, UL approved

Description	GEVU Part Number	Notes
RGB/S-VHS Mux box	MN200574	For int. MAC with C.C.
SCSI Terminator 50P Centronics	066E0770	
SCSI Terminator 50P D-Sub HD.	066E0771	
STK Cable, EchoPAC/S5 Int. Transf.	FA200762	
STK Module Frame Grabber III	MN200524	
Switch, RGBS/SVHS NTSC. Kit,	FA200847	
VCR SVO9500 NTSC (VCR SVO9500MD2 NTSC)	FB100013	(Apr. 1999)
VCR SVO9500 PAL (VCR SVO9500MDP2 PAL)	FB100012	(Apr. 1999)

2.6 Probes

Description	GEVU Part Number	Notes
Adapter for Bird detector	KZ307247	For position sensor
Adapter for Bird detector	KZ307248	For position sensor
APAT, 2.5 MHz, 5 el.	TG100101	
APAT, 3.25 MHz, 4 el.	TK100104	
APAT, 5.0 MHz, 4 el.	TN100119	
APAT, 7.5 MHz, 4 el.	TT100101	
CLA, 3.5 MHz, 192 el.	KK100004	
CLA, 5 MHz, 192 el.	KN100003	
Doppler stand-alone, 2 MHz	TE100024	
Doppler Tc. probe, 2 MHz	KE100001	
Doppler, pencil probe, 6 MHz, Vermont	TQ100002	
Doppler, pencil probe, 6 MHz, Vingmed	TQ100001	
ECLA, 6.25 MHz, 128 el. TV	KQ100002	
FLA, 10.0 MHz, 192 el.	KW100001	
FLA, 10.0 MHz, 192 el. (10 LV)	KW100004	
FLA, 5.0 MHz, 192el.	KN100003	
FLA, 7.5 MHz, 192 el.	KT100001	
FPA, 2.5 MHz, 64 el.	KG100001	
FPA, 3.5 MHz, 96 el. Diasonics	KK100005	
FPA, 3.5 MHz, 96 el. Echo	KK100001	
FPA, 5.0 MHz, 128 el.	KN100001	
FPA, 5.0 MHz, 96 el.	KN100002	

Description	GEVU Part Number	Notes
MPTE, adult multiplan, 5 MHz	TN100053	
MPTE, ped., 7.5 MHz	TN100065	
PAMPTE, 5.0 MHz, Oldelft, 64 el.	KN100007	
PAMPTE, 5.0 MHz, VMS, 64 el.	KN100006	
TE, Mono, Adult, 5 MHz	TN100047	

2.7 Misc. Parts

Description	GEVU Part Number	Notes
Adapter Plate for EIZO T57-S/F56	FA307632	
Air filter	098A0400	Used on systems produced before Nov. 1997
Bird box, mec. subassy.	FA200700	For position sensor
Bracket for hard disk	FA307123	
Bracket for Panasonic AG830 VCR	FA307665	For Premium
Bracket for Panasonic AG830 VCR, top	FA307666	For Premium
Bracket for SCSI Cables	FA307479	
Bracket for Sony UP1800 printer, top	FA307605	For Premium
Bracket, B/W printer, bottom	FA307668	For Premium
Bracket, B/W printer, top	FA307667	For Premium
Brake handle with direction lock	FA307477	
Brake wire for rear wheel locking	FA200530	
Bumper-2	ML307197	For Premium
Cable holder, Elite	FA307616	
Card rack side panel	FA307458	
Cartridge Drawer Hard disk SCSI	066E0531	
Cartridge Frame Hard disk SCSI	066E0532	
Caster, front	098A0103	Obsolete
Caster, rear	FA200167	Obsolete
Chock Absorber for HD	FA307552	4 used for one disk
CONN-DSCREW Lock	064F3008	
Connector cover	FA307136	
Cover f/MAC7300 Opening	FA307748	Oct. 1997
Cover for MO Opening	FB307094	

Description	GEVU Part Number	Notes
Cover for MO-Drive Opening	FA307094	
Cover for P90	FA307772	Jan. 1998
Cover, f/ opening for Bird Receiver Cable	FA307733	Nov. 1997
Cover, for Ext I/O	FA307254	
Cover, for opening, for I/O conn, Elite, Mac	FB307625	
Cover, Front, f/MAC7300/ PASI/O/B/W	FA307747	
Cover, Front, lower	FA307413	
Cover, Front, Supervision, for MAC 7300	FA200748	Oct. 1997. Premium with int. MAC
Cover, Front, Supervision, w/ opening for Pas. I/O, Mac7300, P 90.	FA307749	Nov. 1997
Cover, Front, Supervision, with opening	FA307596	
Cover, left side, lower	FA307138	
Cover, left side, lower	FB307072	
Cover, left side, lower, Elite, Mac	FB307624	
Cover, left side, upper	FA307140	For high frame
Cover, left side, upper	FA307701	For Premium
Cover, left side, upper, Elite	FA307769	For CVP-2950-MD (printer) and AG-MD830E (VCR)
Cover, left side, upper, Elite	FA307771	With opening for CVP-2950-MD (printer)
Cover, left side, upper, w/opening for MD830E	FA307734	Oct. 1997
Cover, left side, upper, w/opening for UP1800EPM	FA307735	Oct. 1997
Cover, left side, upper, w/opening for UP1800EPM and MD830E	FA307662	Oct. 1997
Cover, plastic, bottom, left	FA307237	
Cover, plastic, bottom, right	FA307238	
Cover, plastic, Patient I/O front	FA307407	
Cover, rear, lower	FA307142	
Cover, rear, lower, gray	FA307915	
Cover, rear, upper	FA307141	For high frame
Cover, rear, upper	FA307679	For Premium
Cover, rear, upper, gray	FA307916	
Cover, right side	FA307944	GE Vingmed Silk Screening
Cover, right side, lower	FA307137	

Description	GEVU Part Number	Notes
Cover, right side, upper	FA307139	For high frame
Cover, right side, upper	FA307678	For Premium
Cover, Sony UP1800	FA307413	
Cover, Supervision, for MO disc opening	FA307597	
Cover, top, plastic	FA307130	For high frame
Cover, top, plastic	FA307613	For Elite/Premium
Cover, top, rear	FA307131	For high frame
Cover, top, rear	FA307614	For Elite/Premium
EchoPAC/S5 Transfer Kit ^{w}/ Frame Grabber	EP200007	
EchoPAC/S5 Transfer Kit ^{wo}/ Frame Grabber	EP200008	
Ethernet Media Adapter (for coax)	066E0705	Used externally if connected in a network with coax.
Ethernet Media Adapter (for twisted pair)	066E0708	For int. MAC
Ethernet Noise Filter Ferrite Assy (coax)	FA200460	Used externally if connected in a network with coax.
Fan (single)	098A0050	
Fan module, complete	FA200149	
Flexible cable guide, left	FA307334	
Flexible cable guide, right	FA307335	
Foot Rest	FA307235	
Foot Switch	FA200451	
Foot Switch Box	FA307239	
Gel holder	FA307729	Oct. 1997
Gel holder, System FiVe Elite	FA307681	Oct. 1997
Hub (4 port) for twisted pair	066E0725	For int. MAC
Lock for EIZO T57-S/F56	FA307626	
Locktite, tube	084B2701	Used when mounting Mobility Kit (BT-99)
Mounting bracket, Sony printer	FA307428	
Mounting plate for Sony UP1800 printer	FA307639	For Premium
Mounting plate, monitor pedestal	FA307173	
Mounting plate, VCR	FA307175	
Patient I/O mech. box	FA307127	Premium
Pedestal adapter plate	FA307384	
Pedestal, Monitor	FA200292	

Description	GEVU Part Number	Notes
Peripheral mounting plate	FA307174	
Probe Conn. Mtg./EMC plate	FA307234	
Probe holder with handle, left	FA307817	
Probe holder with handle, right	FA307815	
Probe holder, left	FA307133	
Probe holder, Premium	FA307615	For Elite/Premium
Probe holder, right	FA307132	
Rear bumper	FA307145	
Retaining bar	FA307441	
Retaining bar, guide block	FA200442	
RGB Relay Mux Box 2	FB307089	
Rod, Back	FB307056	
Rod, Front	FB307055	
Shock absorber for hard disk	FA307552	
Support bracket, B/W printer	FA307383	
System SW CD, v1.8	FB200084	System FiVe
Tention Rod Sleeve	FB307042	
Wheel Assembly	FA200636	Large size wheels, rear, with turn.
Wheel Assembly Elite, Front	FA200635	Large size wheels, front
Wheel, Front	FB200044	
Wheel, Rear, Left	FB200045	
Wheel, Rear, Left,	FA200845	Fixed
Wheel, Rear, Right	FA200845	Fixed
Wheel, Rear, Right	FB200046	
Wheels, Rod Between Rear Wheels	FB307003	

2.8 Cables

Description	GEVU Part Number	Notes
Cable Harness, APA Coaxes on RLY bd.	FA200281	
Cable Harness, MAC	FA200864	
Cable Harness, MAC	FB200106	
Cable, ACCTRL	FA200312	
Cable, B/W printer	FA200633	

Description	GEVU Part Number	Notes
Cable, Bird Power	FA200567	For position sensor
Cable, Bird RS-232	FA200568	For position sensor
Cable, Color printer	FA200446	
Cable, Comp. Vid., Ext., LCD3”	FA200694	Aug. 1997
Cable, Comp. Vid., Int., LCD3”	FA200693	Aug. 1997
Cable, DC power for hard disk	FA200386	
Cable, ECG cable for clip on electrodes	164L0036	
Cable, EchoPAC - System-5	FA200528	
Cable, EchoPAC/S5 Transfer	EP200015	
Cable, Ethernet jumper	FA200370	
Cable, Ethernet, EchoPAC I/O	FA200537	
Cable, Ethernet, Patch, 5,00M	070D2950	
Cable, Ethernet, RJ45, 2,00M	070D2901	
Cable, FP Audio On/Off	FA200958	
Cable, FP Control, ext.	FA200081	
Cable, FP Control, int.	FA200078	
Cable, FP Power, ext.	FA200282	
Cable, FP Power, int.	FA200079	
Cable, Ground for HD	FA200792	Mar.1998
Cable, Ground for monitor	FA200507	
Cable, INT I/O HUB AUI	FA200592	
Cable, MAC SVHS Mux Box	FA200796	
Cable, MAC to RGB mux box	FA200773	For MAC 7300 and G3
Cable, MAC to RGB mux box	FA200880	For MAC 8500 only
Cable, MAC to S-VHS mux box	FA200796	For MAC 7300 and G3
Cable, MAC to S-VHS mux box	FA200882	For MAC 8500 only
Cable, Mains, Shielded 1,15M	070C5115	
Cable, Monitor Switch Control	FA200795	For MAC 7300 and G3
Cable, Monitor Switch Control	FA200885	For MAC 8500 only
Cable, Patient I/O ctrl.	FA200634	
Cable, Phono	070M0007	
Cable, Phono mini - BNC	ML200343	
Cable, Power, DC-power	FA200313	

Description	GEVU Part Number	Notes
Cable, Power, HV Supply	FA200318	
Cable, RGB, 1:1	070M0005	
Cable, RGB, Mux Box to Monitor	FA200775	For all MACs
Cable, RGB, Rack to Monitor	FA200256	
Cable, RGB, S5 to Mux Box	FA200774	For MAC 7300 and G3
Cable, RGB, S5 to Mux Box	FA200881	For MAC 8500 only
Cable, SCSI 0,9M	070D3053	
Cable, SCSI 0.9M	070D3049	
Cable, SCSI 1,2M	070D3052	
Cable, SCSI 1,5M	070D3051	
Cable, SCSI for hard disk	FA200387	
Cable, SVHS, Mux Box to VCR	FA200798	For MAC 7300 and G3
Cable, SVHS, Mux Box to VCR	FA200884	For MAC 8500 only
Cable, SVHS, S5 to Mux Box	FA200797	For MAC 7300 and G3
Cable, SVHS, S5 to Mux Box	FA200883	For MAC 8500 only
Cable, Temp Sense and Fans	FA200147	
Cable, VCR ctrl.	FA200155	
Cable, VGA Monitor, 2,00M	070D2910	
Cable, Video	070M0006	

2.9 Labels

Description	GEVU Part Number	Notes
Label for Hard disk	FA314535	
Label, Pedal Functions	FB314040	

Your Notes:

3 System FiVe –REM

Systems covered (GEVU Part Number):

FB008715, SystemFiVe REM,115VAC (FB110) (USA). FB008717, System FiVe REM, 230VAC (FB150)

FB008716, SystemFiVe REM w/Mac, 115VAC. FB008718,SystemFiVe REM w/Mac, 230VAC.

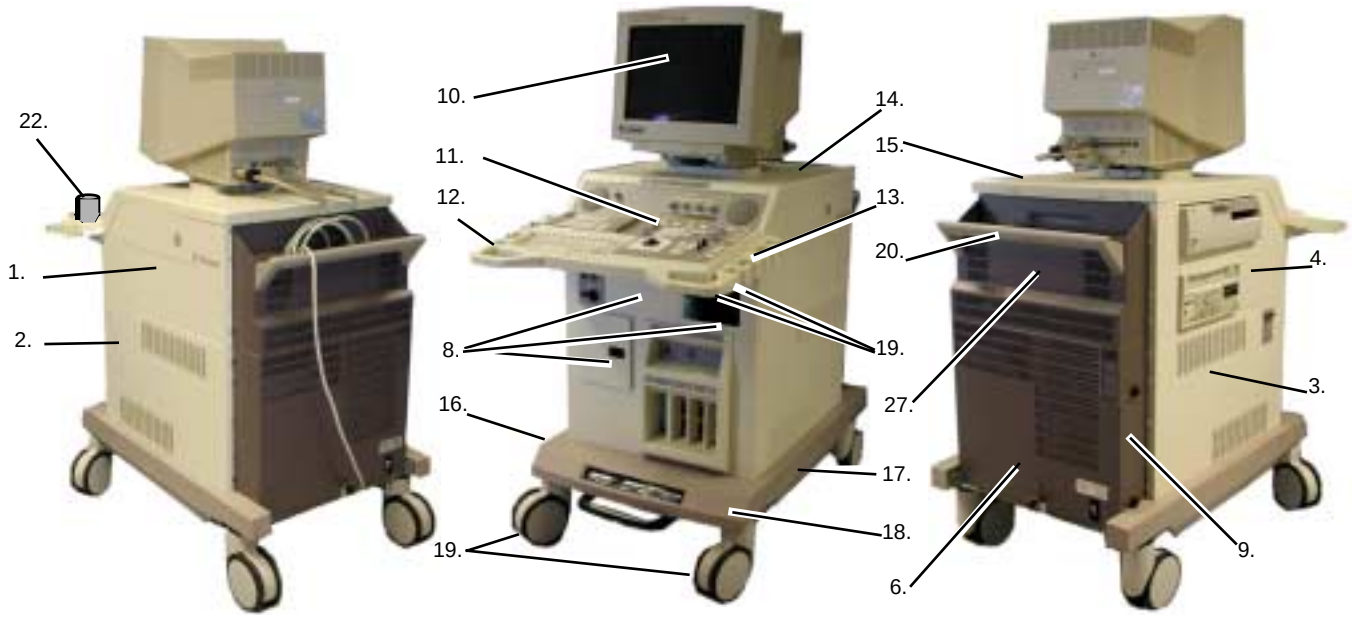

Figure 0-1 Covers etc., System FiVe - 4. REM.

ITEM	Name	FRU	Part Number	Description	Note
1.	RIGHT SIDE COVER, UPPER	2	FA307944	,	BASIC
2.	RIGHT SIDE COVER, LOWER	2	FA307137		
3.	COVER, LEFT SIDE LOWER	2	FB307072		Basic
4.	LEFT SIDE COVER, UPPER	2	FA307946		BASIC
5.	REAR COVER, UPPER	2	FA307916	(DARK GREY)	
6.	REAR COVER, LOWER	2	FA307915	(DARK GREY)	
7.	COVER F/BIRD RECEIVER CABLE	2	FA307733		
8.	FR. COV. F/MAC/PAS.I-O/B-W/ MO	2	FB307067	Front Cover with Opening for Mac, Patient I/O, B-W printer, MO Drive	
9.	COVER F/EXT. I/O	2	FA307917	Cover for External In/Out, Dark Grey	
10.	MONITOR SYSTEM-5 17"	1	066E0019	EIV - T57S	
11.	FRONT PANEL FRONT PANEL W/LCD 4"	1 1	FA200045 FB200176	Front Panel (Complete) Front Panel w/LCD 4"	wo/ EchoPAC option. w/ EchoPAC option
12.	PROBEHOLDER W/HANDLE, RIGHTt	2	FA307815		

Table 0-1 Covers etc., System FiVe - 4. REM.

ITEM	Name	FRU	Part Number	Description	Note
13.	PROBEHOLDER W/HANDLE, LEFTt	2	FA307817		
14.	TOP COVER ELITE	2	FA307613		
15.	TOP COVER, REAR ELITE	2	FA307614		
16.	PLASTIC COVER, BOTTOM, LEFT	2	FA307237		
17.	PLASTIC COVER, BOTTOM, RIGHT	2	FA307238		
18.	FOOTREST, ROUNDED	2	FA307814		
19.	CABLEHOLDER ELITE	1	FA307616		Elite
20.	REAR HANDLE	2	FA307816		
21.	CONNECTOR COVER	2	FA307136		
22.	GEL HOLDER, ELITE	2	FA307681		

Table 0-1 Covers etc., System FiVe - 4. REM.

3.1 Card Rack (Card Cage)

3.1.1 Front End Boards

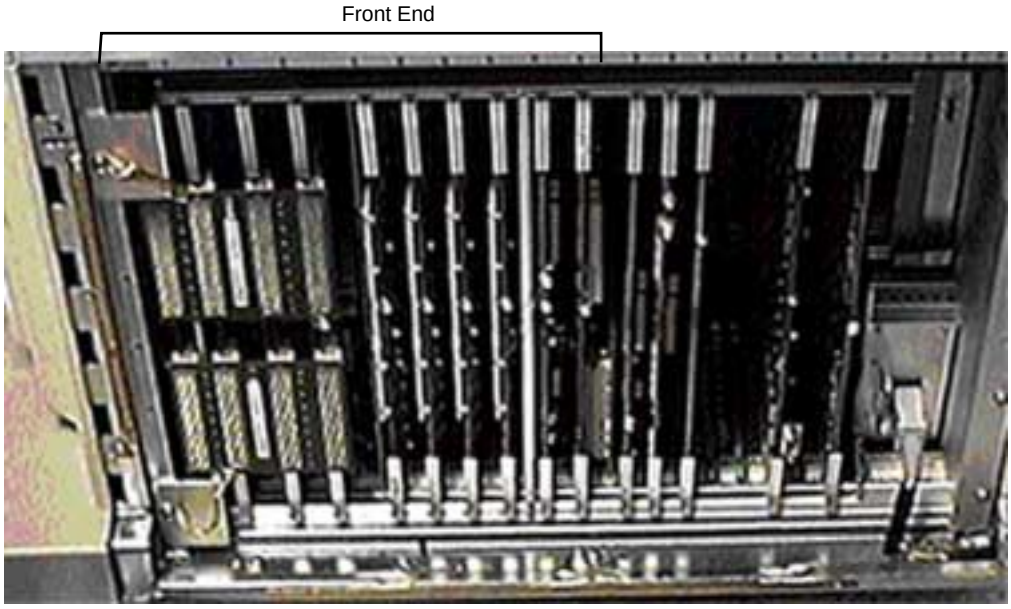

Figure 0-2 Card Rack (Card Cage).

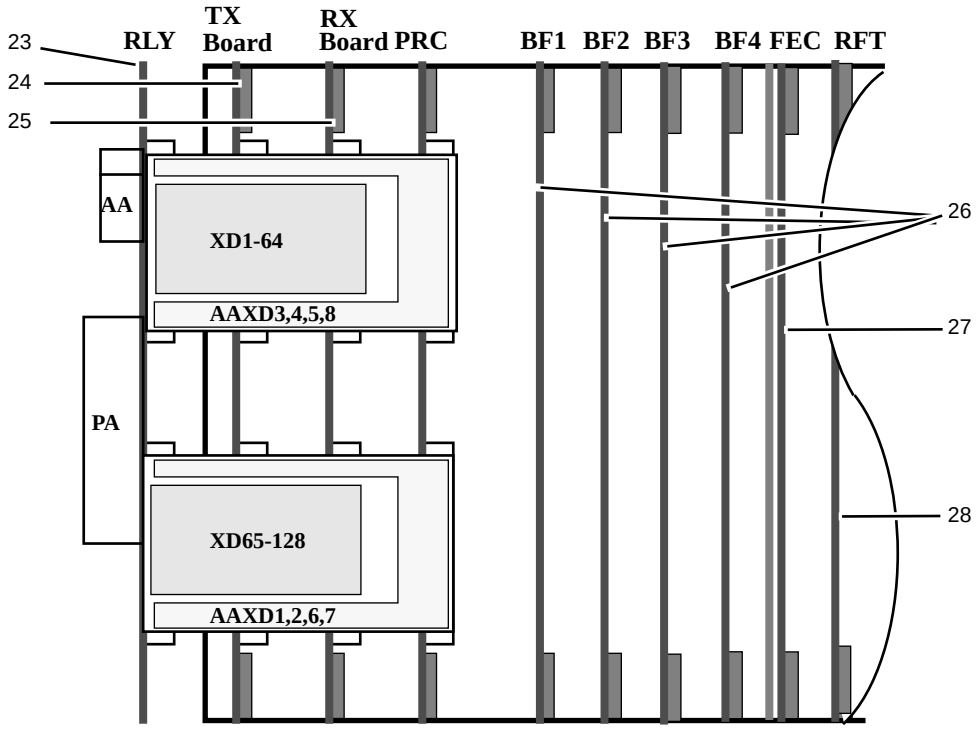

Figure 0-3 Front End (FE) Modules

ITEM	Name	FRU	Part Number	Description	Notes
23.	RELAY BOARD RLY-2 (NO APAT SUPPORT)	1 1	FA200434 FA200890		
24.	TX-128 MAIN BOARD MODULE TX128-I	1 1	FA200021 FA200999		
25.	RX 128 BOARD VER.2	1	FA200907		
26.	MODULE, BEAM FORMER 32	1	FA200765		4 in each scanner
27.	FRONT END CONTROLLER	1	FA200764		
28.	RFT1	1	FA200540		

Table 0-2 Card Rack (Card Cage), Front End Boards

3.1.2 Mid. Processor Modules

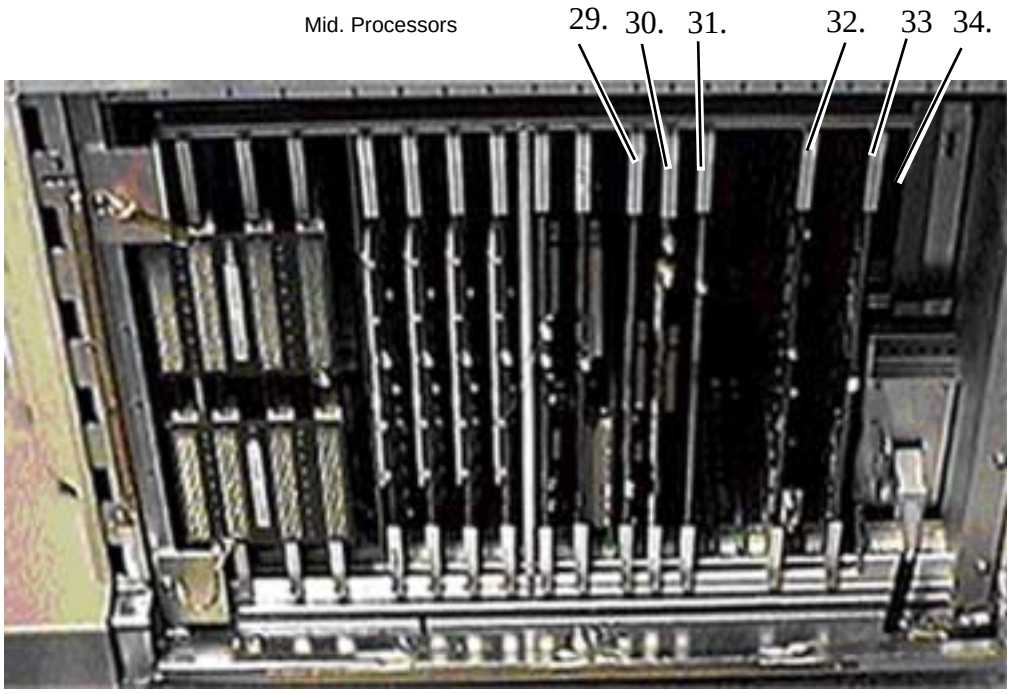

Figure 0-4 Mid Processor Boards.

ITEM	Name	FRU	Part Number	Description	Notes
29.	SPECTRAL DOPPLER PROCESSOR	1	FA200026		
30.	COLOR FLOW PROCESSOR	1	FA200027		
31.	IMAGE PORT 2	1	FA200572		
32.	GRAPHIC-5	1	FA200030		
33.	SCAN CONVERTER	1	FA200029		
34.	CPU BOARD VME 64 SYSTEM 5	1	FA200109	VME 64	SYSTEM 5 x

Table 0-3 Card Rack (Card Cage), Mid Processor Boards

3.1.3 Display and Control Modules

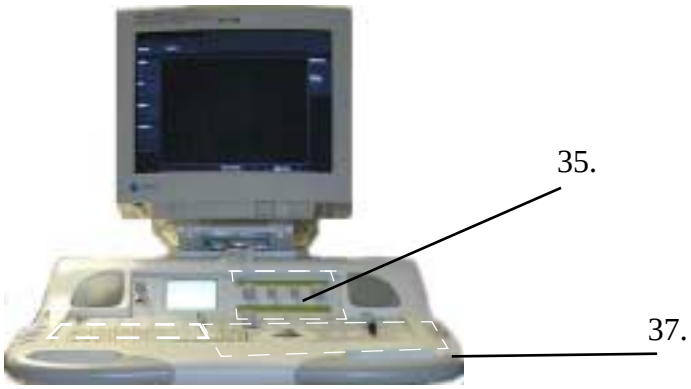

Figure 0-5 Front Panel, Dispaly & Rotary and Main Boards

ITEM	Name	FRU	Part Number	Description	Notes
35.	ROTARY & DISPLAY BD. 4	1	FB200177		
36.	FP ROTARY/DISPLAY BOARD	1	FA200057		
37.	FP MAIN BOARD 2	1	FA200191		

3.1.4 I/O Boards

ITEM	Name	FRU	Part Number	Description	Notes
38.	INTERNAL I/O COMPLETE	1	FA200925		
39.	EXTERNAL I/O COMPLETE	1	FA200926		
40.	TRANSDUCER BUS BOARD	1	FA200064		
41.	IV & DP CONNECTOR BOARD	2	FA200248		
42.	TEMP SENSE	1	FA200255		

3.1.5 Power Supplies

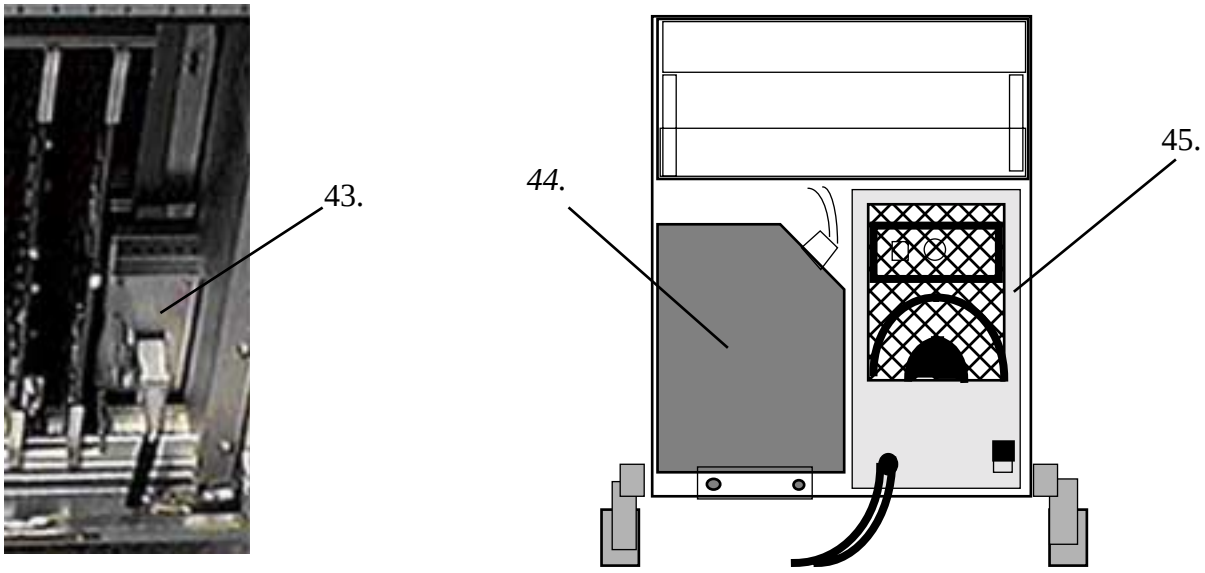

Figure 0-6 Rear end of Card Cage and Rear end of Scanner with Rear Lower Cover removed

ITEM	Name	FRU	Part Number	Description	Notes
43.	AC POWER SUPPLY AC-POWER SUPPLY 115V	1 1	FA200040 FA200231		
44.	DC POWER SUPPLY SYSTEM 5	1	FA200034		
45.	HV POWER SUPPLY SUBASSY	1	FA200114		

3.1.6 Card Cage (Rack)

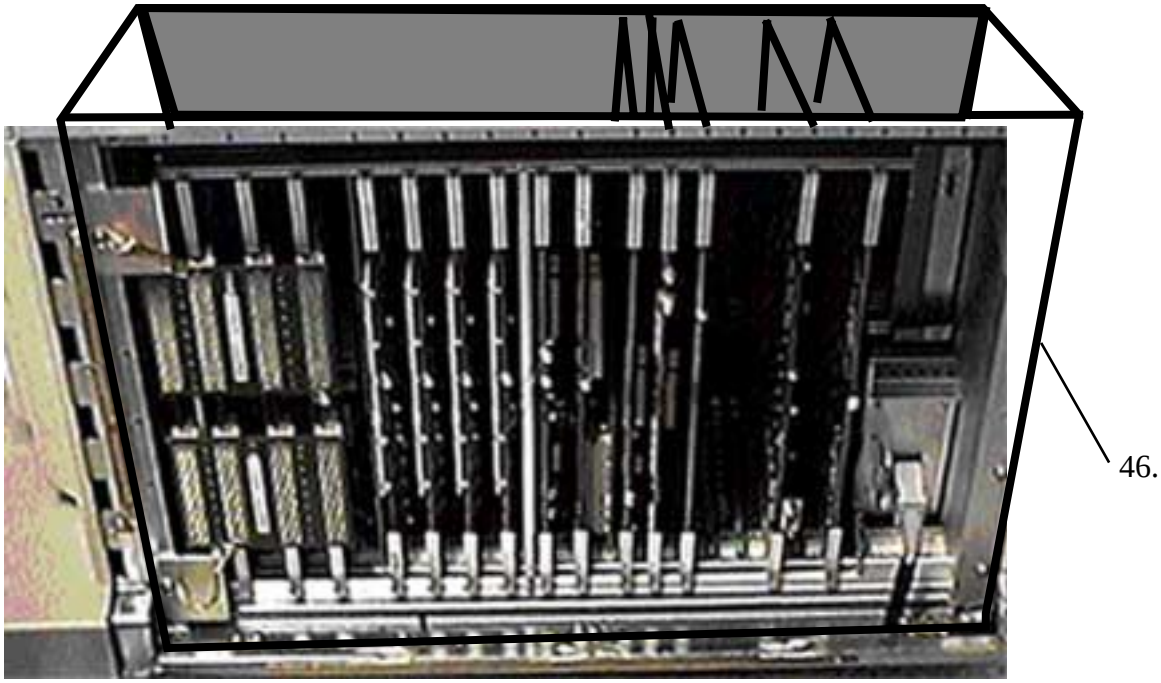

Figure 0-7 Card Rack sketch showing Motherboard

ITEM	Name	FRU	Part Number	Description	Notes
46.	CARD RACK W/MBD SUBASSY	1	FA200112		

3.1.7 Peripheral

Figure 0-8

0.1 Macintosh

Figure 0-9

3.2 Mich. Parts

Figure 0-10

47.ITEM	Name	FRU	Part Number	Description	Notes
48.	BOARD LOCATION LABLE	2	FA314261		
49.	LABEL, CONNECTOR PANEL	2	FA314311		
50.	BRACKET; FP GND, RIGHT	2	FA307549		
51.	BRACKET; FP GND, LEFT	2	FA307551		
52.	CLAMP, MONITOR CABLES	2	MN307136		
53.	RETAINING BAR	2	FA307441		
54.	RETAINING BAR GUIDEBLOCK	2	FA307442		
55.	CABLE PROTECTOR CLAMP	1	MN307260		
56.	SCREW PAN.HEAD M3*6MM	2	080A306B		
57.	QWERTY KEYBOARD SUBASSY	1	FA200360		
58.	KIT, HDD CARTRIDGE + LABEL	1	FB200095		
59.	CABLE ECG CLIP BK/RD/YE	2	164L0036		
60.	PATIENT I/O BOX	2	FA307127		
61.	PATIENT I/O BOX, REDEL	1	FB200143		
62.	INTERNAL I/O BOX	2	FA307304		
63.	EXTERNAL I/O BOX	2	FA307306		
64.	EXTERNAL I/O PANEL	2	FA307307		
65.	PATIENT I/O	1	FA200193		
66.	PATIENT I/O ECG/PHONO	1	FA200194		
67.	BRACKET F/PAS. I/O BOTTOM	2	FA307598		
68.	BRACKET F/PAS. I/O TOP	2	FA307599		
69.	PATIENT I/O FRONT PLATE	2	FA307376		
70.	LOCK F/PATIENT I/O BOX	2	FA307377		
71.	PAT. I/O ISOL. PLATE F.6,3JACK	2	FA307378		
72.	PAT. I/O ISOL. PLATE F. ECG	2	FA307379		

47.ITEM	Name	FRU	Part Number	Description	Notes
73.	CARD RACK TOP COVER	2	FA307459		
74.	LOCK F/ADAPTERPLATE	2	FA307589		
75.	LOCK FOR EIZO T57-S/F5	2	FA307632		
76.	FESTEPLATE FOR HARDDISK	2	MN307805		
77.	BRACKET B/W PRINTER, TOP	2	FA307667		
78.	BRACKET B/W PRINTER, BOTTOM	2	FA307668		
79.	BRACKET F/VCR PANASONIC AG830	2	FA307665		
80.	BRACKET F/VCR PAN. AG830 TOP	2	FA307666		
81.	JORDINGSPLATE FOR KABLER	2	FA307736		
82.	BRACKET, CABLE SUPPORT SVHS	2	FA307759		
83.	MAIN MTG PLATE F/CPV SONY2950	2	FA307766		
84.	SIDE MTG PLATE F/UP2950-MD	2	FA307768		
85.	FOOTSWITCH BOX	2	FA307849		
86.	EIZO CABLE LOCK	2	FA307887		
87.	I/O BOX INTERNAL, CONN. COVER	2	FA307590		
88.	MANUAL,USER MANUAL	2	FA092423	English	System Five
89.	Manuel D'utilisation	2	FA092444	French	System Five
90.	Bedienungsanleitung	2	FA092443	German	System Five
91.	Manual do Usuário	2	FA092998	Portuguese	System Five
92.	Manuale Utente	2	FA092984	Italian	System Five
93.	Användarhandbok,	2	FA092908	Swedish	System Five
94.	Bruksanvisning	2	FA092546	Norwegian	System Five
95.	**UPGRADE MANUALS:**	2	EP284017	Rev A,Upgrade from sw.6.0 to 6.0.x	EchoPAC
96.	**UPGRADE MANUALS:**	2	EP284017	Rev B,Upgrade from sw.6.0.x to 6.1,	EchoPAC
97.	**UPGRADE MANUALS:**	2	EP284017	Rev CUpgrade from sw.4.2 and above to 6.1.1	EchoPAC
98.	INSTALLATION MANUAL	2	EP194010	Rev.A , Sw. 6.1.1,	EchoPAC
99.	INSTALLATION MANUAL	2	EP194010	Rev.B, Sw. 6.2	EchoPAC
100.	INSTALLATION MANUAL	2	EP194010	Rev C. Sw. 6.2.x	EchoPAC
101.	INSTALLATION MANUAL	2	EP194010	Rev.D. Sw. 6.3	EchoPAC
102.	INSTALLATION MANUAL	2	EP194010	Rev.E., Sw 6.3.1	EchoPAC
103.	INSTALLATION MANUAL	2	EP194010	Rev.F., Sw 6.3.2	EchoPAC
104.	Connecting/installation	2	EP294052	Rev.C , Work Station	EchoPAC

3.3 Cables

Figure 0-11

ITEM	Name	FRU	Part Number	Description	Notes
105.	CABLE, FP CTRL, INTERNAL	2	FA200078		
106.	CABLE, FP CTRL, EXTERNAL	2	FA200081		
107.	CABLE, TEMP.SENSE & FAN	1	FA200147		
108.	CABLE, VCR CONTROL	1	FA200155		
109.	CABLE, FP POWER, EXTERNAL	2	FA200282		
110.	CABLE, FP POWER, INTERNAL	2	FA200079		
111.	CABLE, AC-CTRL	1	FA200312		
112.	CABLE; POWER, DC-POWER	1	FA200313		
113.	CABLE, DC POWER SCSI-HD	1	FA200386		
114.	CABLE SIGNAL 1:1 RGB	2	070M0005		
115.	CABLE, MONITOR GND	2	FA200507		
116.	CABLE SHIELDED W/PHONO CONN	2	070M0007		
117.	CABLE MAINS SHIELDED 2,05M	2	070C5205		
118.	CABLE,PHONO MINI/BNC ADAPT	1	ML200343		
119.	CABLE, COLOR PRINTER	2	FA200446		
120.	CABLE, B&W PRINTER	2	FA200633		
121.	CABLE, PATIENT I/O CTRL	2	FA200634		
122.	CABLE, ETHERNET JUMPER	2	FA200370		
123.	CABLE, DC POWER SCSI-HD	2	FA200386		
124.	CABLE, SCSI-HD	1	FA200387		
125.	CABLE SIGNAL SHIELD. VIDEO	2	070M0006		
126.	CABLE MAINS SHIELDED 1,15M	2	070C5115		
127.	CABLE MAINS SHIELDED 1,40M	2	070C5140		
128.	CABLE; POWER, HV-SUPPLY	1	FA200318		
129.	CABLE, RGB, RACK	2	FA200256		

3.4 EMI

Figure 0-12

ITEM	Name	FRU	Part Number	Description	Notes
130.	APAT CONTACT FINGERS	2	FA307416		
131.	EMC SKJERM, HARDDISK		FA307981		
132.	EMC PLATE, LOWER LEFT	2	FA307713		

Abbreviations, Definitions, Glossary, Terminology, Nomenclature

Macintosh HD:User-James:@i-arb:Service:S5_ServiceMan:FA091050_I:Serv_m_I.GLO.fm.
Printed: December 5, 2000.

Numerics

2DF
2D Color Flow Processor Board A3-7, A4-3

A

AA
Annular Array A2-3, A2-15, A2-25, A2-29, A2-40, A2-47

AC
Alternating Current A8-2, A8-6

ACCTRL
AC Controller board K02-2, K03-3, K03-21

ACPWR
AC Power module K03-3, K03-4, K03-21

ADC
Analog to Digital Converter A2-40

Advantage Systems
Same as Premium, except that CLA probes av PAMPTEE probes are optional. 128 channels (128 tx channels, 64 analog rx channels, 64 digital BF channels) H1-2

APAT
Annular Phased Array Transducer A2-11

Aperture
Size of the transducer, with respect to number of wavelengths or in mm. A1-3

Apodization
Weighting of the contribution from elements at the edges in an array transducer. Can be used both on transmit and receive. A1-4

ASIC
Application Specific Integrated Circuit A2-40, A4-17

ATGC
Analog Time Gain Compensation A2-49

AUI
Attachment Unit Interface A1-56

Axial resolution
The ability to separate two neighboring reflectors in the beam direction (vertically). Proportional to frequency. A1-4

B

BA
BEAMADDER ASIC. GE Vingmed's (former Vingmed Sound) custom made Beamforming Circuit A2-40

BF
Beamformer board(s) A2-48, K02-1

BITE
Built In Test Equipment A2-25, A2-29

BW
Black and white A7-8

C

CLA
Curved linear array A2-3

Composite beam
A beam build from data acquired by more than one Xmit, or by more than one MLA. A3-3

Composite Transmit Focus
A vector is constructed from samples from several transmit pulses with different focal points. A1-4

Composite TX-focused beam
A beam build from data acquired by more than one Xmit with different transmit focus. A3-6

Compound scanning
Using linear arrays, an object can be scanned from different directions. By combining the data acquired from these directions, an image with better resolution and finer speckle can be obtained. A1-4

Compression
Amplification of low level echoes and attenuation of high level echoes, so that both can be displayed and visualized at the same time. A1-4

Contrast Resolution
The ability to show a signal from a weak target close to a strong target (also called local dynamic range). A1-4

CPU
Microprocessor board K02-1

CTS
Clear to send A4-17

CW
Continuous Wave (Doppler) A2-29, A3-9, A8-11

D

DC
Direct Current A8-6, A8-9

Depth of Focus
The distance on each side of the focal point where the beam intensity is above a certain number. A1-4

DFT
Discrete Fourier Transform A3-9

DP
Doppler A2-12

DSP
Digital Signal Processor A2-48, A2-53, A3-9, A3-12, A6-3, A6-11

DTXM
Dual Transmitter Module A2-22

Dynamic focus
Tracking of the focus point during receive, from close to far depths. A1-4

E

ECG
Electro Cardio Gram A2-53, A6-5, A6-11

EEPROM
Electrically Erasable Programmable Read-Only-Memory A2-3

Effective Aperture
The projected aperture when angling the beam using phased arrays. A1-3

Elite Systems (High End)
256 channels (128 tx and analog rx channels, 256 digital BF channels). H1-2

EMC
Electro Magnetic Compatibility.

A6-11

Expanding Aperture
The number of elements in the receiver is reduced for shallow depths and gradually increased with depth in order to obtain a uniform focus width throughout the image field. A1-3

EXT I/O
External In/Out K02-1

External I/O
All signals made available to the user at the outside of the system. These signals are galvanically isolated to take care of patient safety. A6-11

F

Far field
The area of the ultrasound beam where it expands beyond the aperture of the transducer. A1-4

FE bus
Front End data bus A4-20

FEC
Front End Controller Board A2-22, A2-40, A2-47, A3-5, A8-11, K02-1, K03-17

FLA
Flat Linear array A2-3

FOC
FOCUSOR ASIC. Vingmed Sound custom made Beamforming circuit A2-40

FPA
Flat Phased array A2-3

FPGA
Field Programmable Gate Array A2-29

Front Panel K02-1

FTC
Fixed Target Cancelling A3-12

G

Geometrical focus
The center of the curvature in a curved transducer. A1-4

GRAPH board
Graphical Processor Board K02-1

I

I
In phase A3-9

I/O
Input/Output signals. A6-11

IMMEM
Image Memory Board K02-1

IMPORT
Image Port board A4-3

INT I/O
Internal I/O board K02-1, K02-2, K03-3, K03-21, K03-22, K04-4, K04-5, K14-2, K15-1

Internal I/O
All signal used of peripherals mounted in the system with power from internal isolation transformer. A6-11

IQ
In phase / Quadrature phase components of complex signal A3-12

IQ-buffer
A data buffer used to transform the input data flow sequence and rate to an output data flow sequence and rate. A3-6

L

LA
Linear Array A2-29, A2-49, A2-60

Lateral resolution
The ability to separate two neighboring reflectors transverse to the beam (horizontally). Inversely proportional to beam width. A1-4

LED
Light Emitting Diode A4-10, A05-3, K04-1, K05-1

LUT
Look-Up-Table A3-12

M

MAC
Macintosh Computer (or computer running the MacOS) K02-1

Main lobe
The area of where the ultrasound beam travels where the signal intensity is within a certain limit. A1-4

Membership (Mid Range) systems
128 channels (128 tx channels, 64 analog rx channels, 64 digital BF channels) H1-2

Mid Range systems
128 channels (128 tx channels, 64 analog rx channels, 64 digital BF channels) H1-2

MLA
Multi Line Acquisition A3-4
Multiple Line Acquisition A2-40

MPTE
Multiplane transesophageal probe A2-15

MSE
Missing Signal Estimation A3-9

Mux
Multiplexer A2-3

N

Near field
The area of the ultrasound beam where its width is less than the aperture of the transducer. A1-4

NTC
Negative Temperature Coefficient A8-4

NTSC
Color television standard used in USA, Japan and in many other countries. A7-2, A7-4

P

PA
Phased Array A2-15, A2-25, A2-29, A2-40, A2-60
Phased array A2-49

PAL
Color television standard used in Europe and in many countries. A7-2, A7-4

Patient I/O box
Patient In/Out box (module) K02-1

PC
Personal Computer (running MS Windows or MSDOS or another disk operating system K02-1

Penetration
A measure for how deep one can visualize structures. A1-4

Performance systems (High End)
256 channels (128 tx and analog rx channels, 256 digital BF channels). H1-2

PLD
Programmable Logic Device A4-10

PRC
Probe Control Board A2-60
Probe Control board A2-12, A2-49
Probe Controller A2-40

Premium Systems (High End)
256 channels (128 tx and analog rx channels, 256 digital BF channels). H1-2

Propagation velocity
The speed of the ultrasound wave through the body. Is different for different types of structure (tissue, blood, fat etc.). A1-4

PW
Pulsed Wave Doppler A3-9

Q

Q
Quadrature phase A3-9

QRS
Characterstic part of the ECG signal A6-5

QRS complex
Characterstic part of the ECG signal A6-5

QRS, QRS complex
Characterstic part of the ECG signal A2-53

R

RAM
Random Access Memory A4-10

Reflector
A plane and large (compared to the wavelength) interface reflecting portions of the transmitted signal back towards the transmitter, straight or in an angle. A1-4

Reverberations
Multiple reflections between materials (e.g. tissue and fat) with different propagation velocity, causing “ghosts”, artifacts and noise in the image. A1-4

RFP
A daughter module that contains optional RF-processing units. A3-3

RFT K02-1
RF and Tissue Processor board A2-48, A3-3, A3-9, A3-12, A4-3

RGB
Red, Green, Blue K03-7

RGBS
Red, Green, Blue, Sync A6-4

RLY
Relay board A2-12, A2-48, A2-59

RPM
Rotations Pr. Minute. A8-2

RTS
Request To Send A4-17

RX
Receive A2-40

RX Board
Receiver board with preamplifiers and TGC amplifiers A2-60

RX128
Receiver board with 128 preamplifiers and TGC amplifiers A2-52

RXD
Receive data A4-17

S

Scatterer
A small object (compared to the wavelength) spreading the transmitted signal in all directions, reflecting a small portion. A1-4

SCL
Serial Clock A2-3

SCONV board
Scan Convertion Board K02-1

SD
Spectrum Doppler (CW or PW) A3-7

SDA
Serial Data A2-3

SDCW
CW Doppler A3-7

SDP
Spectrum Doppler Processor A1-50
Spectrum Doppler Processor Board A2-53, A4-3, A6-4, A6-11
Spectrum Doppler processor board A3-8

Side lobe
Small fields outside the main lobe, caused by the nature of the transmitted signal. A1-4

SP2
Scan Plane 2 (MPTE) A2-15

Speckle
Texture from a homogeneous material (e.g. tissue). Will be finer grained with higher frequency. A1-4

SPST
Single Pole Single Throw (Switch) A2-3

STBY
Stand-by A2-12

T

T/R
Transmit/Receive (Switch) A2-25, A2-29

TE
Trans Esophageal Probe A2-15

Temp
Temperature A8-4

Terminal
Data terminal used for communicating via a RS232 serial line. K02-1

TGC
Time Gain Compensation A2-25, A2-29, A05-3
Time gain compensation A3-6
Time Gain Compensation used in the receiver to compensate for the fact that reflections from larger depths are attenuated more than reflections from shallower depths. A1-4

TPG
Transmit Pulse Generator (ASIC) A2-22
Transmit Pulse Generator chip A2-52

Transducer
A device made of piezoelectric material that will vibrate at its resonance frequency when a voltage is applied to it, emitting a wave. A1-3

TX
Transmit A2-40

TX Board
Transmitter board with 64 or 128 transmitters for phased- and linear array probes A2-48
Transmitter Board with transmitter circuits for phased- and linear array probes A2-60

TX128
Transmitter board with 128 channels A2-20

TXD
Transmit data A4-17

V

VCA
Voltage Controlled Amplifier A2-52

VCR
Video Cassette Recorder A4-3

VME
A bus standard K02-1, K05-2,

K12-1

VME 64 bus
A data bus following the VME standard A4-20

X

XDBUS
Transducer Bus A2-29
Transducer Bus Board A2-59

Xducer Bus Board (Transducer Bus Board) A2-59

Xmit
The actual transmit pulse A3-5

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        40 MHz A/D H4-6
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Printed: December 5, 2000.

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GE Vingmed Ultrasound

SYSTEM FIVE

Service Manual

Part No.:
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