medison

mysono201 ULTRASOUND SYSTEM

SERVICE MANUAL VER 1.0

SERTECH
Service & Technology

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1. What is Mysono201?

- Mysono201 manufactured by Medison Co.,Ltd is the newest subminiature and portable ultrasound system with high resolution, deep transmission and variable function for measurement.
- The several probes such as Curved probe, Linear probe are available for wide usage. Mysono201 can be used in a variety of applications Abdomen, Obstetrics, Gynecology, Vascular, Extremity, Pediatric, Cardiac, Urology.
- Mysono201 offers to excellent image quality, several measurement functions such as a standards distance, area, girth, volume by application for Obstetrics, Cardiac, etc.

2. System constitution

The system consists of main body, monitor, probe, accessory, etc.

[Figure 1.1 Mysono201]

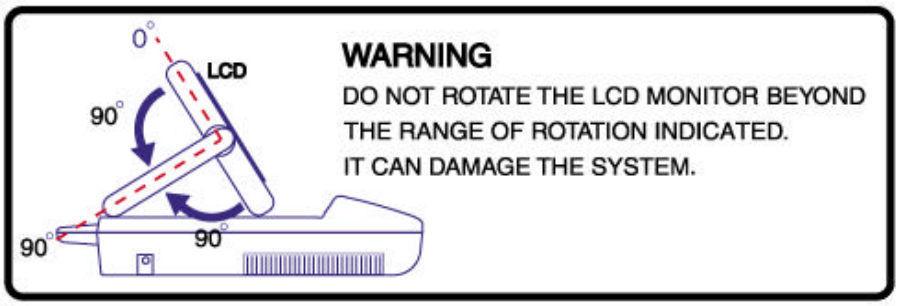
MEDISON or local distributor will make available on request circuit diagrams, components part list, descriptions, calibration instructions or other information which assist your appropriately qualified technical personnel to repair those parts of equipment which are designed by Medison as repairable

2.1 Main body

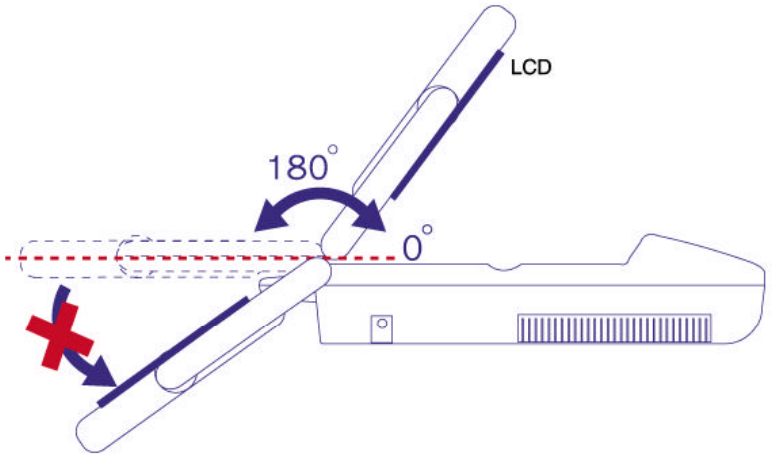
The system is classified by inside for making ultrasound image and by outside for connection to other parts. The housing of system has controllers, probe connector, connector for monitor or other accessories, handle and power switch.

2.2 Monitor

It is TFT LCD Monitor and displays ultrasound image and related information.
It connects to the main body lack of which can control the angle and the height.



[Figure 1.2 LCD Warning]



[Figure 1.3 LCD Warning]

2.3 Probe

Probe generates ultrasound beam and gain the data for display the image.

Probe list and BIOPSY kit available Mysono201 is as follows;

ID	Probe	Biopsy kit	Application
			Mysono201(Human)
12	L4-7CD	BPL-50/65	Small parts(Breast / Thyroid / Testicle), Muscular, Skeletal, pediatric, Peripheral-vascular
13	L5-9CD	BPL-75	Small parts(Breast / Thyroid / Testicle), Muscular, Skeletal, pediatric, Peripheral-vascular
14	L5-9/60CD	BPL-50/65	Small parts(Breast / Thyroid / Testicle), Muscular, Skeletal l, pediatric, Peripheral-vascular
00	C2-5/60BD	Reserved	Abdomen, Obstetrics, Gynecology, Fetal heart
03	C4-7BD	BPC-50	Abdomen, Obstetrics, Gynecology, Fetal heart, Pediatric
04	EC4-9/13CD Vaginal	BPC-65-E/C	Obstetrics, Gynecology, Urology

Human : Image setting, Safety, EMC, AP&I, QA – Total 6 Probe Release.

2.4 Parts

There are supplied with main body.

① Coupling gel
② Power code
③ Power adapter
④ Battery (Option)
⑤ RCA Jack
⑥ Video output cable
⑦ Portable Case
⑧ Operation manual (User guide)
⑨ Smart media (Option) – available hereafter

2.5 Accessories (Option)

It is the optional accessories to connect to the main system. Please refer to supplement OB of user guide.

① B/W Printer
② VCR
③ Non-Interlaced B / W Monitor
④ VGA Monitor
⑤ VHS Monitor
⑥ HMD

3. Safety Precautions

[Notes to users]

Thank you for purchasing the Mysono201 Ultrasound system.

To ensure safe operation and long terms performance stability, it is essential that you fully understand the functions, operating and maintenance instructions by reading this manual before operating your equipment. The system must be operated only by, or under supervision of a qualified person.

"Warning" is used to indicate the presence of a hazard that can cause severe personal injury, death, or substantial property damage if the warning is ignored.

"Caution" is used to indicate the presence of a hazard that will or can cause minor personal injury or property damage if the warnings ignored.

"Note" is used to notify the user of installation, operation, or maintenance information that is important but not hazard related. Hazard warnings should never be included under the Note signal word.

3.1 Safety Precautions

- Classification:
  - Class I equipment with Type BF applied parts
  - Ordinary Equipment
  - Non-AP/APG

- Electromechanical safety standards met:
  _ CSA C22.2 No.601.1, Canadian Standards Association, Medical Electrical Equipment
  - EN60601-1, Second Edition, including Amendments 1 and 2, European Norm, Medical Electrical

- Equipment
  - EN60601-1-2, First Edition, European Norm, Collateral Standard, Electromagnetic Compatibility
  - IEC61157: 1992, International Electro technical Commission, Requirements for the declaration of the acoustic output of medical diagnostic ultrasonic equipment
  - UL 2601-1, Underwriters Laboratories, Medical Electrical Equipment

3.2 Electrical Safety Precaution

It is classified Class I equipment with Type BF applied parts

To ensure user safety, check the following.

WARNING	Never open the system safety cover.; There is a dangerous voltage in system inside. If any repairing or exchanging of parts is desired, ask to the authorized dealer for the service. Do not place the system near of flammable gas or anesthesia gas. It has a danger of explosion. Before using the system, check the housing and the cables. If it has any crack on the housing or wear away on cable, stop to use. Whenever cleaning the system, take off the power code and the battery to avoid the danger of an electric shock. To avoid the danger of an electric shock, use the standard device for digital interface of which achieved IEC certificate. (I.e. IEC60950/EN60950 for the data processing device, IEC60601-1/EN60601-1 for medical device.) For the more, all parts of system meet standard requirement of IEC60601-1-1/ EN60601-1-1. Check whether the peripheral device of input or output port meet standard requirement of IEC60601-1-1/EN60601-1-1 when add it. Do not connect to the system signal in/outlet and the patient at the same time. It is for preventing to leakage current caused by over the maximum permissible range.

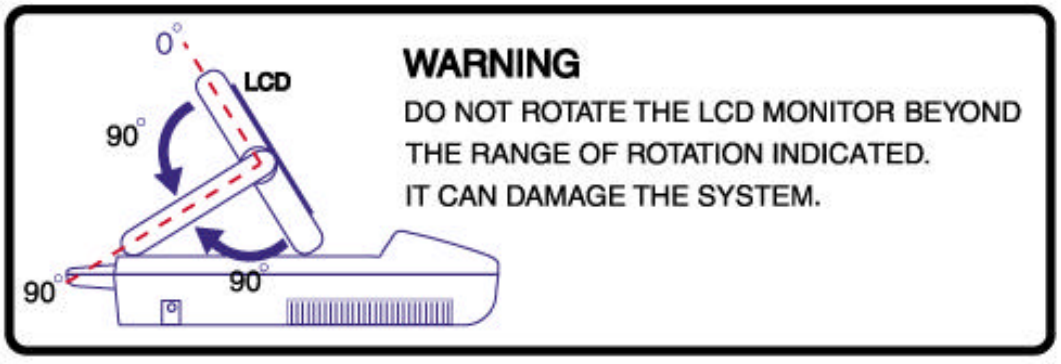
CAUTION	Even though the system passed the test of EMI/EMC standard, it could be down the image quality or could damage the system under using magnetic filed. If you have a poor image or image problem, check whether the source of electromagnetic waves is near of the system or not such as Mobile phone, Pager, Radio, TV or Microwave machine. Please move them far from the system or move the system from affected zone of electromagnetic waves. Electrostatic discharge (ESD) is a shock occurred by Static electricity and a phenomenon in nature. ESD occurs in dry condition such like under using heater or air conditioner. The static electricity occurred by a user or a patient can affect to the system or the probe sometimes. To prevent this problem, please be well aware as follow. : - Spray the prevent of static electricity spray to carpet or Linoleum - Use met for protection of static electricity - Connect a ground between the system and table or bad for patient

3.2.1 System care

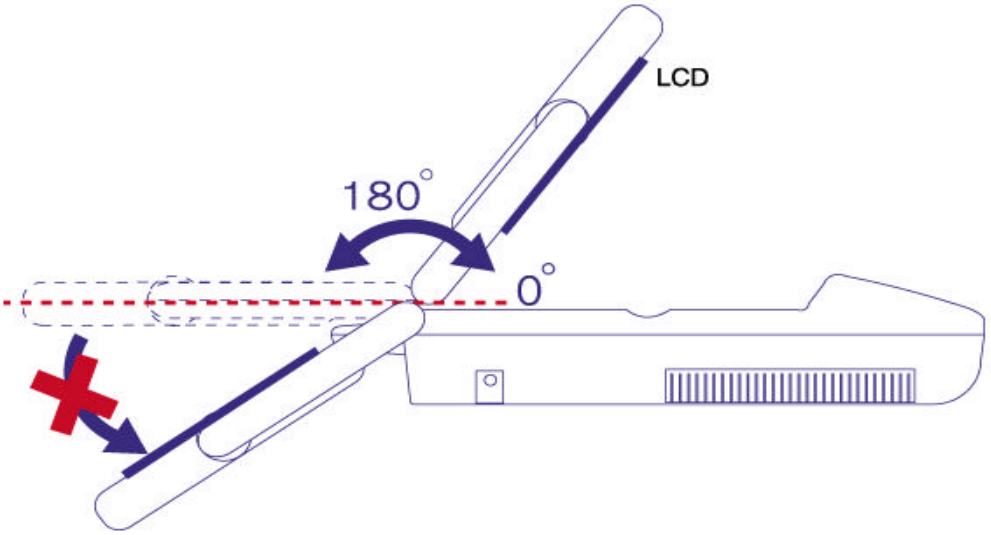
Check the following.

CAUTION	In case that tie too much or twist the probe connected with patient, system could be wrong work. Wrong cleaning or sterilization of the parts connected with patient is dangerous. Refer to “3.4 Maintenance & Cleaning” in this manual. Do not soak the cable in liquid. It cannot prevent flood. Do not use strong solvents such as thinner or benzene, or abrasive cleansers. Since these will damage the cabinet. In general, only treat with waterproof on the ultrasound lens part (Safety grade: IPX7). Do not soak the probe in liquid except the special case with cleaning guide. Do not turn the system off under store the image. That will damage the memory inside. Turn the system off when remove the probe form the system or connect it to the system. Do not keep the system over one hour with close LCD monitor under the system is working. That will damage the keyboard.

WARNING	The turning radius is limited to suitable use. If it is over the limitation, that will damage LCD monitor.



[Safety Figure1. Warning for LCD angle]



[Safety Figure2. Warning for LCD angle]

3.2.2 Battery

Keep in mind the warning and caution to prevent explosion, heat or smoke generation in battery.,

WARNING	Do not disassemble or modify the battery. Keep the circumstance temperature condition when using the battery. - Charge: 0^{O} ~ 45^{O} C - Discharge: -10^{O} ~ 60^{O} C Do not short between terminals of battery. Do not use the battery under the circumstance like as fire, moisture. Do not charge the battery where is near of fire or heater. Keep out of the sun when keep the battery. Keep out the sharp material to face with battery and do not deliver the shock directly to it. Take away the battery from the system when do not use it for a long time.

CAUTION	Do not use the battery except supplied by Medison Do not use a battery except made by Medison. Do not charge a battery with non- allowed method. (Don't use other charge method) Keep a battery from moisture. If smell or burn under using battery, discontinue use of system prompt, remove a battery. Keep the battery under the circumstance temperature -20^{O} ~ 50^{O} C. System working condition and a number of charge/discharge times of battery affect to time of charge/discharge. Medison guaranty the battery during 6 month (battery capacity 50%).

3.2.3 Safety Symbols

The international Electrotechnic Commission (IEC) has established a set of symbols for medical electronic equipment that classify a connection or warm of any potential hazards. The classifications and symbols are shown below.

Isolated patient connection (IEC 601-1-Type BF)

Power Switch represent ON and OFF, respectively.

This symbol identifies a safety note. Ensure you understand the function of this control before using it. Control function is described in the appreciate operation manual.

Output port or Parallel port of VGA

Output port of VHS

Non-interlaced B/W Printer port

Printer remote output port

Humidity protect

3.3 Physical Safety Precaution

WARNING	If you have experienced any trouble with the equipment, switch it off immediately, and contact to Service center or its authorized dealer for assistance. Do not use the system under working wrong or trouble. Non-continuous scanning is caused by hardware problem. It must be repaired. The using of Ultrasound always needs a careful attention. Under the principles of ALARA, energy delivered should be "as low as reasonably achievable" to perform study. Read the explanation about biopsy before using it. Refer to user explanation parts of probe an appendix. Certify biopsy Needle before using it. Do not use curved needle.

ALARA TRAINING PROGRAM

Ultrasound is considered safe at low clinical levels. At high levels and longer exposures, however, its safety is not completely understood. For this reason, always exercise caution when exposing patients to ultrasound. Always use the lowest transmit power levels.
And minimize time of exposure. Under the principles of ALARA, energy delivered should be "as low as reasonable achievable" to perform your study.

The following is a public statement by the one of United Stated Ultrasound Association, AIUM, on the safety of ultrasound diagnosis.

Ultrasound has been in use since the 1950's. AIUM declares the clinical safety of ultrasound scanning and acknowledges its effectiveness as the type medical equipment and its possible use for diagnosis of pregnant women.
There has been no case which shows cause of any physical damage to either patient or user during properly performed diagnosis with an ultrasound scanner. Although it might be possible that unknown effects of ultrasound may come to light in the future, so far the benefits far outweigh any unproved danger. Theoretically, there are two possible ways that ultrasound could have negative affect on the human body.
One is the heat generated by ultrasound as it passes through the human body. Doppler produces the most heat, and it followed by color and B-mode imaging. However, even in the case of Doppler the amount of heat is so minor that there is no equipment that can measure it.
The other one is the possible formation of a cavity by the ultrasound. However, there has been no clear evidence that this can actually occur in the human body.
In conclusion, no negative biological effects of ultrasound have been proven thus far.

3.4 Maintenance and cleaning

WARNING	Whenever maintain or clean the system, turn off the power and remove the plug from the power supply. (Remove the battery from the system, too)

3.4.1 Probe

WARNING	Always use protective eyewear and gloves when cleaning and disinfecting probes and Biopsy guide adapter.

CAUTION	Probes must be cleaned after each use. Cleaning the probe is an essential step prior to effective disinfection or sterilization. Be sure to follow the manufacturer's instructions when using disinfectants. Do not allow sharp objects, such as scalpels or cauterizing knives, to touch probes or cables. When handling a probe, do not bump the probe on hard surfaces.

Probe is very important part to judge the image quality. The optimum image can display under using the correct probe.

3.4.1.1 Cleaning

CAUTION	Do not use lacquer thinner ethylene oxide or any other organic solutions, as these can destroy the membrane of the probe. Do not use a surgeon's brush when cleaning probes. The use of even soft brushes can damage the probe. During cleaning, disinfection, and sterilization, orient the parts of the probe that must remain dry higher than the wetted parts until all parts are dry. This will help keep liquid from entering non-liquid-tight areas of the probe.

1) Disconnect the probe from the system.
2) Remove any sheaths, biopsy guide adapters, or biopsy needle guides (biopsy guide adapters are re-usable portion of the biopsy guide and can be sterilized.)
3) Discard sheaths (sheaths are single-use item)
4) Use a soft cloth lightly dampened in a mild soap or compatible cleaning solution to remove any particulate matter or body fluids that remain on the probe or cable.
5) To remove remaining particulates, rinse with water up to the immersion point.
6) Wipe with a dry cloth; or wipe with a water-dampened cloth to remove soap residue, and then wipe with a dry cloth.

3.4.1.2 Sterilization

Apply this sterilization way to EC4-9/13CD probe only.

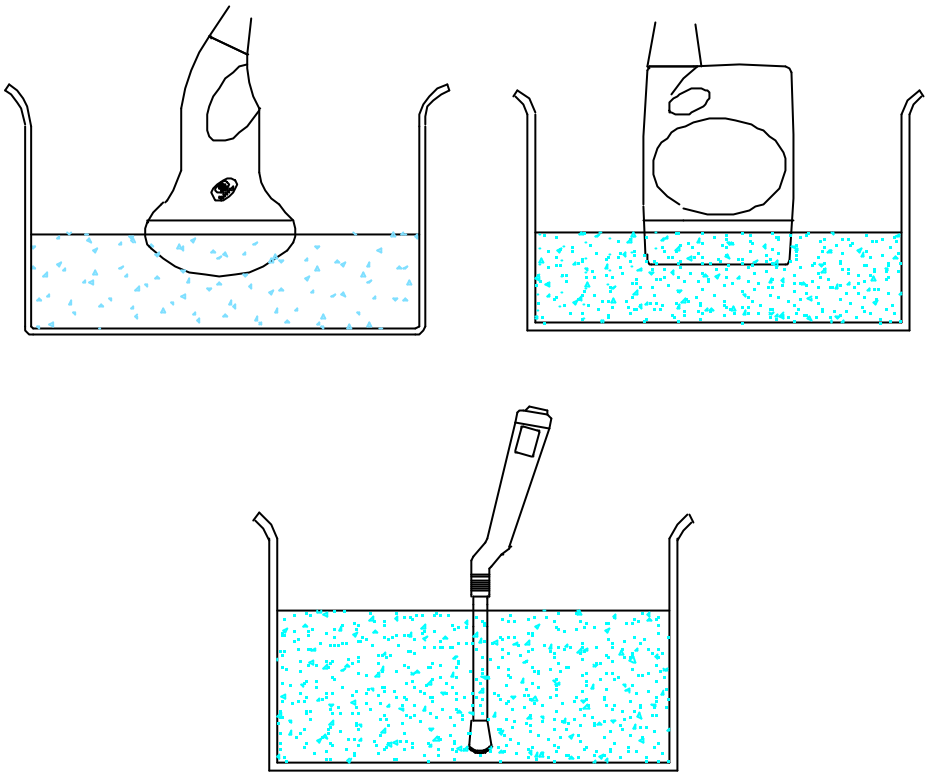
A 10^{-6} reduction in pathogens should be reached following the sterilization procedures in this manual and using the following MEDISON recommended solutions. The following disinfectants are recommended because of both its biological effectiveness (as qualified through the FDA 510(k) process) and its chemical compatibility with MEDISON ultrasound product materials.

Solution	Country	Type	Active ingredient	FDA 510(k)
Cidex	USA	Liquid	Gluteraldehyde	K934434

WARNING	If a pre-mixed solution is used, be sure to observe the solution expiration date. The level of disinfection required for a device is dictated by the type of tissue it will contact during use. Ensure that the solution strength and duration of contact are appropriate for disinfection or sterilization. Be sure to follow the manufacturer's instructions. In neurosurgical application, sterilized probes should be used with a pyrogen-free sheath.

CAUTION	Using a non-recommended disinfection solution, incorrect solution strength, or immersing a probe deeper or for a period longer than recommended can damage or discolor the probe and will void the probe warranty. Do not immerse probes longer than one hour, unless they are sterilizable. Probes may be damaged by longer immersion times. Sterilize probes using only liquid solutions. Using autoclave, gas(EtO), or other non-MEDISON-approved methods will damage your probe and void your warranty.

7) Mix the disinfection solution (or sterilization solution, for sterilizable probe) compatible with your probe according to label instructions for solution strength. A disinfectant qualified by the FDA 510(k) process is recommended.
8) Immerse the probe into the disinfection solution (or sterilization solution, for sterilizable probe) as shown in the figures below for your probe.
9) Follow the instructions on the disinfection (or sterilization, for sterilizable probe) label for the duration of probe immersion. Do not immerse probes longer than one hour, unless they are sterilizable.
10) Using the instructions on the disinfectant or sterilization label, rinse the probe up to the point of immersion, and then air dry or towel dry with a clean cloth (or a sterile cloth, for sterilizable probe).
11) Examine the probe for damage such as cracks, splitting, fluid leaks, or sharp edges or projections. If damage is evident, discontinue use of the probe and contact your customer service representative.



3.4.2 Biopsy guide adaptor and Needle guide

The reusable external surface of biopsy guide adaptor can sterilize under the condition as below. It is possible to reduce the pathogens up to 10^{-6} as following process.

WARNING	Gloves and safety mask should be worn during cleaning and sterilizing the probe and biopsy guide adapters.

CAUTION	Biopsy guide have to clean after using. It is very important process. When using the disinfecting solution, follow the user guide published by manufacturer. Keep out of the sharp things such like a mess for a surgical operation. Be careful to avoid striking the biopsy guide with hard material.

3.4.2.1 Cleaning of the stainless biopsy guide

1) Take off the biopsy guide assembly parts from the probe after using.
2) Disassemble the biopsy guide parts each one.
3) Remove an alien substance still remained on each part using by small brush and water.
4) Rinse it with water to remove again an alien substance.

3.4.2.2 Sterilizing of the stainless biopsy guide

Sterilize it by using an autoclave or Ethylene Oxide.

1) Complete the following process after sterilization.
2) Check the biopsy guide adaptor whether it has a crack, division, or any other damage on it. If there is some damage, stop to use and contact to Medison service agency or its authorized local service agency.

3.4.2.3 Cleaning of plastic biopsy guide

Take off the biopsy guide assembly parts from the probe after using.

1) Disassemble the biopsy guide parts each one. The consumable parts cannot sterilize.
2) Remove an alien substance still remained on reusable part using by small brush and water.
3) Rinse it with water to remove again an alien substance.

3.4.2.4 Sterilizing of plastic biopsy guide

CAUTION	Sterilize only a chemical pasteurization at a low temperature. It can get the permanent damage by sterilization using autoclave, gas or radioactivity.

4) Sterilize it by using a chemical pasteurization at a low temperature approved by FDA 510(K). Check the time (normal 10 hours) and the temperature of solution.

It is a biologically, chemically suitable disinfecting solution approved by FDA 510(k) in U.S.A.

Solution	Country	Type	Active ingredient	FDA 510(k)
Cidex	USA	Liquid	Gluteraldehyde	K934434
Cidex Plus	USA	Liquid	Gluteraldehyde	K923744

5) Complete the following process after sterilization.
6) Check the biopsy guide adaptor whether it has a crack, division, or any other damage on it. If there is some damage, stop to use and contact to Medison service agency or its authorized local service agency.

3.4.3 Surface of system

Follow as below..

WARNING	Gloves and safety mask should be worn during cleaning and sterilizing the surface of system.

CAUTION	Use only the solution recommended by Medison.

3.4.3.1 Cleaning

1) Turn the system off and then remove the plug from the power source.
2) Use a soft cloth lightly moistened with a mild soap or detergent solution to clean the system surface.

3.4.3.2 Sterilization

3) Use a disinfecting solution with suitable concentration recommended by user guide. Medison recommend the solution approved by FDA 510(k) in U.S.A.
4) Check the using time and the concentration of the solution as following the caution on the label.
5) Dry it with a soft sterile cloth.

4.Installation of Mysono201

4.1 Connecting and removing the probe

The system has only one probe connector.

- How to connect the probe

1) Connect the probe to the probe connector located at the right side of the system.
2) Turn the locking lever on the probe connector clockwise to fix the probe.

- How to remove the probe

1) Turn the locking lever on the probe connector counter-clockwise to remove the probe.
2) Take off the probe from the system.

4.2 Connecting and removing the battery

It is optional part to supply the battery.

- How to connect the battery

1) Remove the cover of battery connector located at the bottom of system by pushing forward outside.
2) Insert the battery to the battery connector by matching the bottom of the battery and the system. After fixing the location of the connector pin between the battery and system, press it softly until complete the connection.
3) After complete connection, close the cover of battery connector of the system.

- How to remove the battery

1) Turn off the system power.
2) Remove the cover of battery connector located at the bottom of system by pressing forward outside.
3) Take hold of the battery handle and lift it slightly. Then push it forward outside of the system.
4) After remove the battery, close the cover of the system battery connector.

4.3 Charge and discharge of the battery

The battery has to charge before using.

- How to charge the battery

1) Insert the battery as how to connect the battery
2) Connect the system and AC adaptor supplied with the system. Refer to [appendix 0b. connecting the peripheral device] in user manual.
3) The battery is charging during AC adaptor connecting.
   It is possible to charge under the state both the system on and off.

In case of the system on, it takes about 5 hours to charge.

In case of the system off, it takes about 3 hours to charge.

If need a more information of the time for charge or discharge, refer to [Appendix C. System specification] in the user manual.

Check the battery state by LED color on the system during charging.

- Without Battery: No Color
- Under charging: Orange
- Complete charging: Yellow
- Take off the adaptor: Red

Discharge the battery

When the battery is discharged (the system is working without AC adaptor), the system power will be compulsorily turned off after a period of time (90 minutes) for safety and efficiency of battery and user will hear the warning “beep” sound every 10 seconds.

4.4 Power ON / OFF

Hold the pressing the power switch located at the left side of the system for minimum 1sec. whenever turns on/off the system. It is to prevent the system down and battery discharge.

- How to turn on the system

1) Hold the pressing the power switch for minimum 1sec. with connecting the AC adaptor or inserting the charged battery.
2) Check the image display on the monitor.

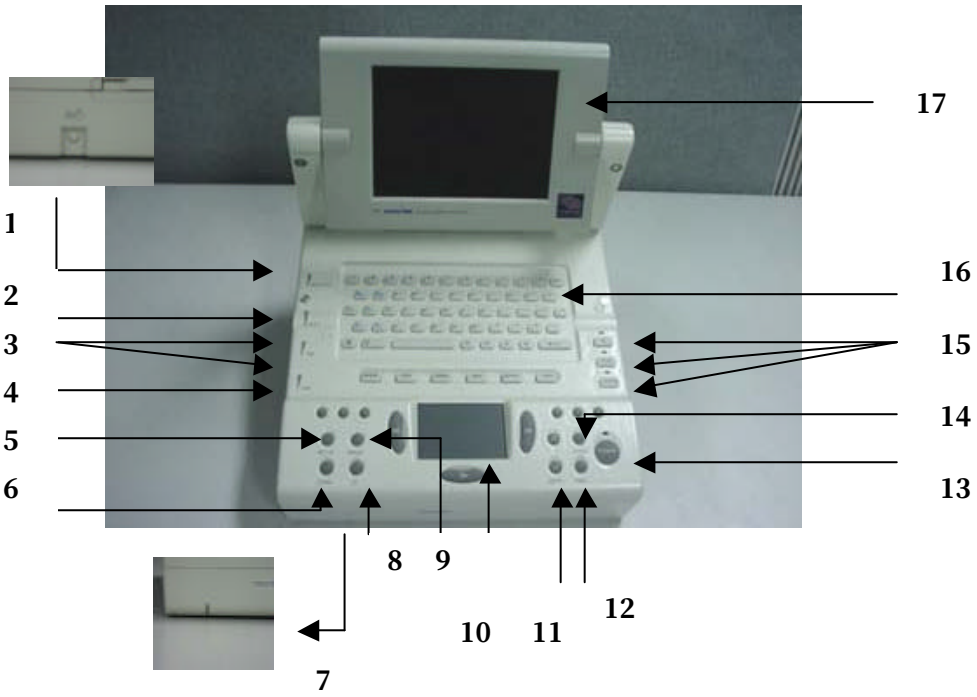
- How to turn off the system

1) Hold the pressing the power switch for minimum 1sec.
2) Check the image disappears on the monitor and switch off.

4.5 Using AC adaptor

It takes about 5 hours to charge completely under connection of AC adaptor to the system.
Refer to [Appendix 0b. connecting the peripheral device] in user manual.

5.Mysono201 Function



No.	CONTROLS	DESCRIPTION
1	Power switch	Turns power on / off → about 1 sec.
2	Brightness	Control the Brightness of LCD monitor. Turn it to clockwise for brightness Turn it to counter-clockwise for darkness
3	Near / Far	Use either Near dial or Far dial When control the Near gain, use Near dial When control the Far gain, use Far dial
4	Gain	Control the image gain Turn it to clockwise for increasing the gain Turn it to counter-clockwise for decreasing the gain
5	Set-up	Change the mode into set-up
6	Clear	Delete the value on the image area such as Text, Body Marker, Indicator, measured value, etc.
7	Battery LED	Display the status of Battery. Disconnect the Battery: No Color Charging the battery: Orange Full charge: Yellow Remove the battery adapter: Red
8	GA	Measure GA(Gestational Age)

No.	CONTROLS	DESCRIPTION
9	Measure	Mode for measuring of distance, volume, circumference, etc.
10	Touch pad	Touch pad
11	Depth	Control the image depth. Up key for shallow depth of the image Down key for deep depth of the image
12	Printer	Print the indicated image.
13	Store	Save the present image on the monitor. It is possible to check the saved image by using I-View. And can be back up by using smart media. (This function will be added in the future.)
14	Freeze	ON/OFF the image scan. Cine function, the image saving, printing or measuring is available under freeze. But the image saving is available only 2D mode.
15	2D/SYN, M, DUAL	Control knobs to select the image mode 2D/SYN: To 2D mode, press it one time. To Synthetic mode, press it again under 2D mode. M: Change 2D/M by pressing this button. Display 2D image on the left side of the monitor and M mode image on the right side of the monitor. Change only M mode by pressing again this button under 2D/M mode. This button works as toggle button between 2D/M and M mode under M mode. Dual: Change Dual mode. It works as alteration to left/right of activated Image.
16	Key board	Use it when input the text or set the image.
17	LCD monitor	Display most of information for using such like a ultrasound image, data, user menu, etc.

Mysono201 P/M Check List

Date: Distributor:

Hospital		System Serial	
Customer		S/W Version	
Address			
Tel. no		Warranty	

Instructions :

This information is for warranty check. Please fill up all items.

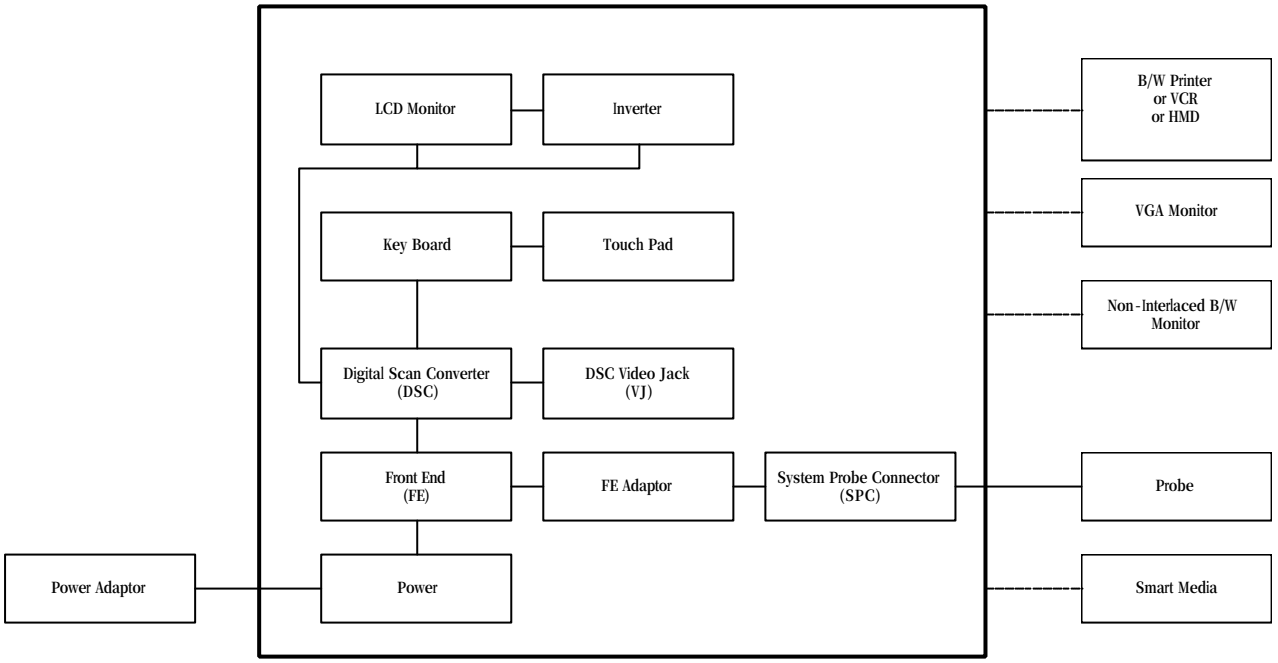
Items	Good	Bad	Remarks
Ⅰ. Check the packing items (compare with packing list)	☐	☐	
Ⅱ. Condition of system housing	☐	☐	
Ⅲ. Probe condition	☐	☐	
A. Functional operation & test (system initialization state)			
1. System works well when power on.	☐	☐	
2. Monitor TEST	☐	☐	
3. Key Board TEST	☐	☐	
B. Probe test (each probe)			
1. Check the probe shape	☐	☐	
2. Knife TEST	☐	☐	
C. Operational Mode Tests			
1. 2D Mode/SYN	☐	☐	
DUAL Mode	☐	☐	
M Mode	☐	☐	
2. Measurement TEST	☐	☐	
D . Electrical Test & Calibration			
1. Power Supply	☐	☐	
2. System Calibration	☐	☐	
3. Power Cord/Plug and 110/220 switch	☐	☐	
E. Mechanical operation			
1. Circuit boards, plugs, jacks, and connectors seated	☐	☐	
3. Seating & connection of cables & cords to peripherals	☐	☐	
F. Echo printer, External monitor, Multi-form camera, VCR	☐	☐	

When you finish filling all up, please send this sheet to Medison by fax or air mail.

Confirmation Signature

Service agency: Customer signature

1. System Block Diagram



System Bolck Diagram

2. Front-End Board (F/E)

2.1 General Description

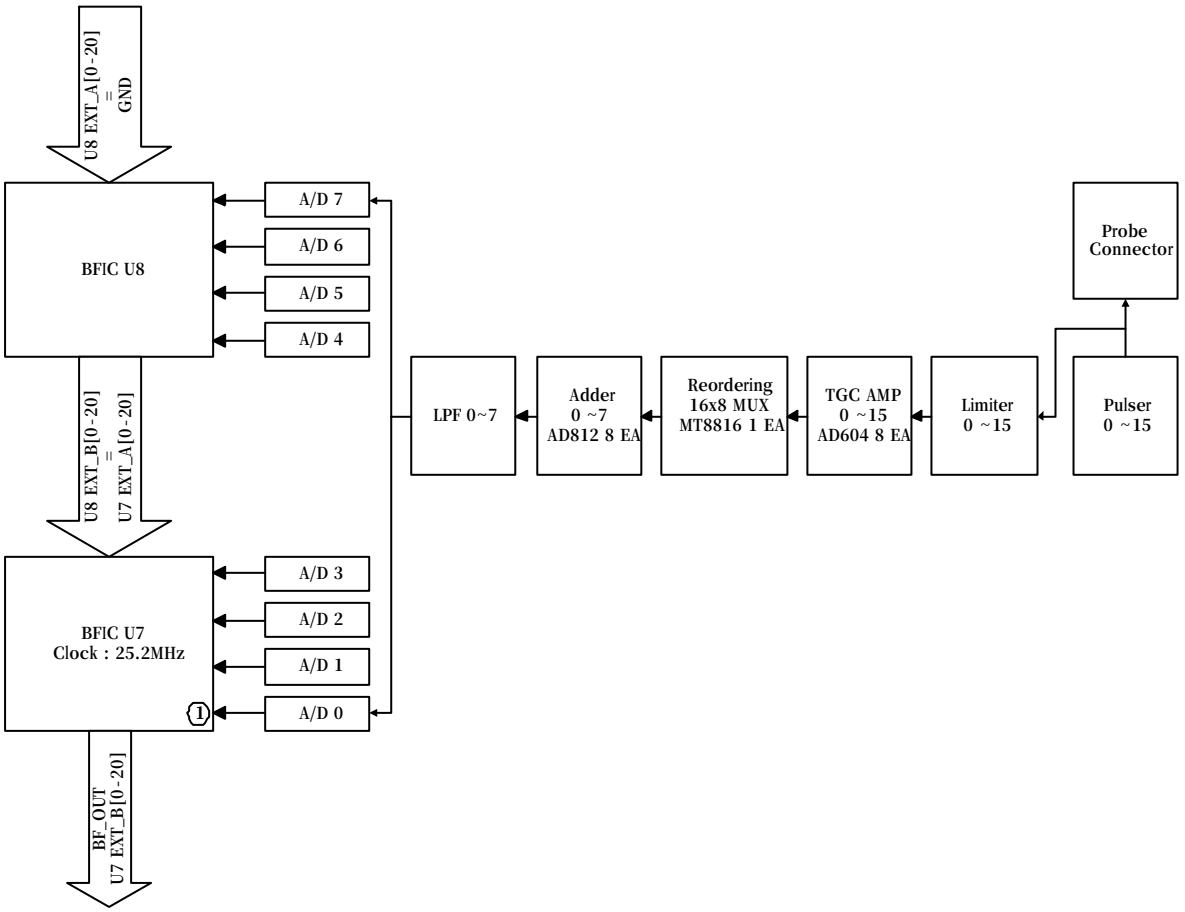
F/E board receives the echo signal of ultrasound and the signal clamps the high voltage to +/- 0.6 V by Limiter then pass through TGC Amp. And then it reordering and its signal path is reduced in half by OP Amp Adder that add the Symmetrical signal per scanline.

Then, to reduce the Aliasing, pass through the Low pass Filter and travels it to Beamforming IC after converting it to A/D. Beamforming IC control the signals of 8 channel by Rx focusing, and forward them to Mid Processor IC MGA015A on DSC.

Its main components are ;

- MOSFET Driver EL7222 x 16 ea
- PMOS TP2520 x 16 ea
- NMOS TN2524 x 16 ea
- Dual TGC Amp AD604 x 8 ea
- Cross Point Switch (16 x 8) MT8816 x 1 ea
- OP Amp AD812 x 8 ea
- Beamforming IC MCB014A x 2 ea
- XC95144 for Control x 1 ea

2.2 Block Diagram



2.3 Signal Definition

2.3.1 CPLD Signal Definition

Name	I/O	Description
ADDR[0-5]	Input	HOST Address
/RPT	Input	Rate Pulse Train
/P_O_RESET	Input	Power On Reset by RC Time Constant
DATA[0-7]	Input/Output	HOST Data DATA[0-15] for MCB014A(BFIC)
/PRB_INS	Input	Low : Probe Inserted High : Probe Not Inserted If Probe is inserted, then /PRB_INS=Low
FREEZE	Input	Freeze If scanning is stopped, then FREEZE=high
/CPU_RD	Input	HOST I/O Read
MASTER_CK	Input	25.2 MHz Clock (50.4MHz/2)
/CPU_WR	Input	HOST I/O Write
/ETRG	Input	Exciting Trigger
PRB_ID[0-4]	Input	Probe Identity Number PROBE_ID[3] : default Low PRB_ID[3] is not used.
TDI	Input	CPLD download TDI
TMS	Input	CPLD download TMS
TCK	Input	CPLD download TCK
TDO	Output	CPLD download TDO
HV_ON	Output	High : High Voltage On Low : High Voltage Off High Voltage On when probe connect to the system
/AD_EN	Output	A/D Converter Enable Default Low
INIT_MODE[2]	Output	BFIC Initial Mode Real Mode : High Download Mode : Low
/TX_MASK	Output	Tx Fire Disable Display Low under Probe Disconnection or Freeze mode

/P_WR	Output	BFIC P Register Write Strobe Use it when latch the Scanline on BFIC
/BFIC_CS[0-1]	Output	BFIC Chip Select /BFIC_CS[0] : A/D Channel 0-3 /BFIC_CS[1] : A/D Channel 4-7
/BFIC_RST	Output	BFIC Reset
/DATA_RD	Output	Host Data Read
/DATA_WR	Output	Host Data Write
/DATA_EN	Output	Host Data Enable
BFIC_ADDR[0-2]	Output	BFIC Address

2.3.2 Connector signals between DSC and FE

Name	I/O	Description
ADDR[0-5]	Input	HOST Address
FE_CTRL_CLK	Input	Front End Control Clock MT8816 Control Clock 16 ea HVSW Clock 24 ea
/FE_CTRL_LE	Input	HVSW Latch Enable
FE_CTRL_RST	Input	MT8816 Reset
FE_CTRL_ADDR[0-5]	Input	MT8816 Address 0-15
FE_CTRL_DATA[0-7]	Input	MT8816 Control AY[0-2]=DATA[0-2] CPSW_DATA,CS = DATA[3] HVSW Control /HVSW_DATA[0-3]=DATA[4-7]
SCANLINE[0-7]	Input	Scanline 0-255
SYNTHETIC	Input	Low : Normal Tx High : Synthetic Tx
CTRL_RESERVED	Input	Reserved / Default Low
FREEZE	Input	High : Freeze Low : Real
25.2MHZ	Input	Master Clock 25.2MHZ
/EX_TRG	Input	Exciting Trigger
/B_EOF	Output	Beamforming Data Enable Use it on MPIC MGA015 of DSC
/OF	Input	One Frame
/RP	Input	Rate Pulse
/RPT	Input	Rate Pulse Train
TGC_D[0-7]	Input	TGC Data
T_SBCLK	Output	Battery Clock
T_SBDATA	Output	Battery Data
PRINT_REMOTE	Input	Echo Printer Remote
B_FREEZE_REMOTE	Output	Freeze/Remote The switch on the VET probe is using for toggle. Using for Freeze, press it short. Using for Store, press it long (over 3secs.)
FP[0-2]	Input	Focal Point / FP[2] = Default Low
CLK_120KHZ	Input	Power Clock 120KHZ

CLK_240KHZ	Input	Power Clock 240KHZ
VP5D	Output	+5V
VP3.3D	Output	+3.3V
VP12A	Output	+12V
VP5A	Output	+5V
VN5A	Output	-5V
/CPU_WR	Input	Host Write
/CPU_RD	Input	Host Read
EXT_B[0-16]	Output	Beamforming Data
LCDVR_A	Output	LCD Brightness Knob
LCDVR_B	Output	LCD Brightness Knob
GAIN_A	Output	GAIN Knob
GAIN_B	Output	GAIN Knob
NEAR_A	Output	NEAR Knob
NEAR_B	Output	NEAR Knob
FAR_A	Output	FAR Knob
FAR_B	Output	FAR Knob

2.3.3 Connector signals between Power and FE

Name	I/O	Description
PRINT_REMOTE	Output	Echo Printer Remote
CLK_120KHZ	Output	Power Clock 120KHZ
CLK_240KHZ	Output	Power Clock 240KHZ
HV_ON	Output	High : High Voltage On Low : High Voltage Off
T_SBCLK	Input	Battery Clock
T_SBDATA	Input/Output	Battery Data
VP5D	Input	+5V
VP3.3D	Input	+3.3V
VP12A	Input	+12V
VP5A	Input	+5V
VN5A	Input	-5V
HVP	Input	+80V
HVN	Input	-80V

2.3.4 Connector signals between FE Adapter and FE

Name	I/O	Description
PLS_OUT[0-15]	Input/Output	Ultrasound Echo
+80VA	Output	+80V
-80VA	Output	-80V
+5VA	Output	+5V
/HVSW_DATA[0-3]	Output	High Voltage Control Data
HVSW_CLK	Output	High Voltage Control Clock 3.15MHz Clock 24 ea
/HVSW_LE	Output	High Voltage Control Latch Enable
PRB_ID[0-4]	Input	Probe ID
/PRB_INS	Input	Low : Probe Inserted High : Probe Not Inserted
FREEZE_REMOTE	Input	Freeze Remote Short Click : Freeze Long Click : Store

2.3.5 Connector signals between FE Adapter and SPC(System Probe Connector)

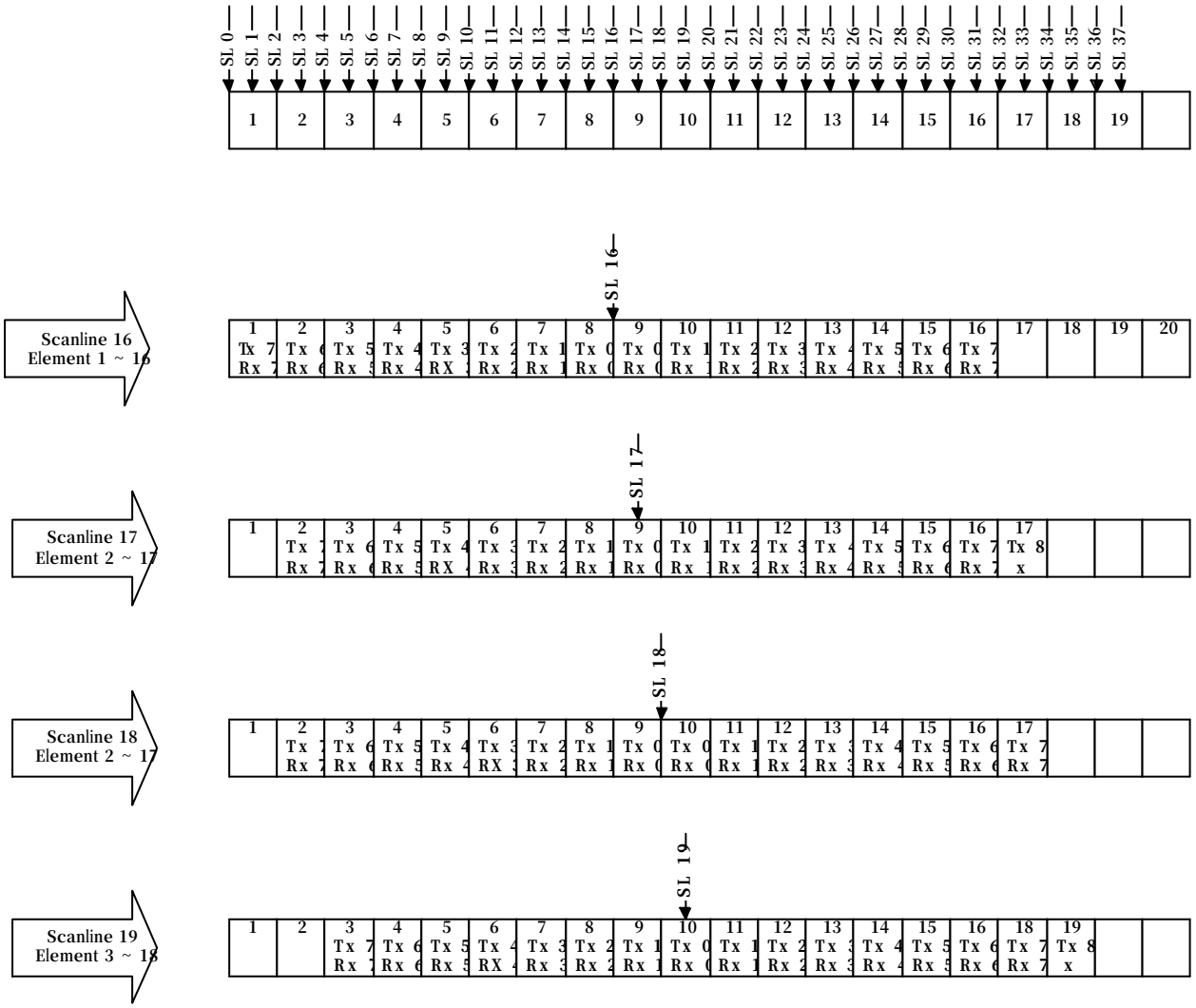
Name	I/O	Description
PLS_OUT[0-15]	Input/Output	Ultrasound Echo
+80VA	Output	+80V
-80VA	Output	-80V
+5VA	Output	+5V
/HVSW_DATA[0-3]	Output	High Voltage Control Data
HVSW_CLK	Output	High Voltage Control Clock 3.15MHz Clock 24 ea
/HVSW_LE	Output	High Voltage Control Latch Enable
PRB_ID[0-4]	Input	Probe ID
/PRB_INS	Input	Low : Probe Inserted High : Probe Not Inserted
FREEZE_REMOTE	Input	Freeze Remote Short Click : Freeze Long Click : Store

2.3.6 Connector signals between SPC(System Probe Connector) and Probe

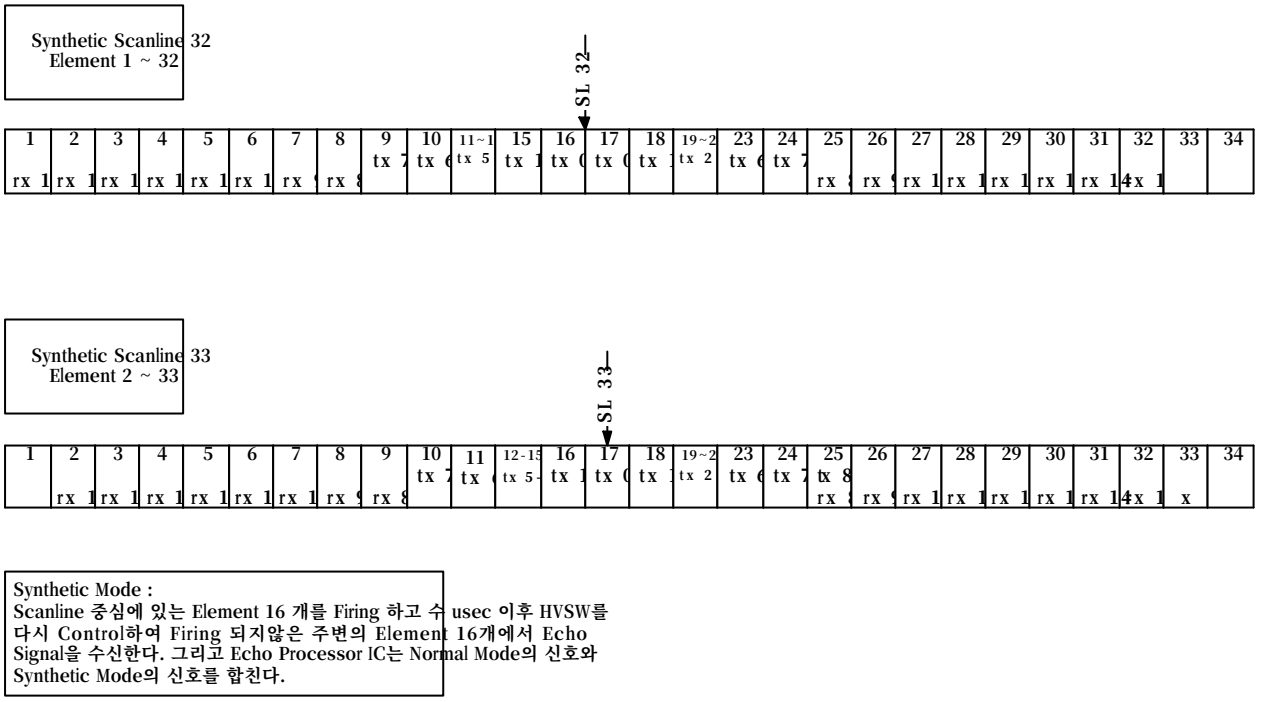
	1	2	3	4	5	6
A	ECHO 0	GND	ECHO 1	GND	ECHO 2	GND
B	GND	ECHO 3	GND	ECHO 4	GND	ECHO 5
C	ECHO 6	GND	ECHO 7	GND	ECHO 8	GND
D	GND	ECHO 9	GND	ECHO 10	GND	ECHO 11
E	ECHO 12	GND	ECHO 13	GND	ECHO 14	ECHO 15
F	N.C.	N.C.	GND	+ 80 V	+ 80 V	GND
G	GND	- 80 V	- 80 V	GND	+ 5 V	GND
H	/DAT0 0	/DATA 1	GND	/DATA 2	/DATA 3	GND
J	Remote	HVSW_CLK	/HVSW_LE	N.C.	N.C.	PRB_ID 0
K	PRB_ID 1	PRB_ID 2	GND	PRB_ID 3	PRB_ID 4	/PRB_INS

2.4 Scanline Definition

2.4.1 Normal Mode

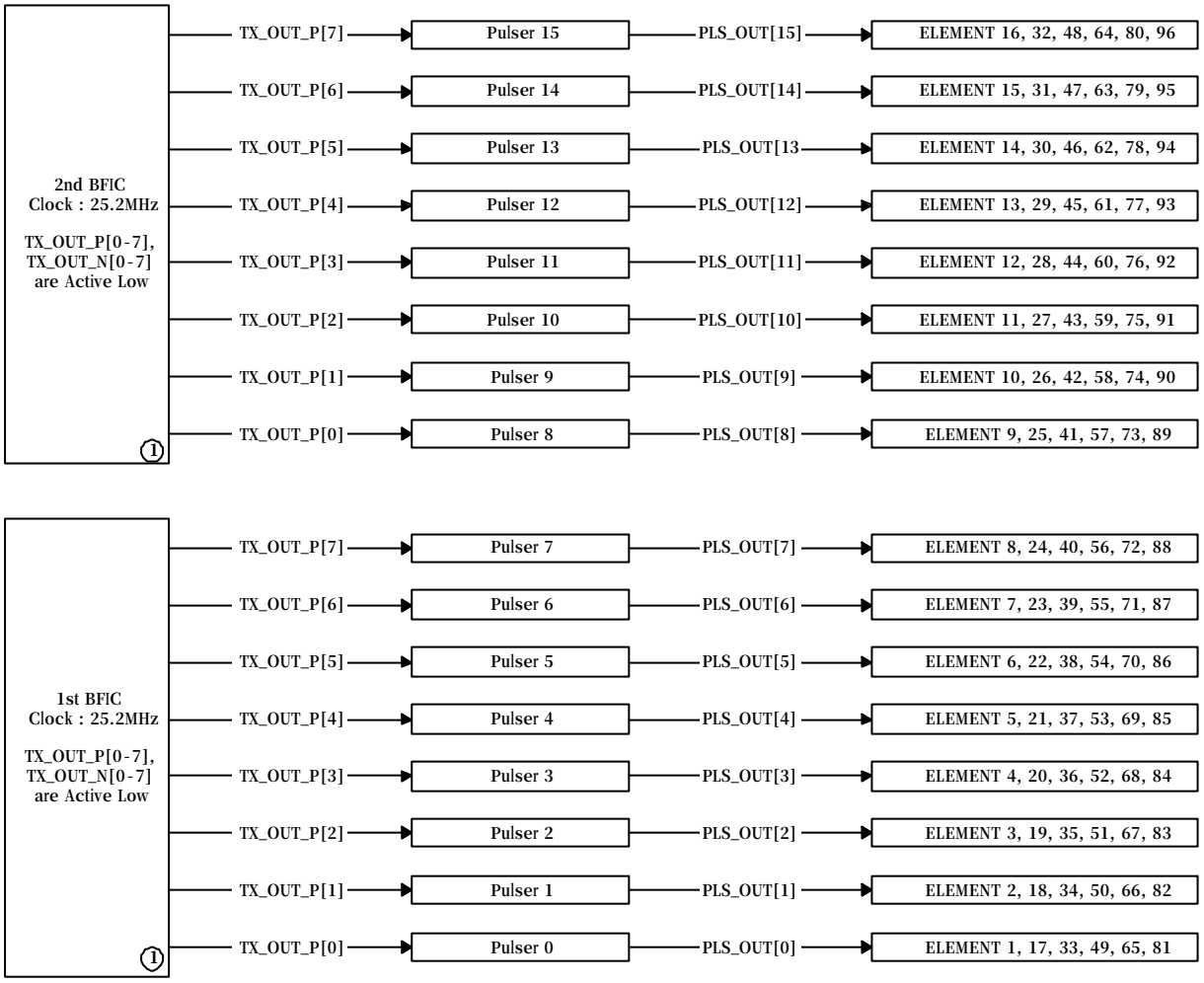


2.4.2 Synthetic Mode



Synthetic Mode :
Scanline 중심에 있는 Element 16 개를 Firing 하고 수 usec 이후 HVSW를 다시 Control하여 Firing 되지않은 주변의 Element 16개에서 Echo Signal을 수신한다. 그리고 Echo Processor IC는 Normal Mode의 신호와 Synthetic Mode의 신호를 합친다.

2.5 Pulser vs Elements



2.6 Detail Description

2.6.1 TGC Amp

The main chip of TGC Amp is AD604. Two Variable Gain Amp is located inside of the chip and they are composed of 2 channels TGC Amp. The ultrasound signal that was reflected or propagated from a medium can compensate by Variable Gain as time, that is to say it is a proceeded distance, at this stage.

Gain Range	: 0 ~ 48 dB (Preamp Gain = + 14 dB)
Input resistance	: 300 kohm
Variable Gain Scaling	: 20 dB/V
Gain [dB]	= 20[dB/V] * TGC_Curve[v] - 5 [dB]
Output Impedance	: 2 ohm
Load resistance	> 500 ohm
Reference Voltage	: 2.5V (Gain Scaling 20 dB/V)

2.6.2 Reordering

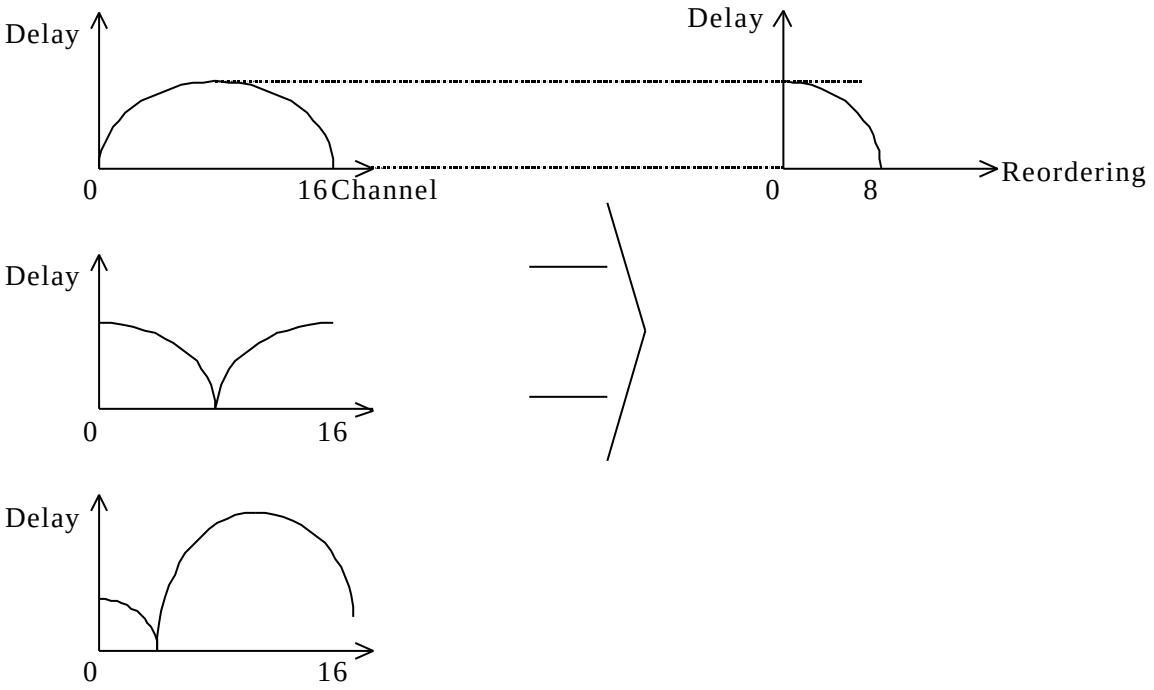
One MT8816 generate 16 ×8 MUX.

It is controlled by Scan Lind regardless TX Focal Point or Probe type.

[Normal Tx Mode]

The ultrasound signal symmetrically controls the reordering around Center Element. But at the point of BFIC Channel, the Center of signal could be moved as Scanline because it has sixteen MUX (6x1) as High Voltage Switching IC in the Probe Box.

Thus it is possible to control BFIC RX Control date size by reordering this signal.



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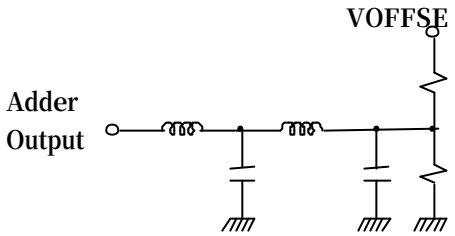
[Synthetic Tx mode]

To achieve 1 scanline image, the element that used Tx or Rx is the same in Normal Tx mode. Under Synthetic Tx mode, it is the same as Tx element but RX receive the first signal from the center 16 elements and receive again the second signal from the near side 16 elements. As the result, RX generate 32 channel image in MGA015A Mid Processor ASIC by adding two scanline Beamforming data in RF domain

2.6.3 LPF

Low-Pass Filter located the edge of the Analog Receiver Channel is worked both noise suppression as stop band and Anti-aliasing Filter as reduce aliasing caused by high frequency probe such as 7.5MHz Probe



[Figure 5. Low-Pass Filter]

A/D clock is 25.2 MHz and maximum center frequency of probe is 7.5MHz.
And 3dB cut off frequency for Trade-off is 10MHz.
LPF works as Bessel filter and constructs the circuit by 4^{th} step for reducing a ringing.

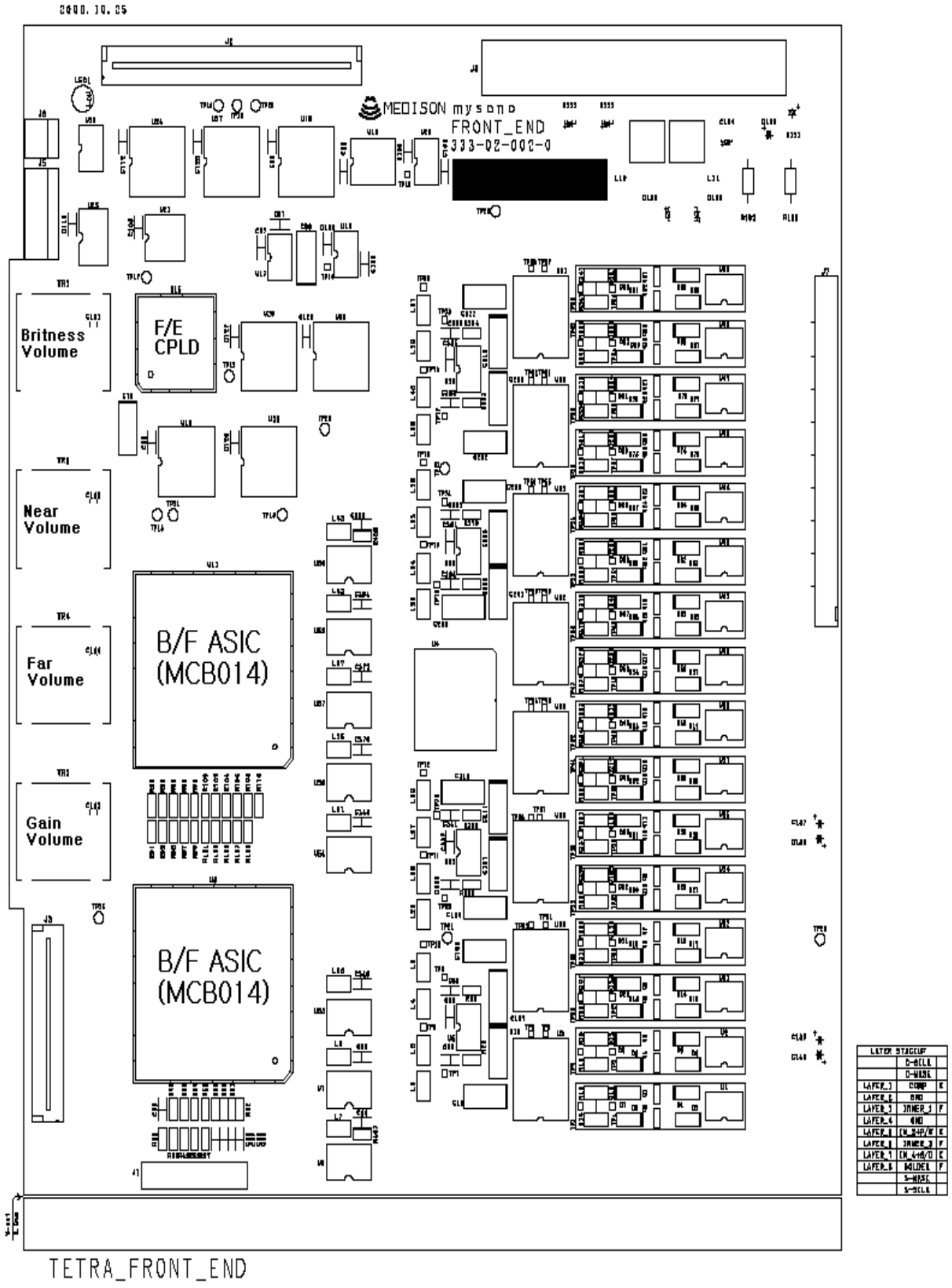
2.6.4 Beamforming IC MCB014A

For Reordering, it is necessary 8 Channel A/D Converters. BFIC has 4 Channels. To make a Beamforming, two BFICs are required.
Tow's Compliment is output and Bit 1 to 16 is used at the last output.

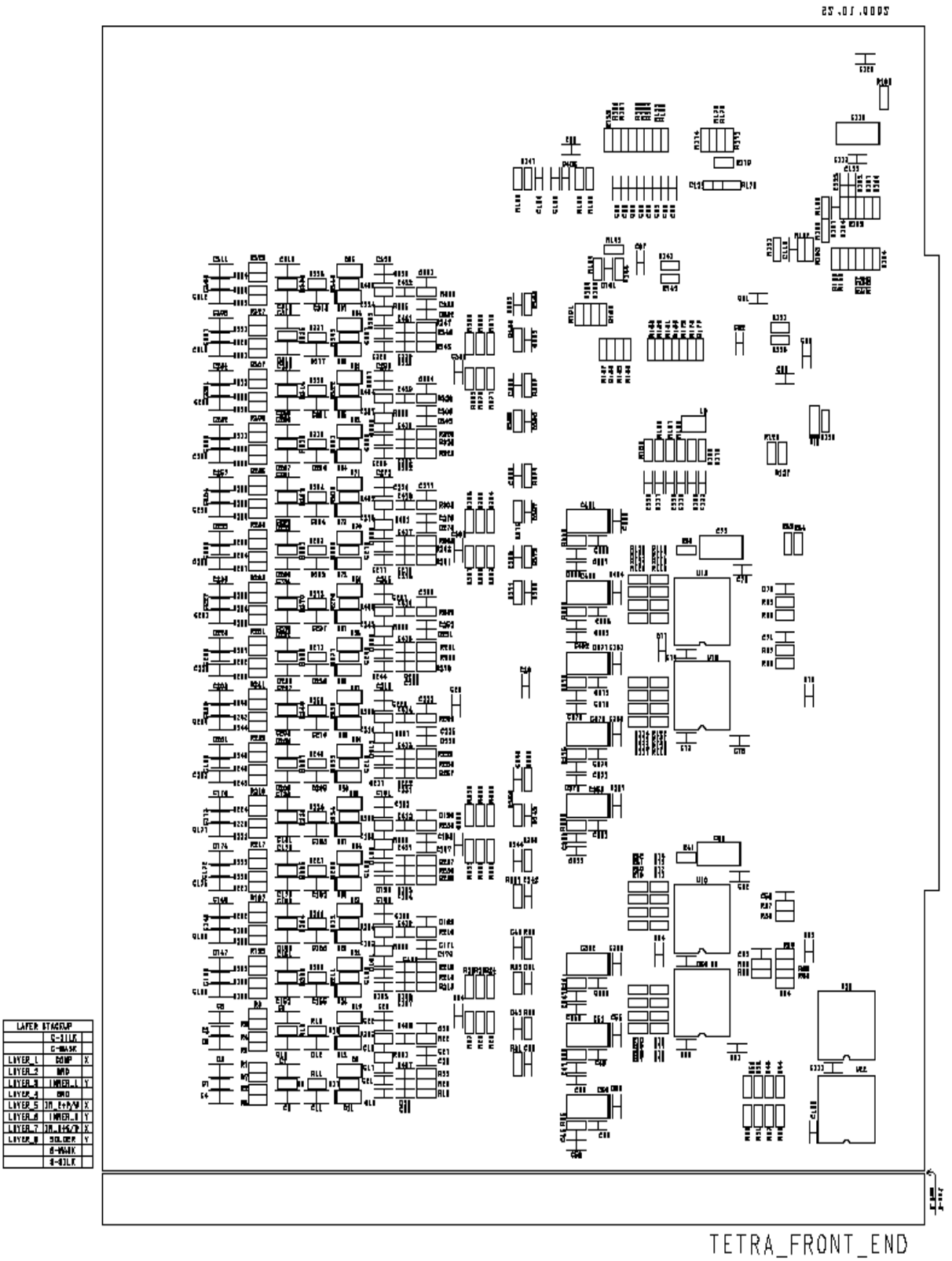
Both of main clock and the last output data rate are 25.2Mhz. It is possible to control Tx Delay by twice frequency and to control Tx Period under 25.2MHz, 40nsec.
To prepare the next calculation of scanline during Beamforming, have to provide the next scanline between /RPT rising point and /ETRG rising point.

2.7 PCB BOARD LAY OUT

2.7.1 F/E TOP SIDE

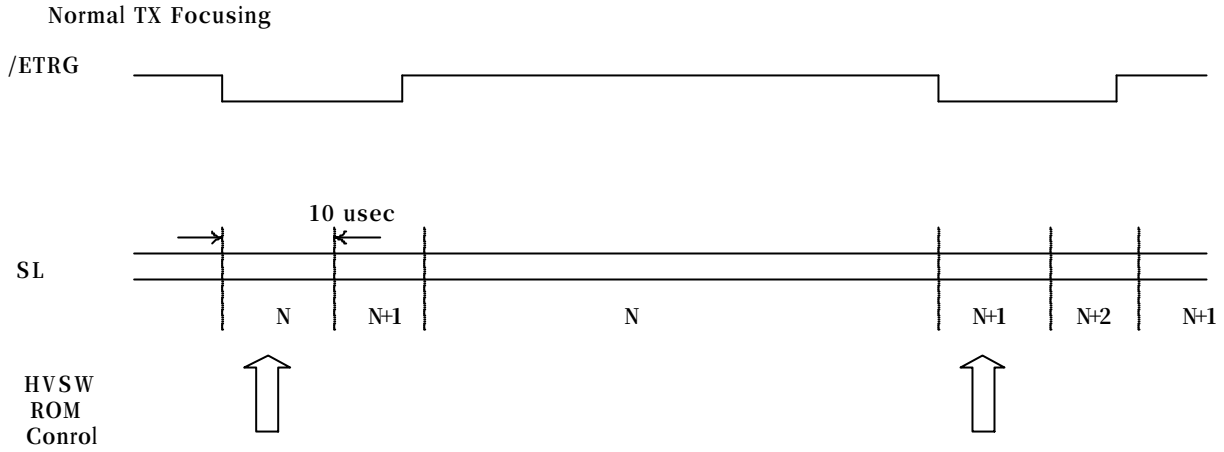


2.7.2 F/E BOTTOM SIDE



2.8 Timing Chart

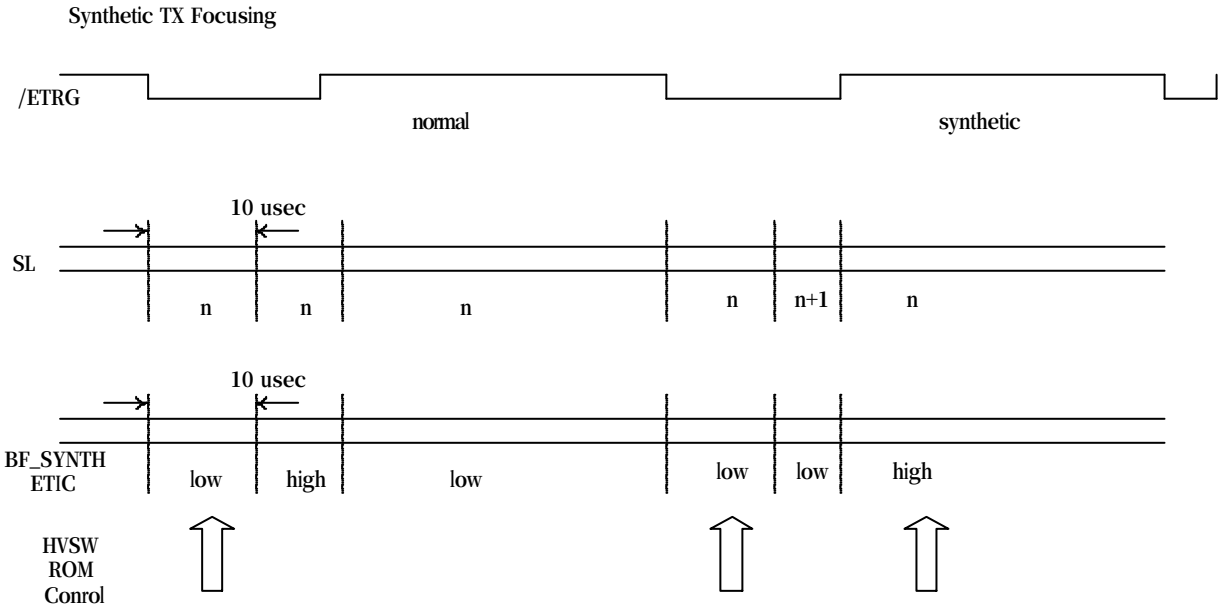
2.8.1 Normal TX Focusing



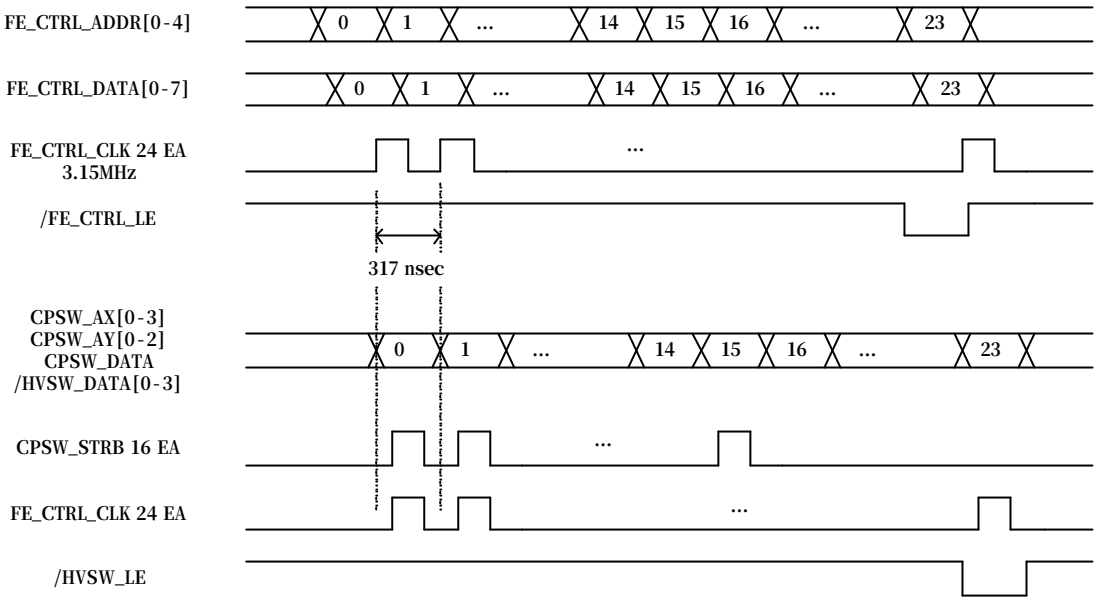
N= Current scanline
N+1 = Next Scanline

If Next scanline is M Mode Line,
then N+1 means M mode scanline.

2.8.2 Synthetic Tx Focusing

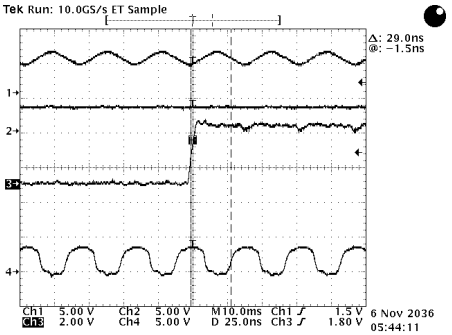


2.8.3 Control Timing

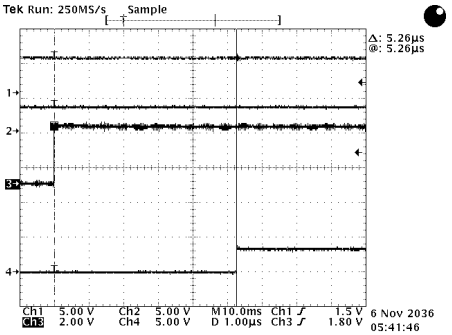


2.9 Wave Form

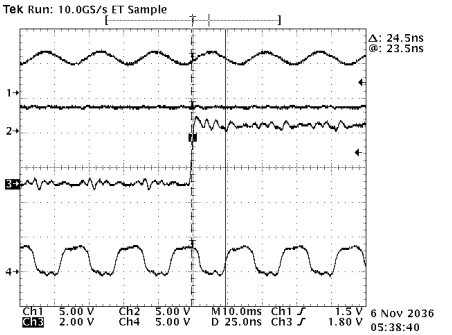
/EOF Master_ck (U8,182) = 29ns



/ETRG /EOF (U8,182) = 5.26us

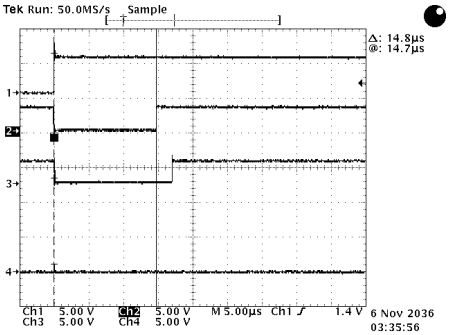


/ETRG (U25,2) , Master_ck (U25,19) = 24.5ns



/OF(TP10) => CH1,/RPT(TP16) => CH2

/ETRG(TP17) => CH3(C2-5/60BD)

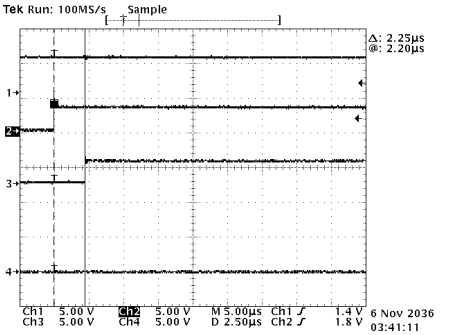


/OF(TP10) => CH1,/RPT(TP16) => CH2

/ETRG(TP17) => CH3

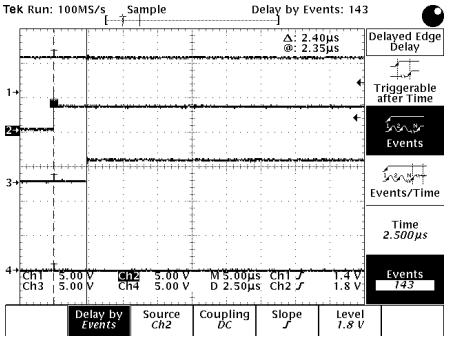
/RPT Event 1 /RPT Blank = 14.8us

/RPT /ETRG rising gap = 225us



/OF(TP10) => CH1,/RPT(TP16) => CH2

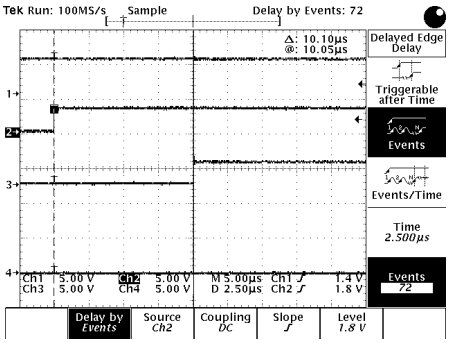
/ETRG(TP17) => CH3,/RPT Event 143 = 2.4us



/OF(TP10) => CH1,/RPT(TP16) => CH2

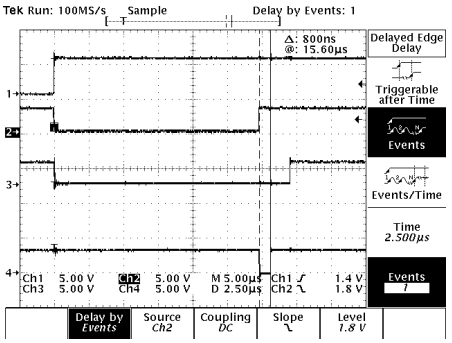
/ETRG(TP17) => CH3

/RPT Event72 /RPT /ETRG rising gap = 10.1us

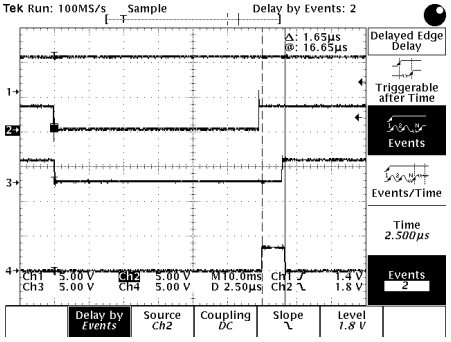


/RPT(TP16)=>TP1,/P_WR(U8(MCB014)PIN 138)

/P_WR Blank = 800ns

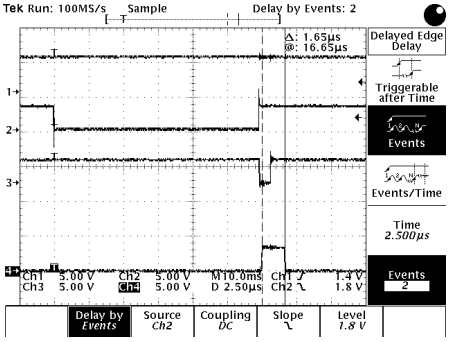


/RPT Scan line(MCB014 = PIN 137) Event2



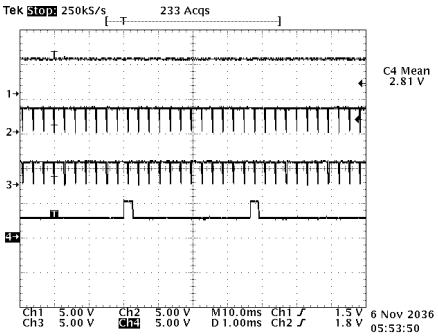
/RPT Scanline(MCB014 = PIN 137) / P_WR

when /P_WR rising, MCBO14 latch it as next scanline hold



/RPT B_FREEZE_REMOTE

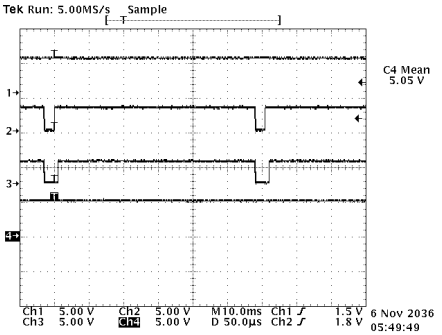
In VET probe, it turns Low when press the switch.



/RPT B_HV_ON (R171)

Connecting with Probe, High = 5.05V

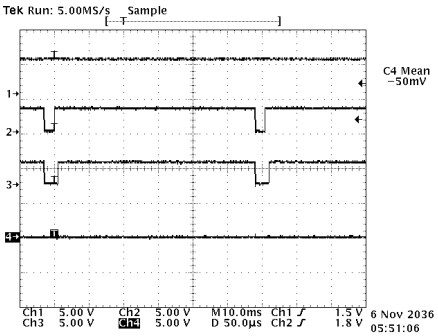
Connecting without Probe, Low = 360mV



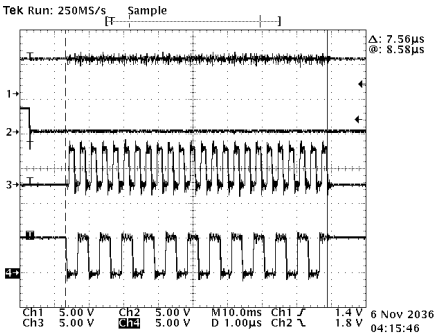
/RPT B_PRBINS (U28,18)

Connecting with Probe, Low = 0V

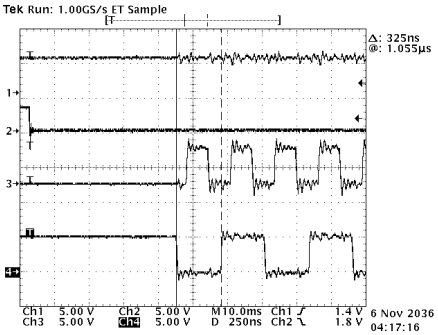
Connecting without Probe, Low = 3.3V



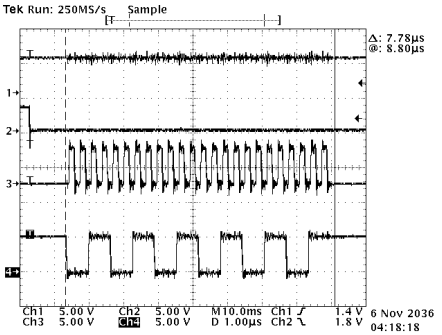
/RPT CPSW_STRB,CPSW_AX0 (U4,5)



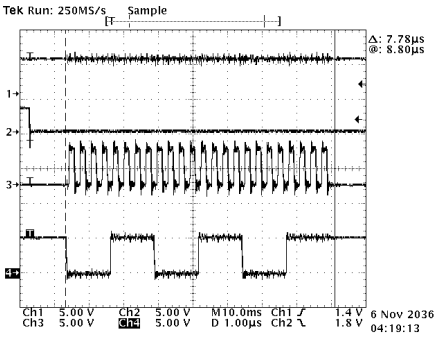
/RPT CPSW_STRB,CPSW_AX0 = 325ns



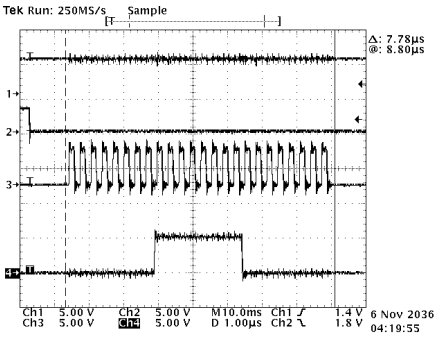
/RPT CPSW_STRB,CPSW_AX1 (U4,24)



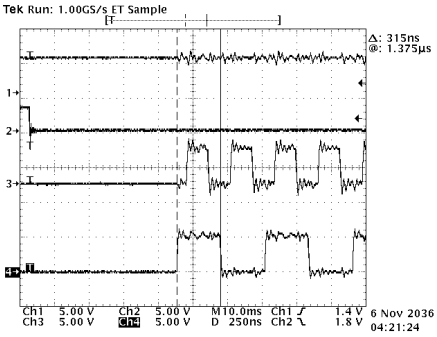
/RPT CPSW_STRB,CPSW_AX2 (U4,25)



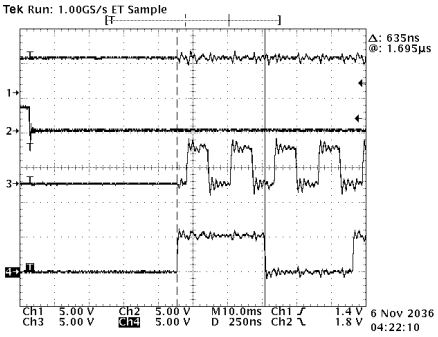
/RPT CPSW_STRB,CPSW_AX3 (U4,4)



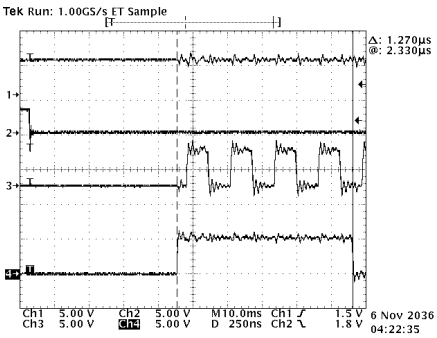
/RPT CPSW_STRB,CPSW_AY0 (U4,26)



/RPT CPSW_STRB,CPSW_AY1 (U4,27)

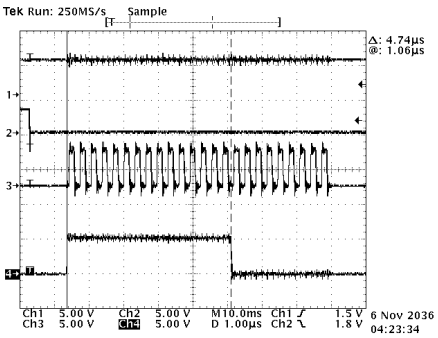


/RPT CPSW_STRB,CPSW_AY2 (U4,2)

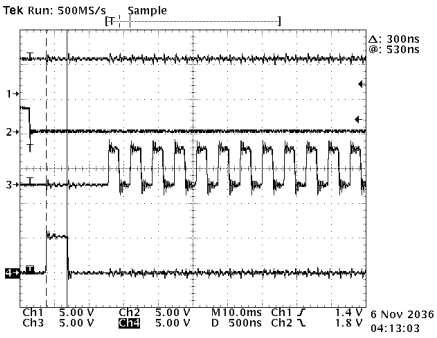


/RPT CPSW_STRB,CPSW_DATA (U4,42)

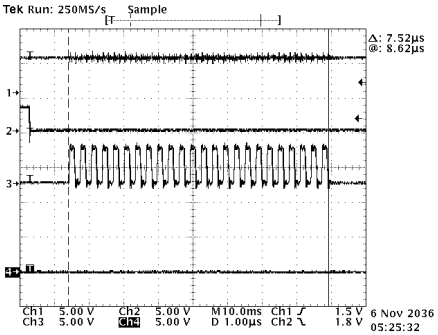
= 4.74us



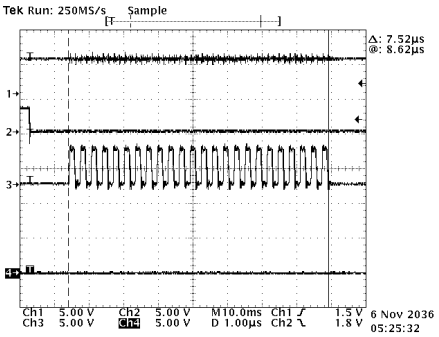
/RPT CPSW_STRB,CPSW_RST(U4,3) = 300ns



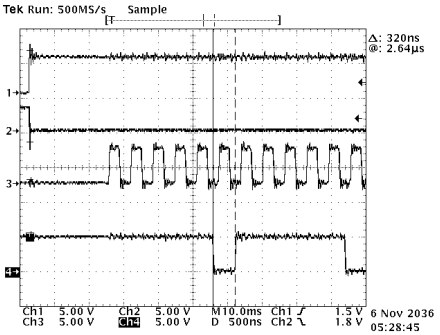
/RPT HVSW_CLK(R170) = 7.52us



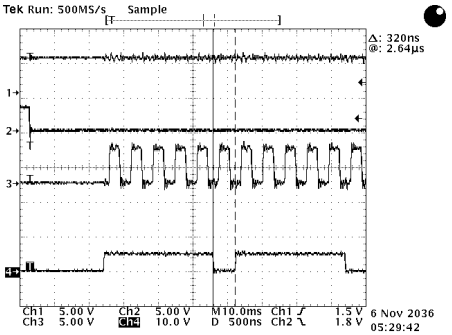
/RPT HVSW_CLK(R170) = 7.52us



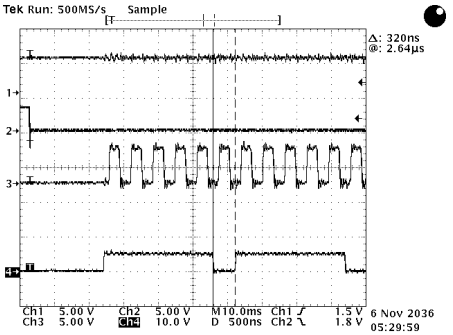
/RPT HVSW_CLK /HVSW_DATA0 (R188) = 320ns



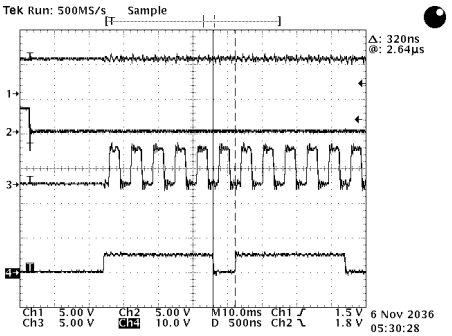
/RPT HVSW_CLK /HVSW_DATA1 (R189



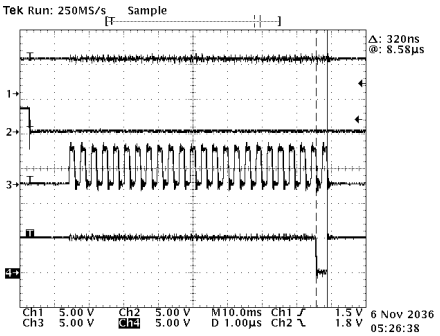
/RPT HVSW_CLK /HVSW_DATA2(R190)



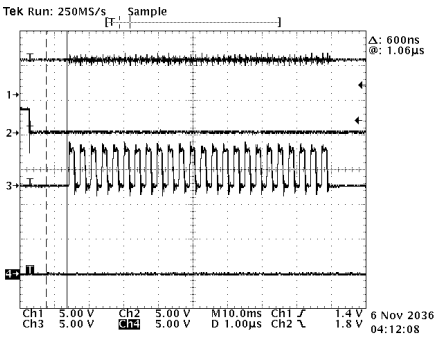
/RPT HVSW_CLK /HVSW_DATA3(R191)



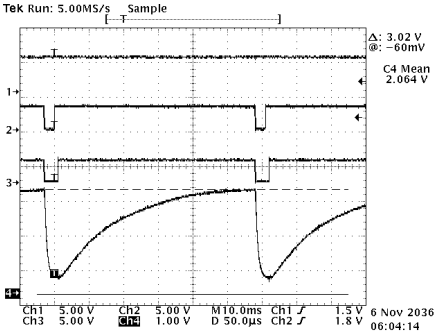
/RPT HVSW_CLK /HVSW_LE(R178)



/RPT SPSW_STRB(U4 PIN20) = 7.5us, 24ea clock

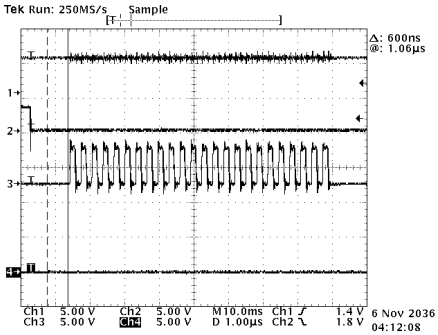


/RPT TGC_CURVE(R147) = 3.02V



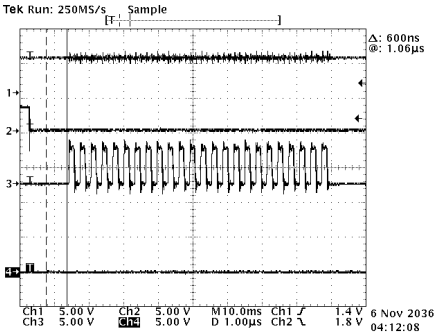
/RPT SPSW_STRB(U4 PIN20) = 7.5us,

24 ea clock

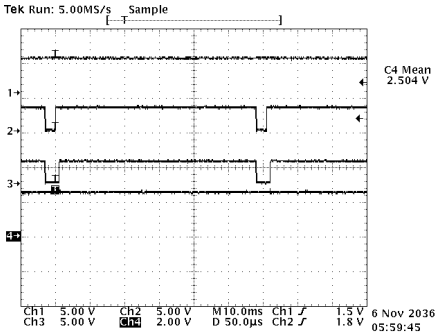


/RPT SPSW_STRB(U4 PIN20) = 7.5us,

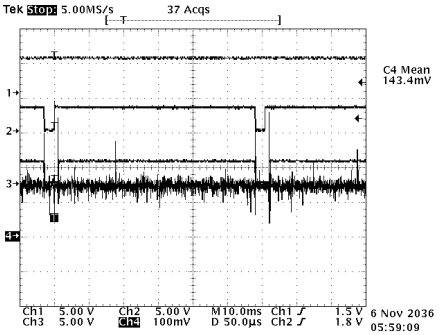
24ea clock



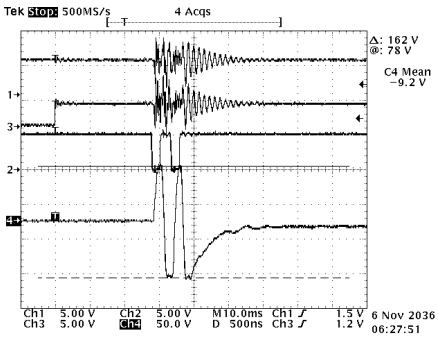
/RPT TGC_REF (TP14) = 2.504V



/RPT VREF_0.1 (R141) = 143Mv

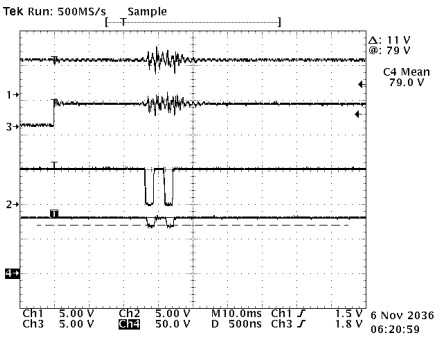


/ETRG /TX_OUT_P [0], C11 = ±80V (Δ = 162V)



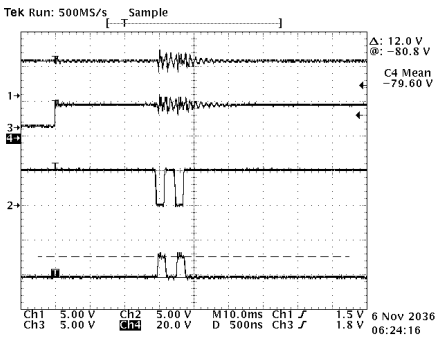
/ETRG /TX_OUT_P [0]

C3 = 5V -> 12V -> 80V (Δ = 11V)



/ETRG /TX_OUT_N [0]

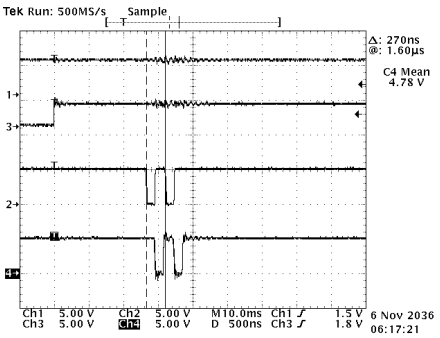
C4 = 5V -> 12 -> -80V (Δ = 12V)



/E/TRG = CH3

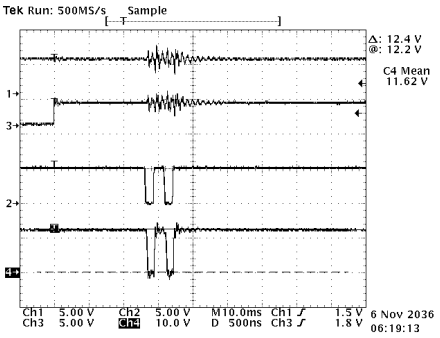
/TX_OUT_P [0] (U1, 4) = CH2

/TX_OUT_N [0] (U1, 2) = CH1

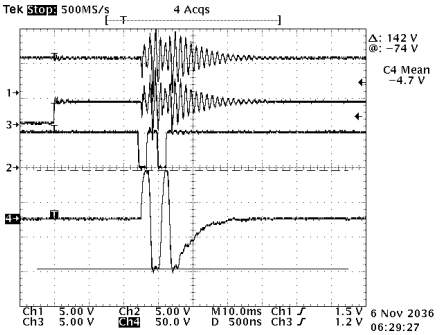


/ETRG /TX_OUT_P [0], EL7222, pin_5 = 5V

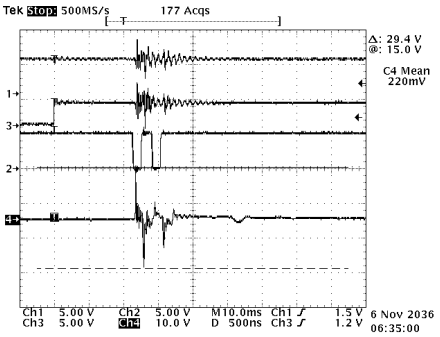
-> 12V



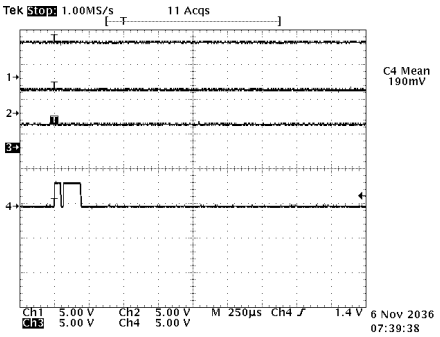
/ETRG /TX_OUT_P [0], TP1 = (Δ = 142V)



/ETRG /TX_OUT_N [0], TP3(±9)



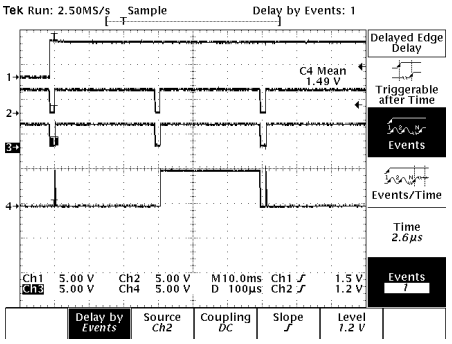
/RPT /INIT_MODE [2] = High



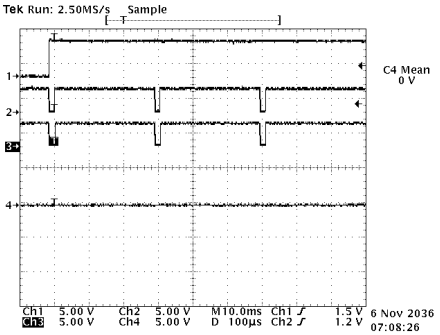
/OF /RPT, SYATHETIC (U8, PIN129)

Normal = low

Synthetic = high

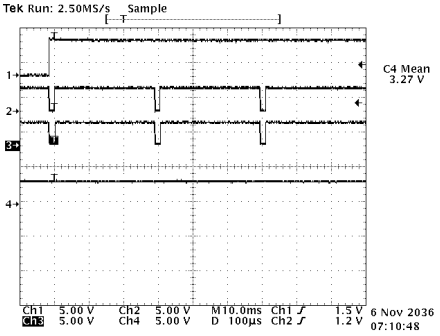


/RPT, BFIC_ADDR [0,1,2] = Low

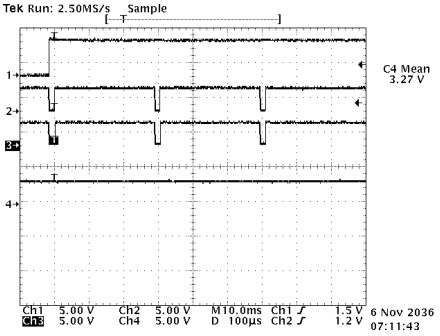


/RPT /BFIC_CS [0] = High 3.27V

/RPT /BFIC_CS [1] = High 3.27V

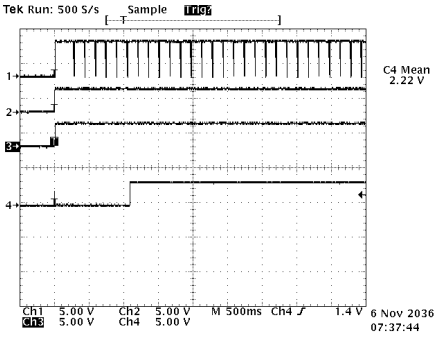


/RPT /BFIC_RST = High 3.27V



/RPT /BFIC_RST, INIT_MODE [2]

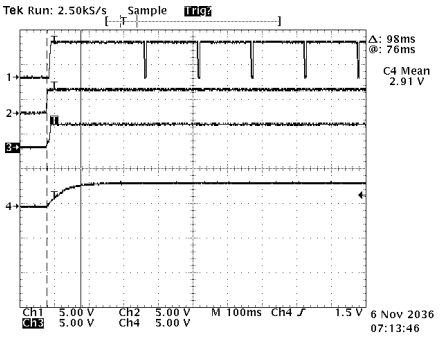
Booting, Low -> High -> Low



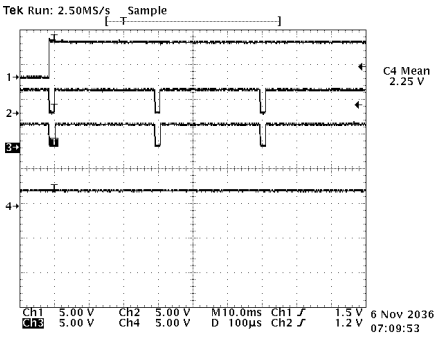
/RPT /FP [0-2] =

Power ON, High = 3.27V

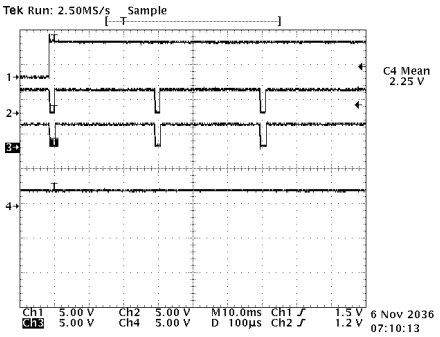
Low = 30mV



/RPT /DATA_RD = High 2.25V

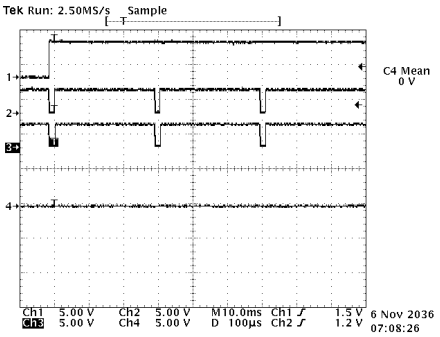


/RPT /DATA_WR = High 2.25V



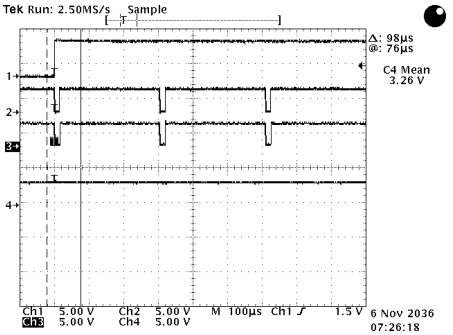
/RPT /FP [0-2] =

Change from 0 to 3 under Focal point moving

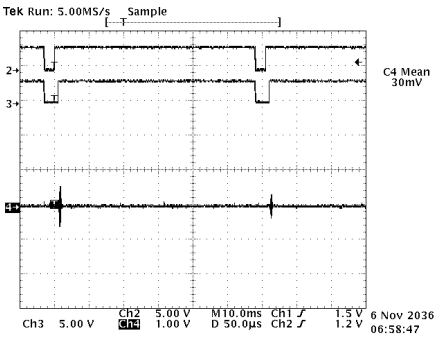


/RPT /INIT_MODE [2] =

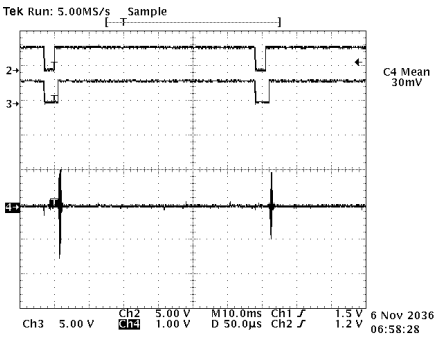
Booting 시 Low -> High -> Low



/RPT, TP9 = LPF output 30Mv

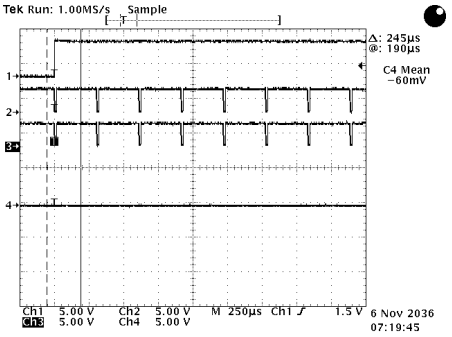


/RPT, TP7 = Adder output 30mV

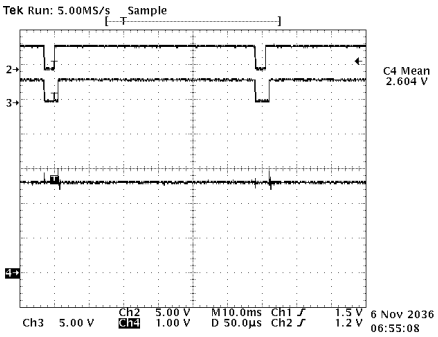


/RPT /TX_MASK = Real = High

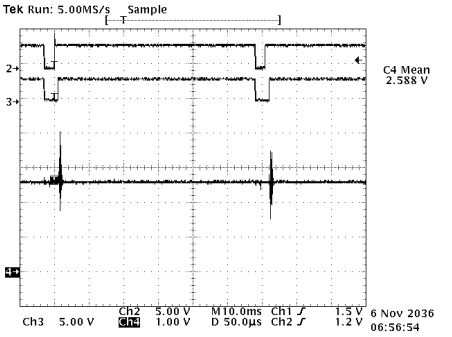
Freeze = Low



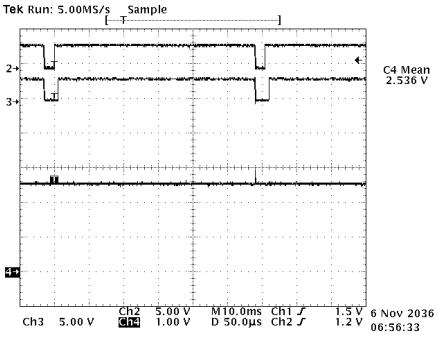
/RPT (U3, PIN1), C19 = 2.61V



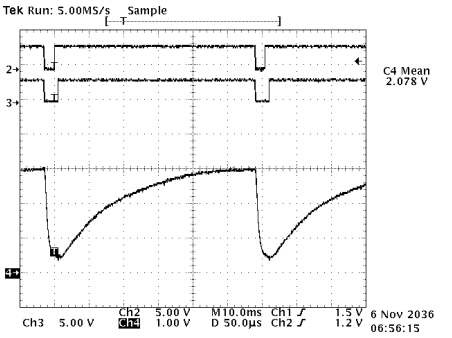
/RPT (U3, PIN22), TP5 = 2.59V



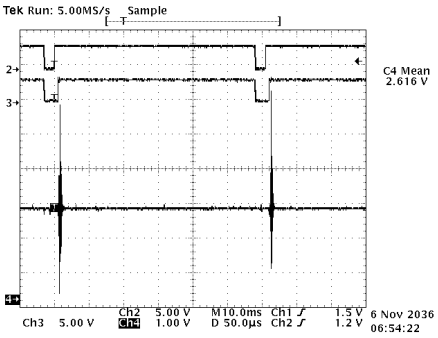
/RPT (U3, PIN23), R20 = 2.53V



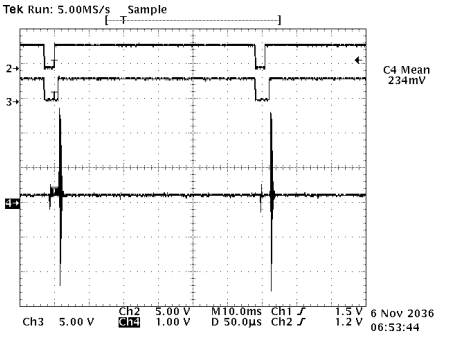
/RPT (U3, PIN24), R19 = TGC – CURVE



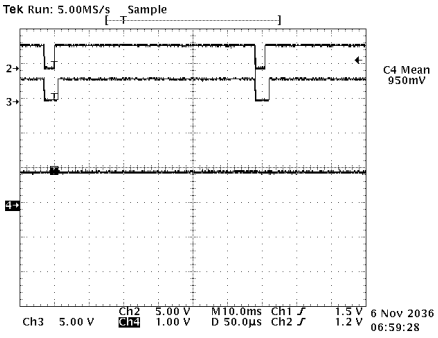
/RPT (U3, PIN3), C21 = 2.61V

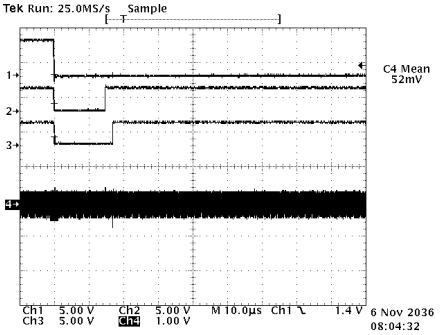
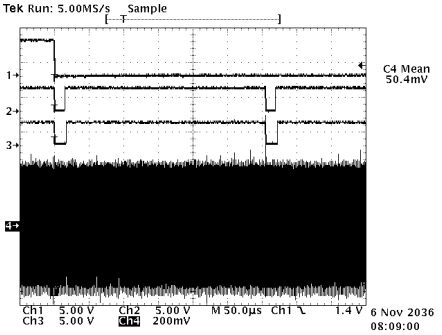
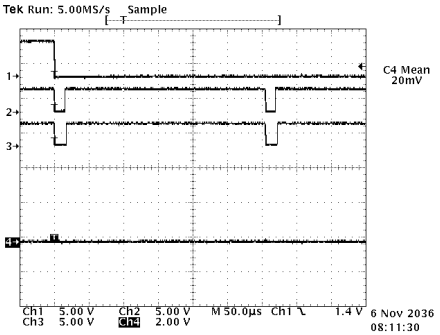
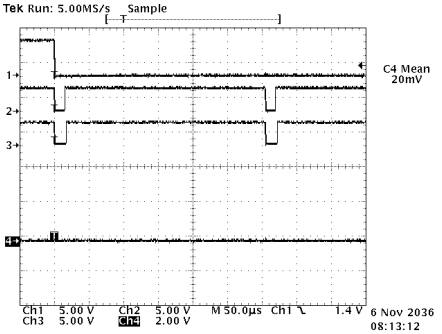
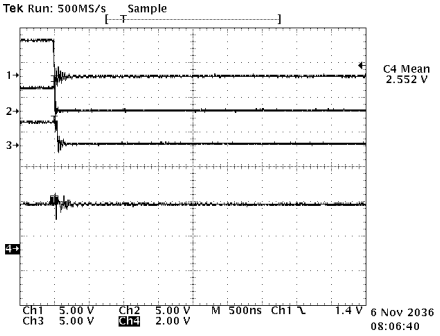
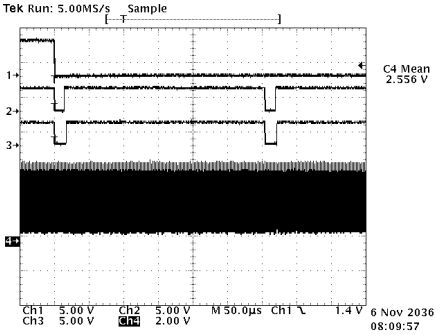


/RPT (U3, PIN4), C21 = 226mV



/RPT (U6, PIN6) AD9283 /A2N 950Mv

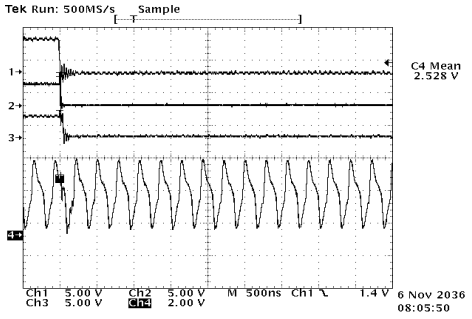


Function generator voltage = 1.17 V frequency = 3.5 M /ETRG /TX_OUT_N [0], TP3 	Function generator voltage = 1.17 V frequency = 3.5 M /ETRG /TX_OUT_N [0], TP3 
Function generator voltage = 1.17 V frequency = 3.5 M /RPT, TP7 	Function generator voltage = 1.17 V frequency = 3.5 M /RPT, TP9 
Function generator voltage = 1.17 V frequency = 3.5 M /RPT (U3, PIN1), C19 	Function generator voltage = 1.17 V frequency = 3.5 M /RPT (U3, PIN1), C19 

Function generator

voltage = 1.17 V frequency = 3.5 M

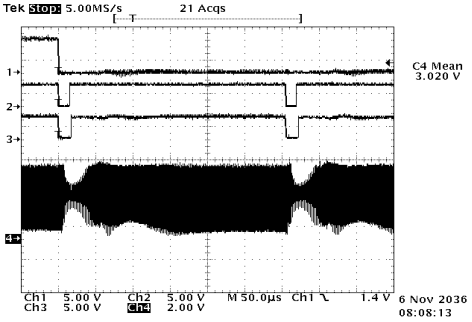
/RPT (U3, PIN2), C21



Function generator

voltage = 1.17 V frequency = 3.5 M

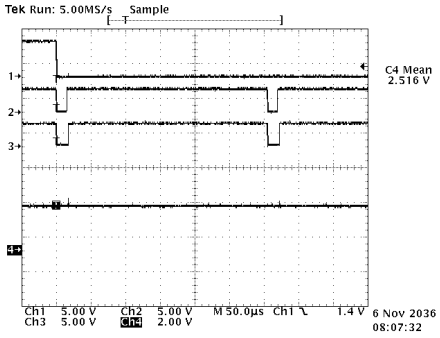
/RPT (U3, PIN22), TP5



Function generator

voltage = 1.17 V frequency = 3.5 M

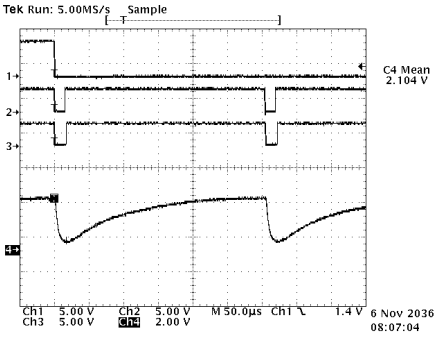
/RPT (U3, PIN23), R20



Function generator

voltage = 1.17 V frequency = 3.5 M

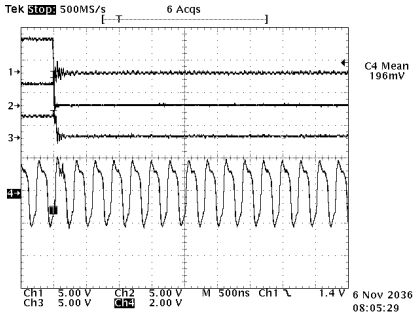
/RPT (U3, PIN24), R19 = TGC – CURVE



Function generator

Voltage = 1.17 V frequency = 3.5 M

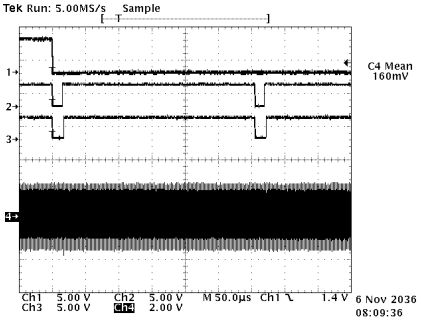
/RPT (U3, PIN4), C21



Function generator

voltage = 1.17 V frequency = 3.5 M

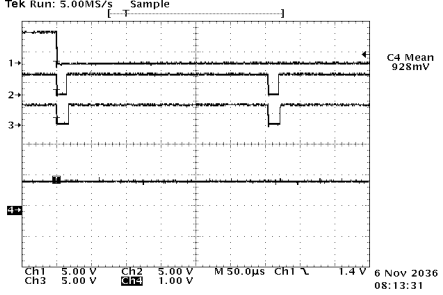
/RPT (U3, PIN4), C21



Function generator

voltage = 1.17 V frequency = 3.5 M

/RPT (U6, PIN6) AD9283 /A2N

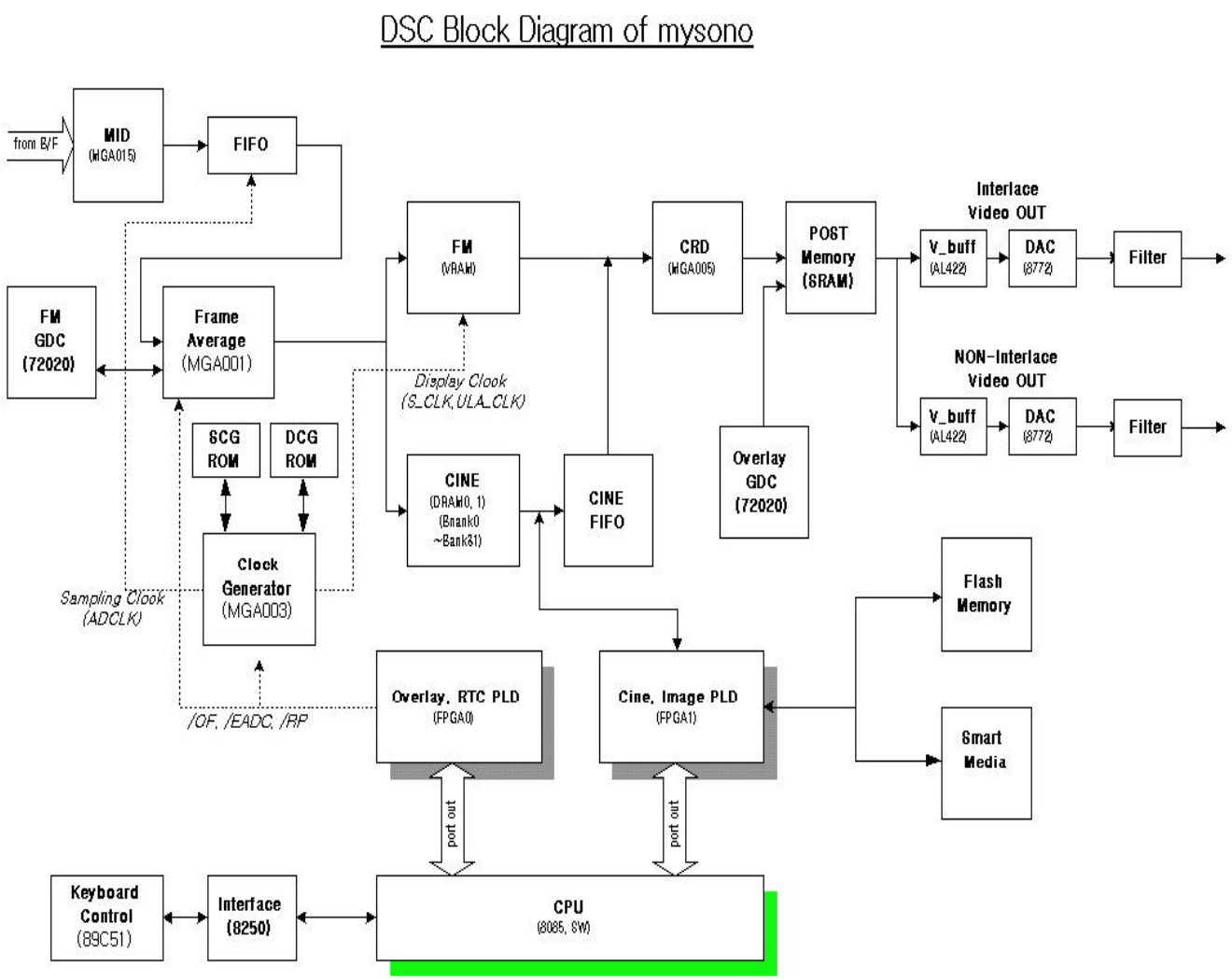


3.DSC Board

3.1. Description Overall

- B/F data pass to FIFO through MID Processor and the data is sampling by ADCLK on Clock Generator (MGA003) and then transfer to Frame Average (MGA001).
- MGA003 generates the Clock by integrating the standard signal (/OF, /RP, /EADC) come form RTC Controller (FPGA0), Sampling Clock information as Scan Line inside SCG•DCG ROM and Display Clock information.
- MGA001 works as Frame Average Function by using /OF, /RP, /EADC come from RTC Controller (FPGA0) under controlling Frame GDC, and then transfer the data to Frame Memory and Cine Memory.
- In Real mode, the data come from MGA001A is stored both Frame Memory and Cine Memory simultaneously. But the data come from Frame Memory transfer to CRD (MGA005).
- In Cine mode, the data come from MGA001A is not transfer either Frame Memory or Cine Memory and the data stored in Cine Memory pass to CRD (MGA005) and display on the screen.
- The Port out Command in CPU of Cine Controller (FPGA1) control the Cine Memory.
- The data come from Frame Memory (or Cine memory) is variable DCG rate each H-Sync. CRD (MGA005) interpolate it by 12.6MHz unit in 1D (Horizontal Interpolation) and make a data as equal then pass it to Post Memory for displaying.
- Port out command of CPU input into Overlay GDC. Overlay GDC generates Overlay data and then pass them to Post memory. And generate the general Control signals that are necessary in Overlay.
- Post Memory integrates the data come from CRD and Overlay GDC and makes the image adapted on 640x480. Then pass it to Video Buffer (AL422) and display it on the LCD (or Monitor).
- Video Buffer (AL422) receive the control signals come from Video Output Controller to adjust Refresh Rate of LCD (or Monitor) and output the Image data as 25.2MHz and then transfer them to DAC (TDA8775).

3.2. Block Diagram



3.3 Signal Definition

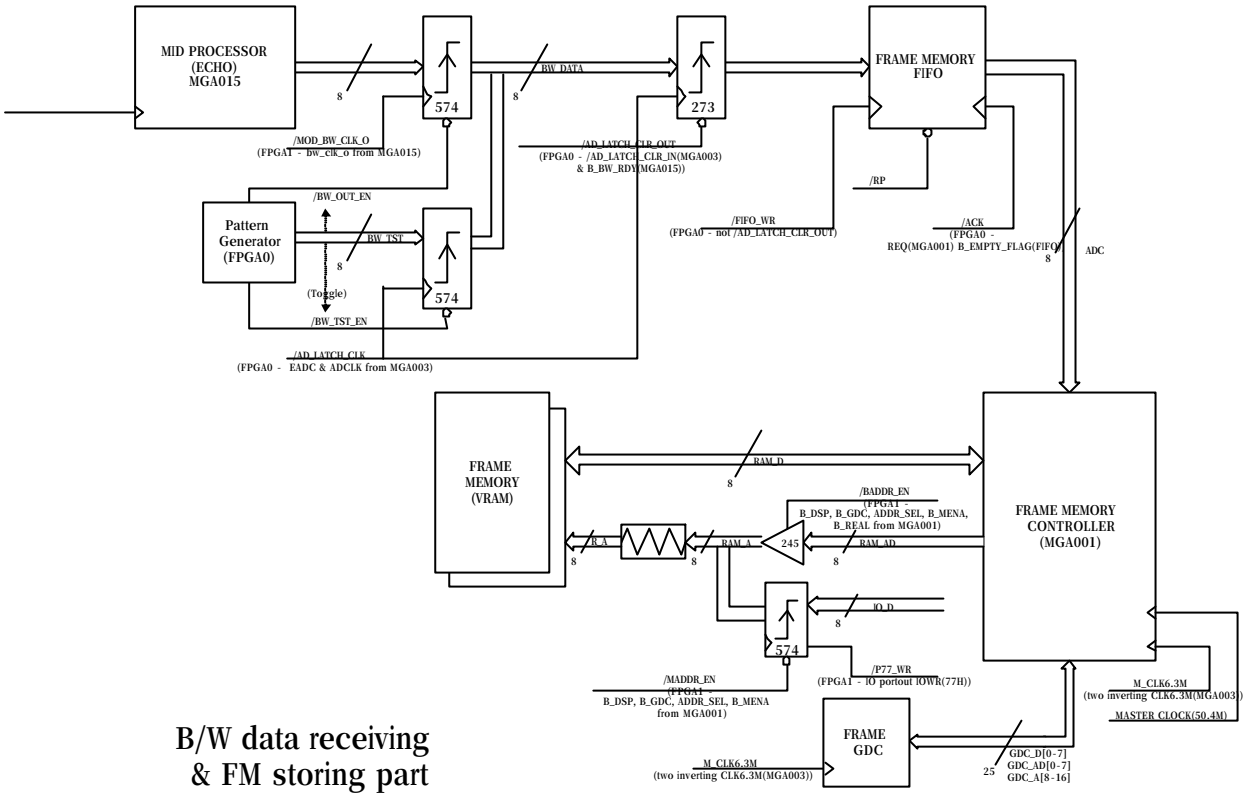
Name	I/O	Description
A[0-15]	Input	HOST Address
AD[0-15]		HOST DATA
RST		8085 CPU RESET
ALE	OUTPUT	DATA ADDRES ENABLE
/IO_W	OUTPUT	IO CHIP WRITE ENABLE
/RD		IO READ
IO_D[0-7]		UPD72020의 DATA BUS
/OL_GDC_RAS		OVERLAY GDC RAS
OL_GDC_BLK		OVERLAY GDC BLK
/OL_GDC_DBIN		OVERLAY GDC DBIN
/OL_GDC_RD		OVERLAY GDC READ
/OL_GDC_WR		OVERLAY GDC WRITE
CLK3.15		POWER CLOCK 3.15Mz
ADDR[0-5]	Input	HOST Address
FE_CTRL_CLK	Input	Front End Control Clock MT8816 Control Clock 16 개 HVSW Clock 24 ea
/FE_CTRL_LE	Input	HVSW Latch Enable
FE_CTRL_RST	Input	MT8816 Reset
FE_CTRL_ADDR[0-5]	Input	MT8816 Address 0-15
FE_CTRL_DATA[0-7]	Input	MT8816 Control AY[0-2]=DATA[0-2] CPSW_DATA,CS = DATA[3] HVSW Control /HVSW_DATA[0-3]=DATA[4-7]
SCANLINE[0-7]	Input	Scanline 0-255
SYNTHETIC	Input	Low : Normal Tx High : Synthetic Tx
CTRL_RESERVED	Input	Reserved Default Low
FREEZE	Input	High : Freeze Low : Real
25.2MHZ	Input	Master Clock 25.2MHZ
/EX_TRG	Input	Exciting Trigger
/B_EOF	Output	Beamforming Data Enable Use it on MPIC MGA015 of DSC

/OF	Input	One Frame
/RP	Input	Rate Pulse
/RPT	Input	Rate Pulse Train
TGC_D[0-7]	Input	TGC Data
T_SBCLK	Output	Battery Clock
T_SBDATA	Output	Battery Data
/CPU_RD	Input	Host Read
EXT_B[0-16]	Output	Beamforming Data
LCDVR_A	Output	LCD Brightness Knob
LCDVR_B	Output	LCD Brightness Knob
GAIN_A7	Output	GAIN Knob
GAIN_B	Output	GAIN Knob
NEAR_A	Output	NEAR Knob
NEAR_B	Output	NEAR Knob
FAR_A	Output	FAR Knob
PRINT_REMOTE	Input	Echo Printer Remote
B_FREEZE_REMOTE	Output	Freeze/Remote The switch on the probe is using for toggle. Using for Freeze, press it short. Using for Store, press it long (over 3secs.)
FP[0-2]	Input	Focal Point FP[2] = Default Low

- NOTE : Refer to Article 5. in chapter 2. [ASIC PIN definition]

3.4 Detail Description

3.4.1 B/W Data Receiving & FM Storing Part



B/W data receiving & FM storing part

3.4.1.1 Mid-Processor (MGA015A)

- Mid-processor plays as converter RF data come from F/E board into BW data that can use in DSC pass through several digital signal processing.
- MGA015A ASIC clock divides system master clock 50.4MHz into 25.2MHz on MGA003 and pass through it to Clock buffer. As the result, it uses 25.2MHz.
- The data of Internal MGA015A is controlled by CPU Portout downloading. Host controller (FPGA1–host data, host address, host_wr, host_rd) works as the download interface.
- RF data, the first TX/RX result come from B/F, is stored SRAM in MGA015A. But external SRAM is necessary to display BW data that generated by summing up the second R/F data of TX/RX result.
- MGA015A makes /BW_CLK_0 that 74HCT574 located on the back stage is to latch the BW data. But because /BW_CLK_0 do not make any clock during /RP blank period, /RP the last data remain in 74HCT574. Thus the first sampling data in /RP enable period is possible to be the last data during hole /RP period. As the result, white spot symptom appears at near part on the image. To remove this symptom, use /MOD_BW_CLK_0 include dummy clock. It clears 74HCT574 data within RP blank period.

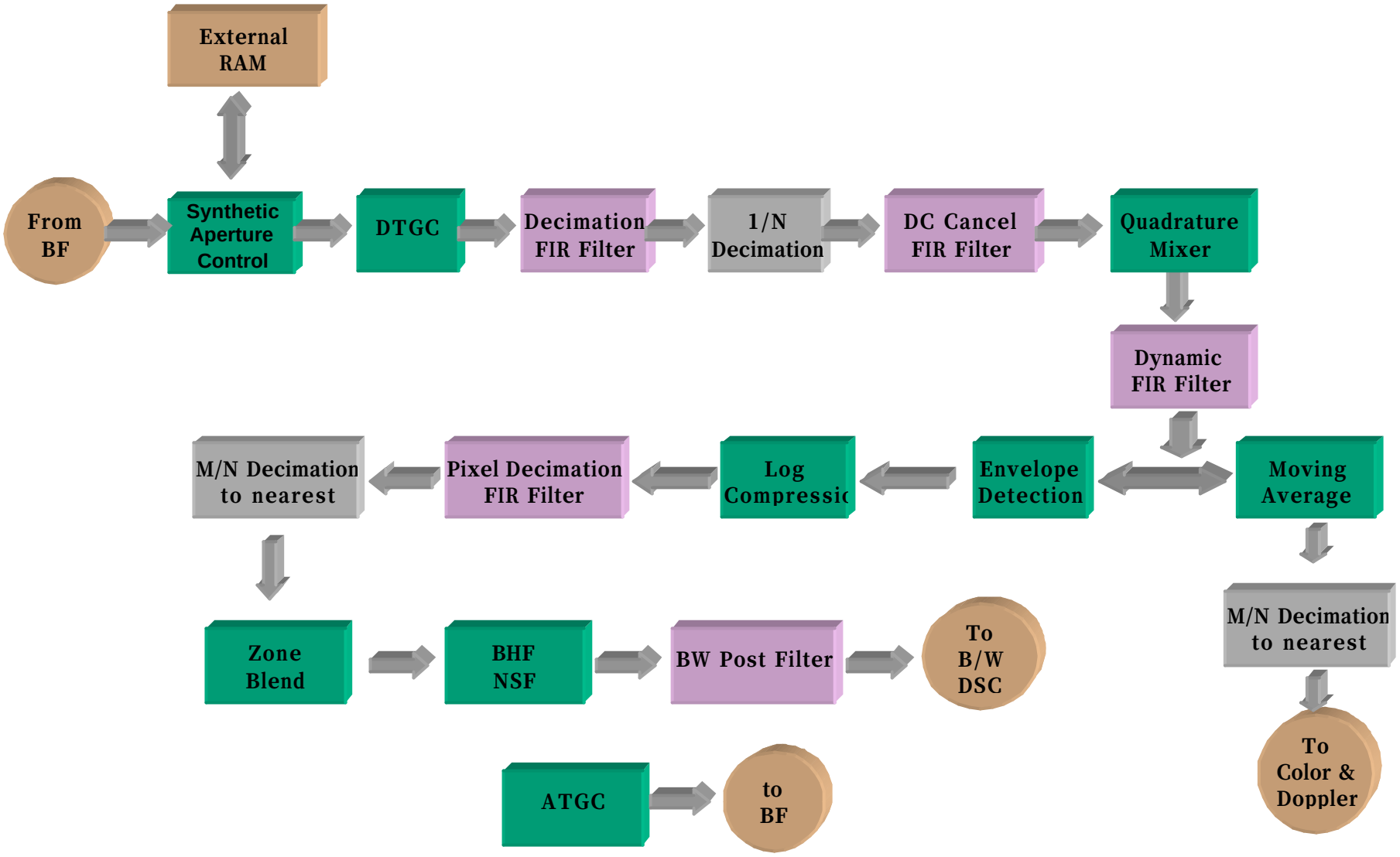


Figure 1. Mid-Processor (MGA015)

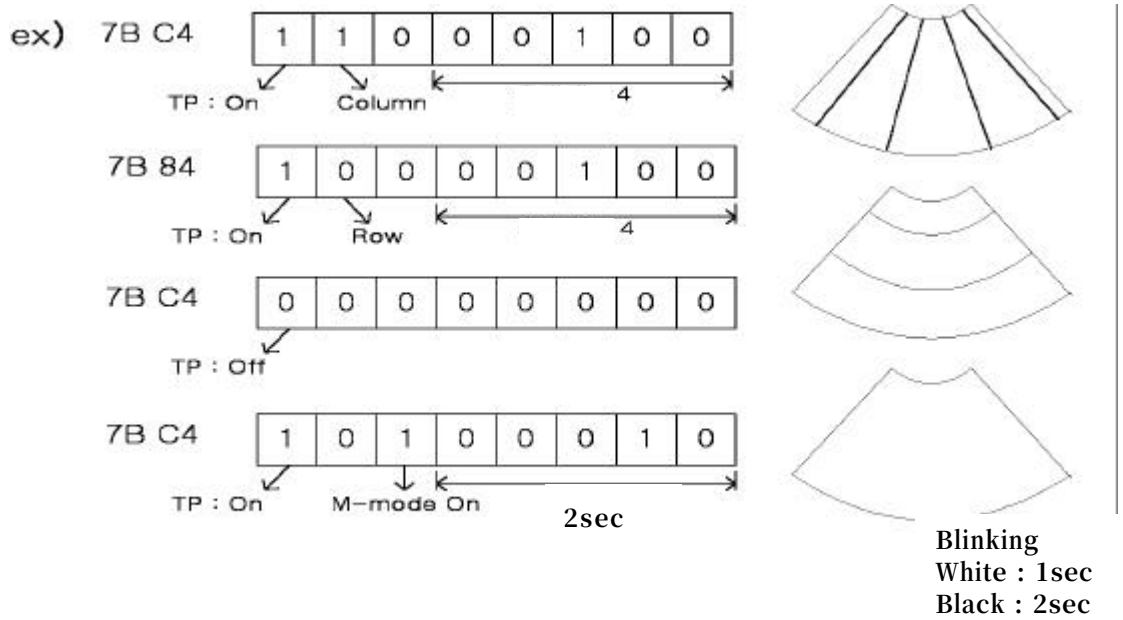
3.4.1.2 Pattern generator

- FPGA0 drives Pattern generator.
- Pattern generator is a block that makes a test pattern to check DSC function whether it works well or not.
- According to test pattern on/off, change from /BW_OUT_EN to /BW_TST_EN.
- Test pattern on/off is set by CPU portout.

[Test pattern type and the bit value of 7BH port]

Bit7 : test pattern on/off Bit6: Row/Colume selection

Bit5 : m-mode test pattern on/off Bit4~Bit0: increment value



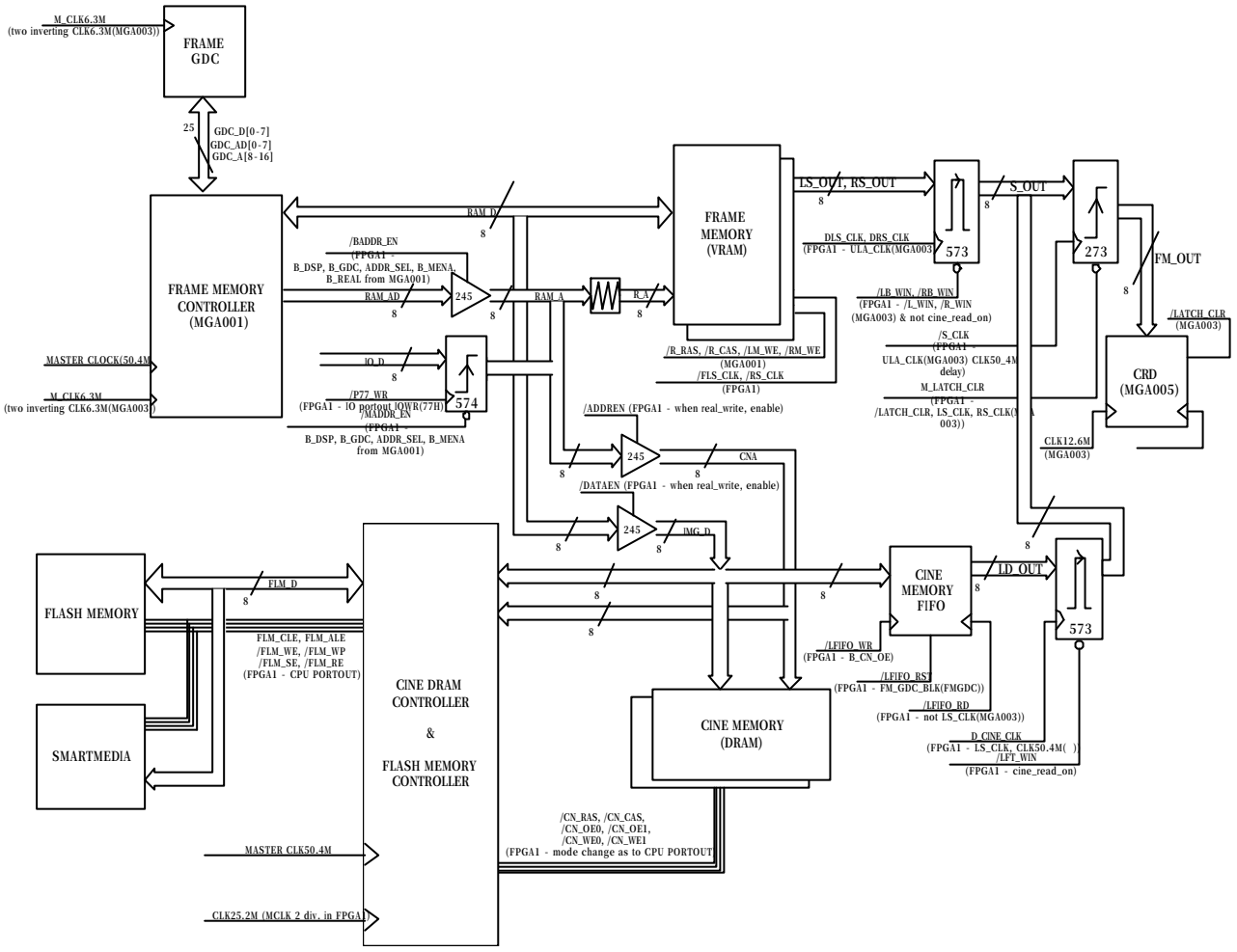
3.4.1.3 Before FM controller (MGA001)

- BW data sampling get according to /AD_LATCH_CLK.
- /AD_LATCH_CLK is a clock that generated by masking ADCLK come form MGA003 into /EADC.
- Master reset of 74HCT27 is achieved by /AD_LATCH_CLR_OUT. /AD_LATCH_CLR_IN signal generated by MGA003 match the BW data sampling point as masking /BW_RDY.
- Frame memory FIFO stores the BW data with scanline direction temporary and support to write the data on the Frame memory. To match the timing point, FIFO write clock uses an inverter type of /AD_LATCH_CLK.
- The clock that read Frame Memory FIFO receive the BW data using /EMPTY_FLAG. /ACK is a clock to read Frame FIFO and receive BW data using REQ and /EMPTY_FLAG.
- REQ represent whether MGA001 is ready to BW data process and /EMPTY_FLAG check whether the FIFO is empty.

3.4.1.4 FM controller (MGA001)

- MGA001 for exclusive use of FMC design to generate several signals under ASIC Technology.
- The related signals of Frame memory are DATA & Address Bus, Control signal such as /RAS , /CAS, /OE, /WE, etc.
- Data Bus of Frame memory is connected with Frame Average Logic at chip inside and average factor is 6ea. Mysono201 used 4ea among them.
- MGA001 use two clocks. Master clock is 50.4MHz and 6.3MHz clock same as Frame GDC. In case of 6.3MHz clock, use 6.3MHz half clock of MGA003 with the result of passing through inverter twice since clock slew rate is not fine.
- Frame GDC generate the standard signals such as FM_GDC_HS, FM_GDC_BLK, /FM_GDC_RAS, /FM_GDC_DBIN and perform the factor data and functions. However, for /FM_GDC_RAS signal, use /FM_GDC_RAS_LATCH signal with latching the rising edge as 50.4MHz to match the necessary point at MGA001
- FMC is connected with address bus and data bus for Frame memory.
  In M-mode, to store a designated scanline data in a designated FM address, the latch that portout the address form CPU is connected with address bus.
- M mode CPU portout latch output and 245buffer output of FMC address bus are working as either enabling or switching by BADDR_EN and /MADDR_EN that use integrating the signals come from MGA001 such as /DSP, /GDC, /ADDR_SEL, /M_ENA, /REAL according to mode status.

3.4.2 FRAME MEMORY & CINE MEMORY FLASH MEMORY PART



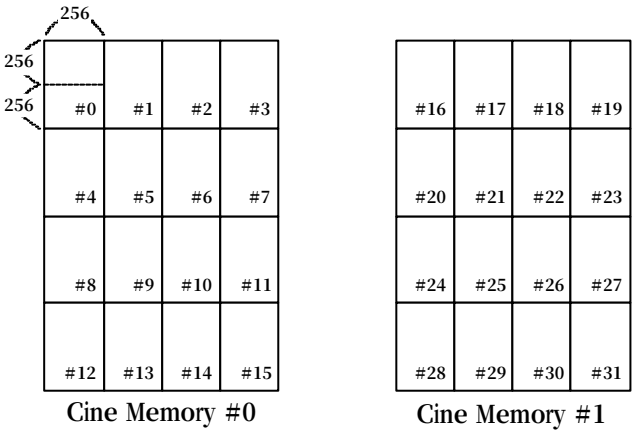
3.4.2.1 Frame Memory (VRAM)

There is two Frame Memory type, RM and LM.

	B – MODE	B/M – MODE	B/B - MODE	M-Mode
LEFT Frame Memory	B	B	LB	Not used
RIGHT Frame Memory	Not used	M	RB	M

- Operation for writing on Frame memory is achieved by MGA001 control signal such as /R_RAS, /R_CAS, /LM_WE, /RM_WE, etc.
- Operation for reading on Frame memory is recognized by Display clock at SAM. (cf. VRAM = DRAM + FIFO) And latch it by 573 latch data.

3.4.2.2 Cine Memory (DRAM)

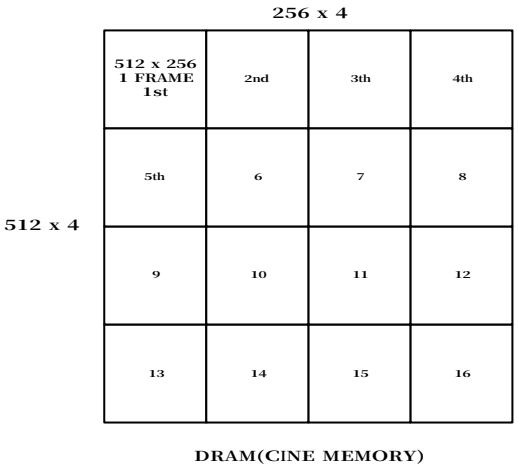


Cine Memory #0 Cine Memory #1

- Cine memory store total 32 frame and use for image store include Cine image.
- Cine memory controller (FPGA1) controls the cine memory.
- Under Real mode, Cine memory is stored with Frame memory at the same time using the data come from FMC directly and control signal such as /R_RAS, /R_CAS, /RM_WE, /LM_WE. But under Cine mode, data is output from Cine memory instead of FM and connected with Cine memory FIFO of DRAN back stage to work as VRAM.
- Frame memory data path and Cine memory data path meet at Data bus, called S_OUT.

  And 573 latch is enable by toggle signal of /LFT_WIN, /LB_WIN (or /RB_WIN) according to mode.

DRAM Memory(CINE Memory) Map



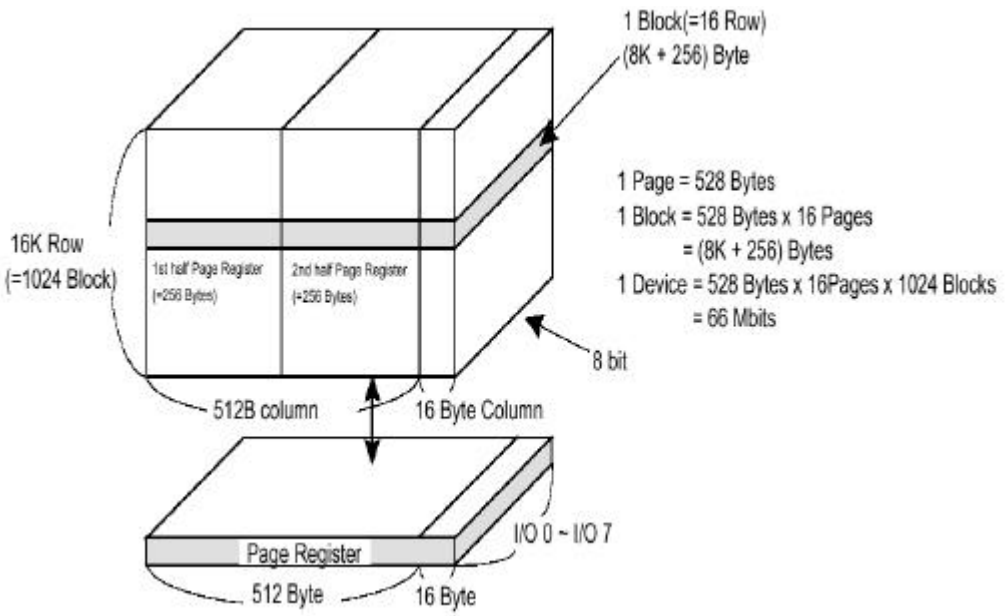
* mysono201 내부에는 2개의 DRAM이 있고 한개당 16개의 frame이 들어 갈 수 있다. 그러므로 CINE는 총 32장을 제공한다.

* CINE memory에 있는 image를 FLASH memory로 저장(store)하는 방법은 두개의 ROW(256 bytes) 가 한조가 되어 한개의 page(512 bytes)에 저장 된다. 이렇게 총 256개의 조가 저장되고 1개의 block이 16page이므로 총 16개의 block이 필요한 샘이다.

.

Figure 1. Cine Memory Map

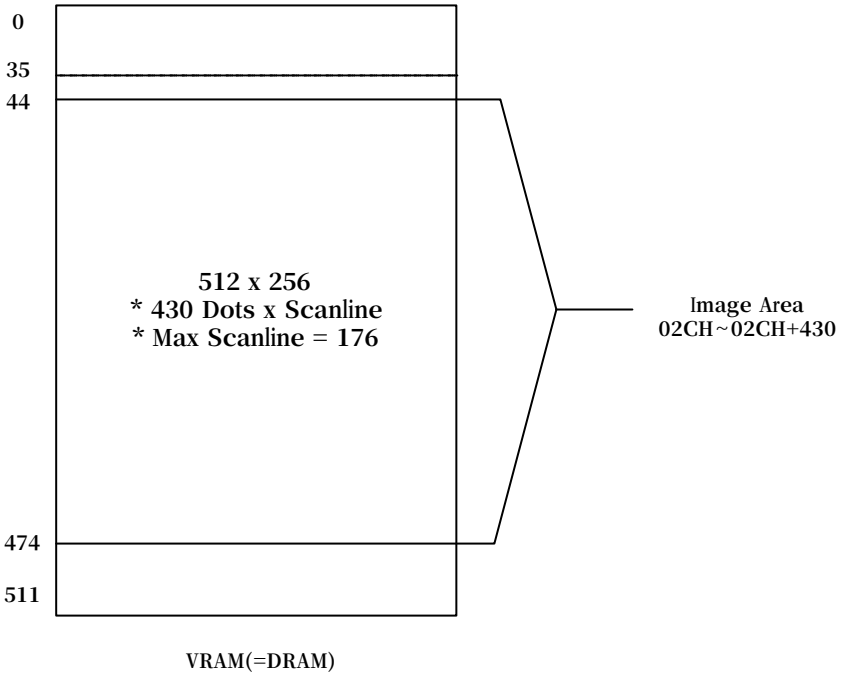
3.4.2.3 Flash Memory



Flash memory is a NAND type and use a backup memory for image saving.

- It is controlled at Flash memory controller (FPGA 1) generated by CPU Portout.
- Flash memory control is achieved at Flash memory controller (FPGA1) under CPU portout. But as CPU controls by the control signals such as FLM_CLE, FLM_ALE, /FLM_WE, /FLM_RE that are selected through CPU portout, Flash memory controller work as simple interface.

1 Frame in Flash

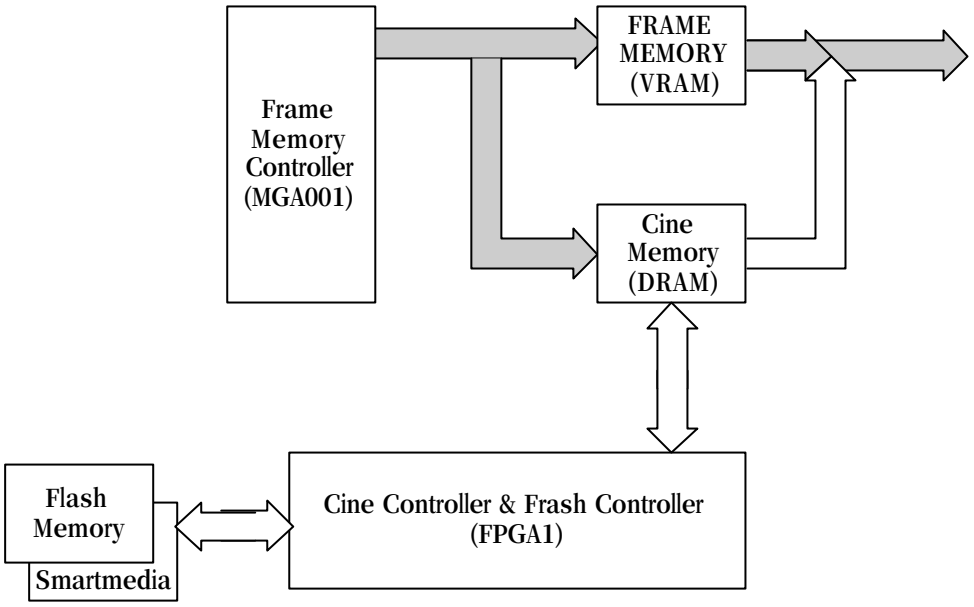


* VRAM에서 RAS Addr기준으로 43까지는 Image가 없는 영역이다.
이 것은 256 x 43 bytes 만큼이 비어 있다는 이야기이고,
이 것은 256 x 32 (512 x 16 = 1 block), 즉 총 16 block 중 1번째 block에는 image data가 존재하지 않는 것을 의미한다.
그러므로 첫번째 block은 다른 용도로 사용이 가능하며,
현재 이부분에는 ULA, System parameter, Report data, 화면 Display data 등이 들어가 있다.

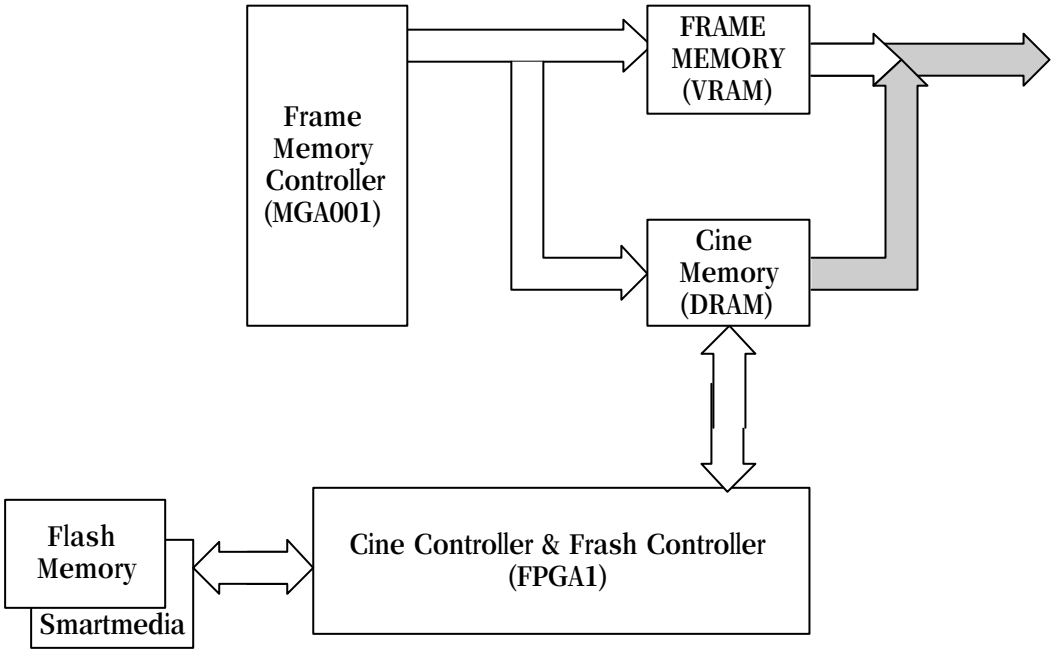
Figure 2. Fresh Memory Map

3.4.2.4 Memory Path by Mode

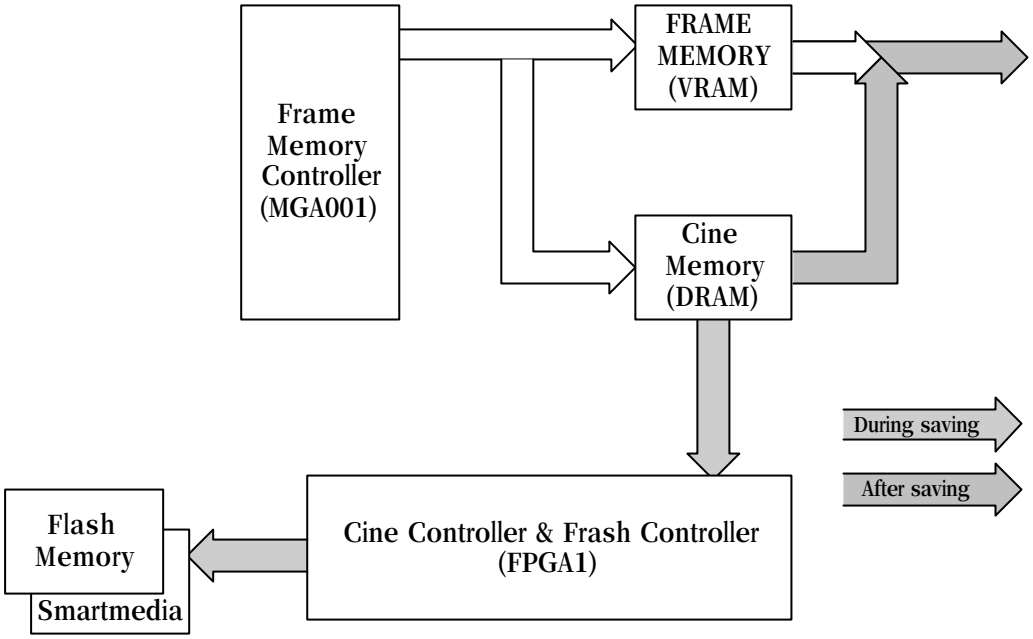
- Real Mode



- Cine Mode

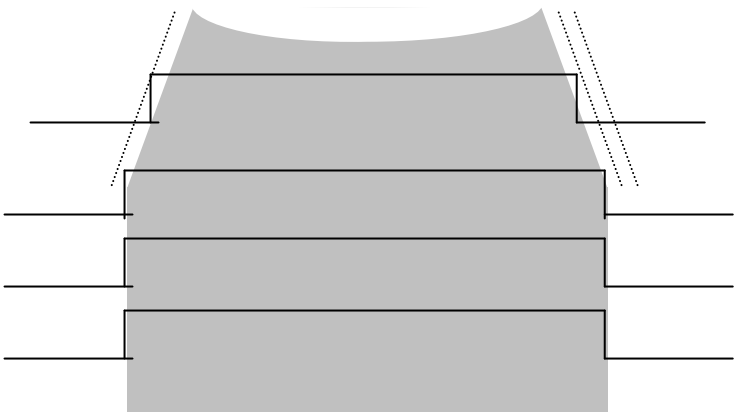


- Flash Memory Save



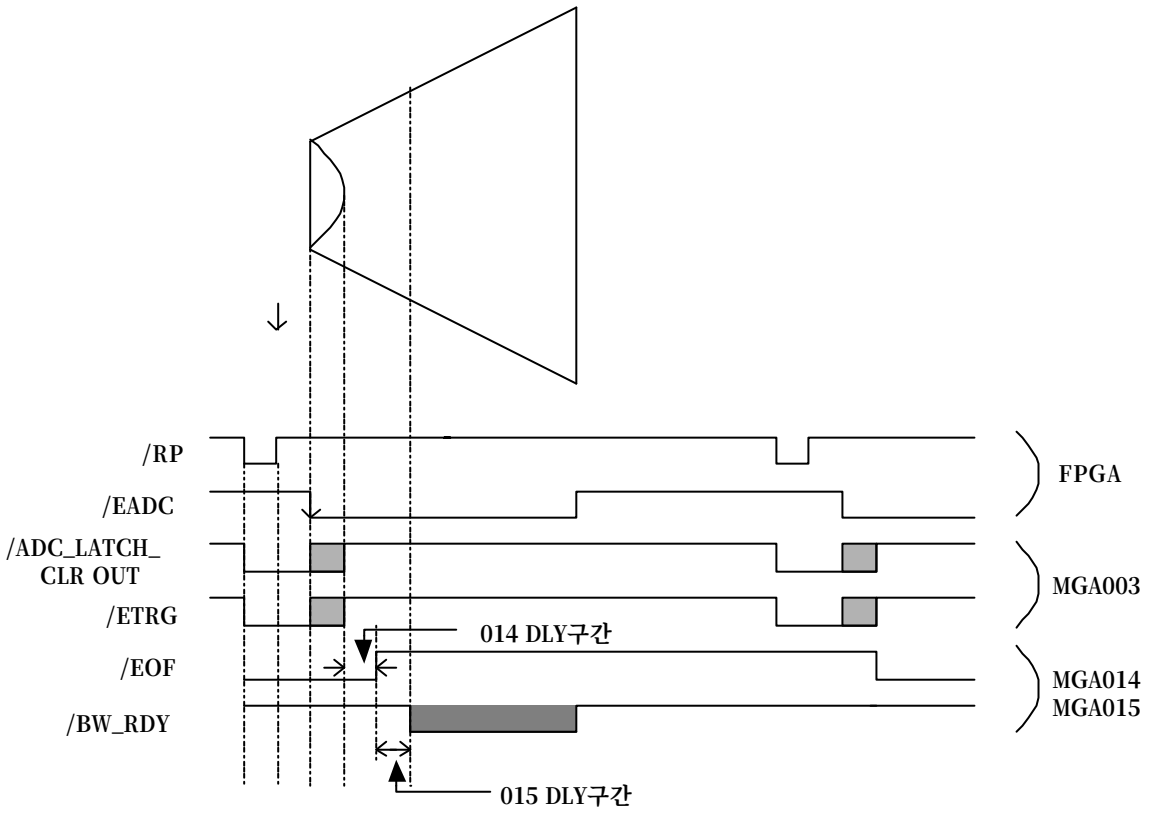
3.4.2.5 Scanline Masking Window

- When change the Mode (BM→B or BB→B) or control the Gain, an unsuitable image display on the monitor due to save unsuitable data out of image area since VRAM address control unstable
- Display clock is a regular according to probe element.
  It occurs as much as scanline.

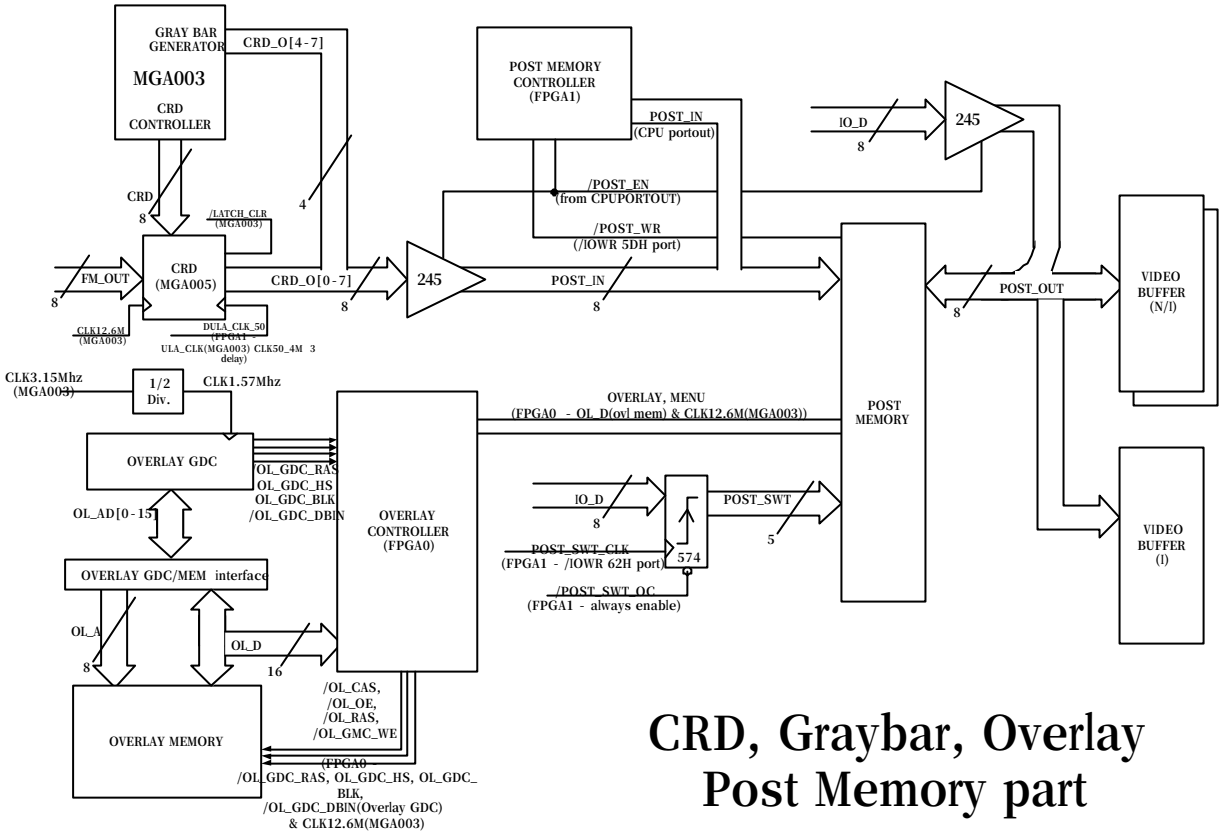


Display clock is constant by probe element. That is to say, Display clock generates as much as scanline. Thus, if count a number of scanline and use it for the Master reset of 74HCT27 on the front stage of MGA005, the dummy scanline problem can be solved by pass through only the data under image area. The other data out of image area is reset.

However, due to only the display clock is available that pass through the disable period of /LATCH_CLR, make a new signal of /M_LATCH_CLR and use to /MR in 74HCT273.



3.4.3 CRD, Graybar, Overlay Post Memory Part



CRD, Graybar, Overlay Post Memory part

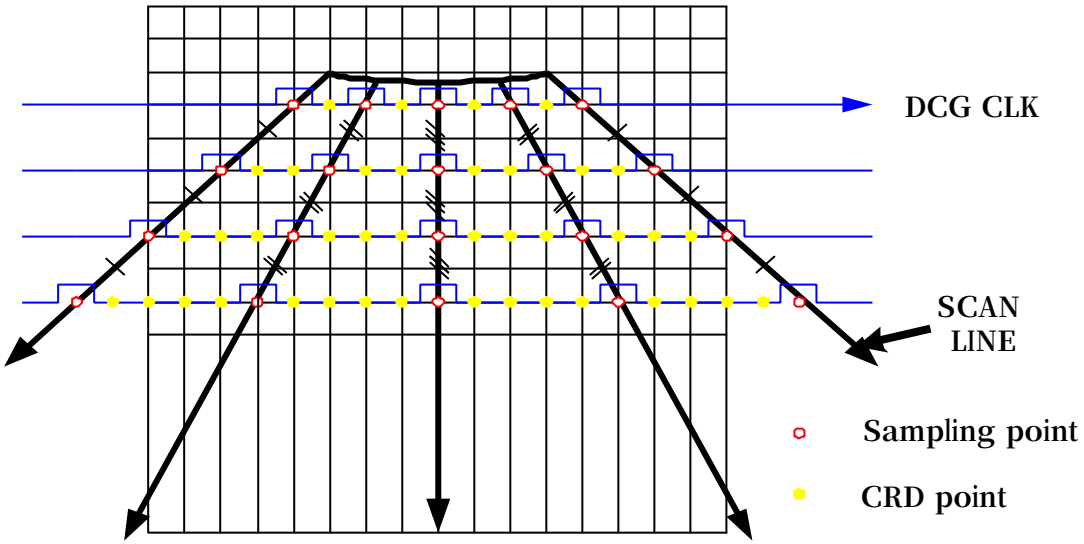
3.4.3.1 CRD

- Display the ultrasound image of the Convex probe on the monitor, system recognize and read the data of Frame memory by Display clock that generated on DCG (Display Clock Generator).
- One scanline will be interpolated to the Horizontal Sync (HSYNC) as fixed Scanline number from the system and the frequency of interpolation DCG Clock will be changed whenever the HSYNC is generated according to the Vertical Sync (VSYNC). The image from Far-Field is interpolated as low frequency DCG Clock and there is a possibility of mosaic problem on actual display.
- The CDR Logic uniformly converts the frequency of signal as 12.6 MHz that input to the Monitor by 1D interpolation to horizontal axis for the data that is interpolated from the Frame Memory as Monitor Dot Clock 12.6 MHz.
- MGA003 gives a parameter required for CRD, treat it as Dot Clock.
  Input clock receive the data using DULA_CLK_50.
- The parameter that need to CRD get from MGA003, and process it by Dot clock. But the received clock gets the data by using DULA_CLK_50 that delays the ULA clock.

3.4.3.2 Graybar

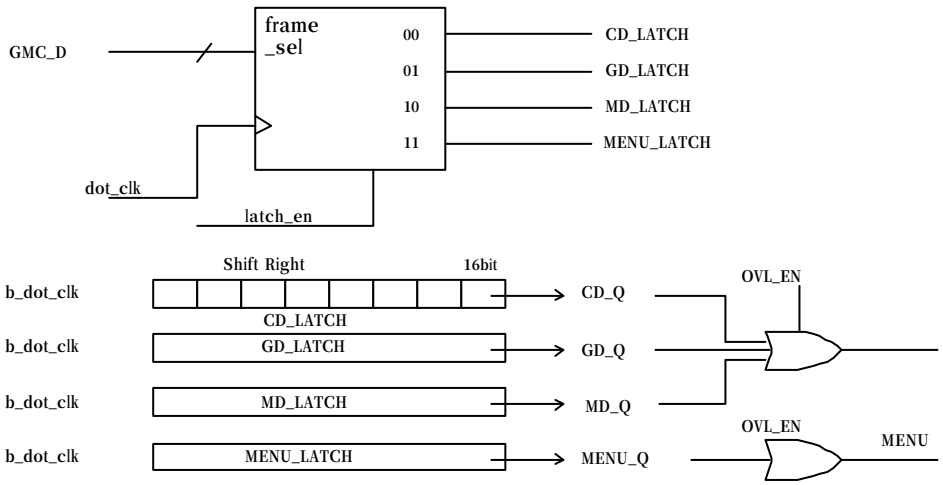
- Graybar generate 4 Bit data come from MGA003.
- The signal related with Graybar is as follows;
  - GRAY_OE : Controlled by MGA003 and manages the output point of Graybar data
  - CRD_O[4-7] : Graybar data and share both MGA005 output bus and upper 4bit.
  - /BMODE_EN : It is a Enable signal to control data output of MGA005

The basic schema of Graybar is as follows;

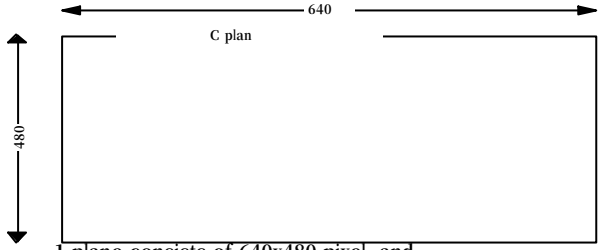


3.4.3.3 Overlay

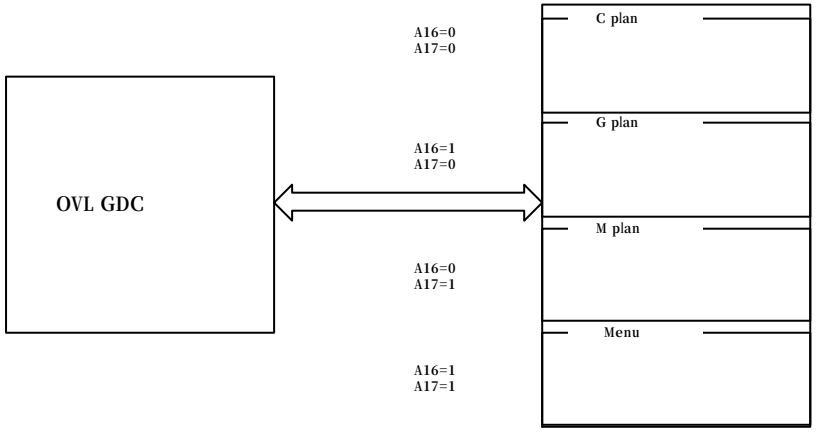
- Overlay data is generated by using overlay memory with controlling overlay GDC by CPU. It goes to FPGA0 and processed to C, G, M, MENU then the final output is overlay data and menu data. The data processing method is described as below block diagram. GMC-D is the data that is processed by overlay GDC in overlay memory and 12.6 MHz of dot_clock is used.
- This data is serially output from FPGA0 and combined with image in post memory.



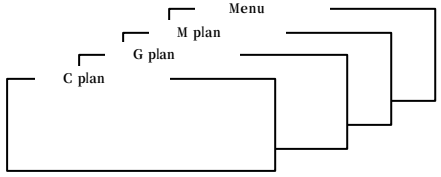
3.4.3.4 Overlay Control Schema

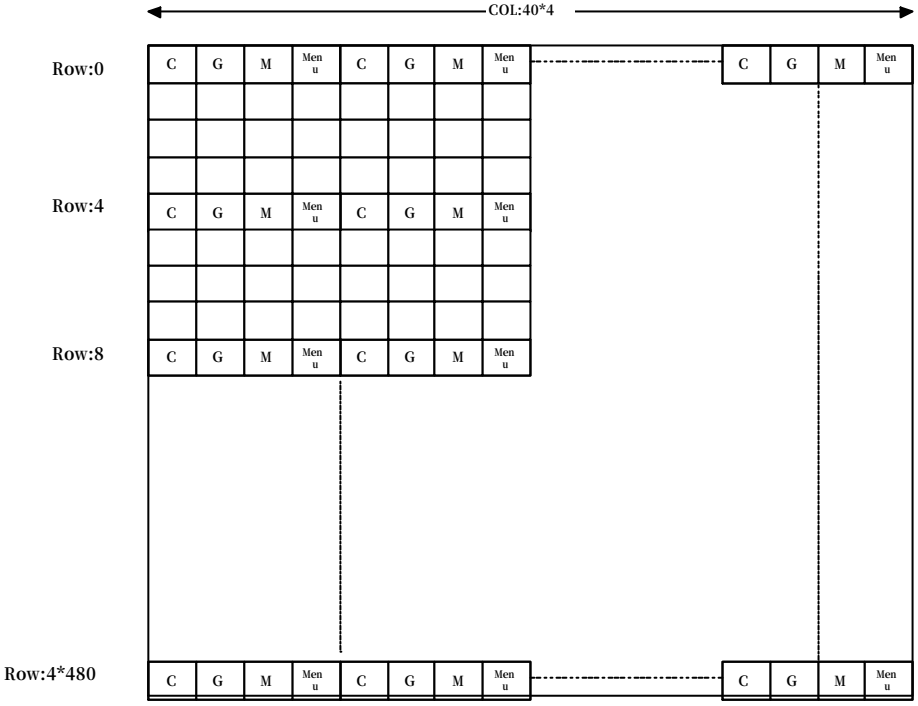


1 plane consists of 640x480 pixel, and
overlay data is mapped by 1bit to 1 pixel.
1 picture=(40 COL x16)x480 Row



GDC manage the external RAM address like above picture,
and each picture plane is overlaped like following .





<DRAM Memory allocation>

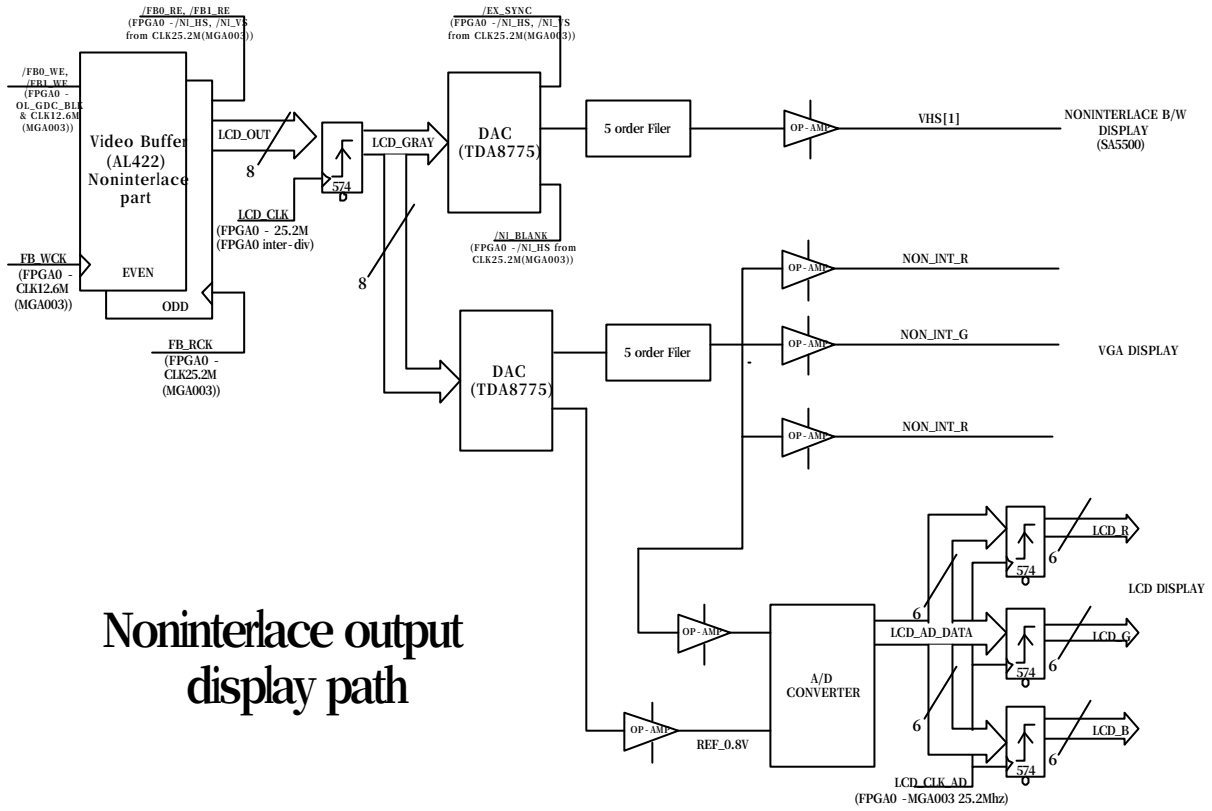
When GDC write to DRAM:
Column:
DRAM_A0 <= OL_AD16
DRAM_A1 <= OL_AD17
Row:
DRAM_A0 <= 0
DRAM_A1 <= 0

When GDC write to DRAM:
Column:
DRAM_A0,1: 0~3 in a GDC_RAS pulse
Row:
DRAM_A0 <= 0
DRAM_A1 <= 0

3.4.3.5 Post Memory

- Post memory consists of SRAM. It combines an image data and an overlay data into the data displayed on the screen.
- It could change the display settings such as Gamma setting by control the data in Post memory.

3.4.4 Noninterlace Output Display Path Port



Noninterlace output display path

3.4.4.1 Function

→ Non-Interlaced B/W Monitor

(Recommended by Medison. Medison supplies this monitor.)

→ VGA Monitor (We does not fixed specify model. You can use any type.)

→ NTSC or PAL VHS Monitor (We does not fixed specify model. You can use any type.)

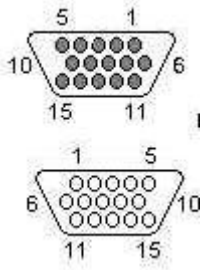
→ NTSC or PAL VCR Record (Only Record. Does not support VCR Play Function.)

→ B/W Echo Printer

3.4.4.2 VGA

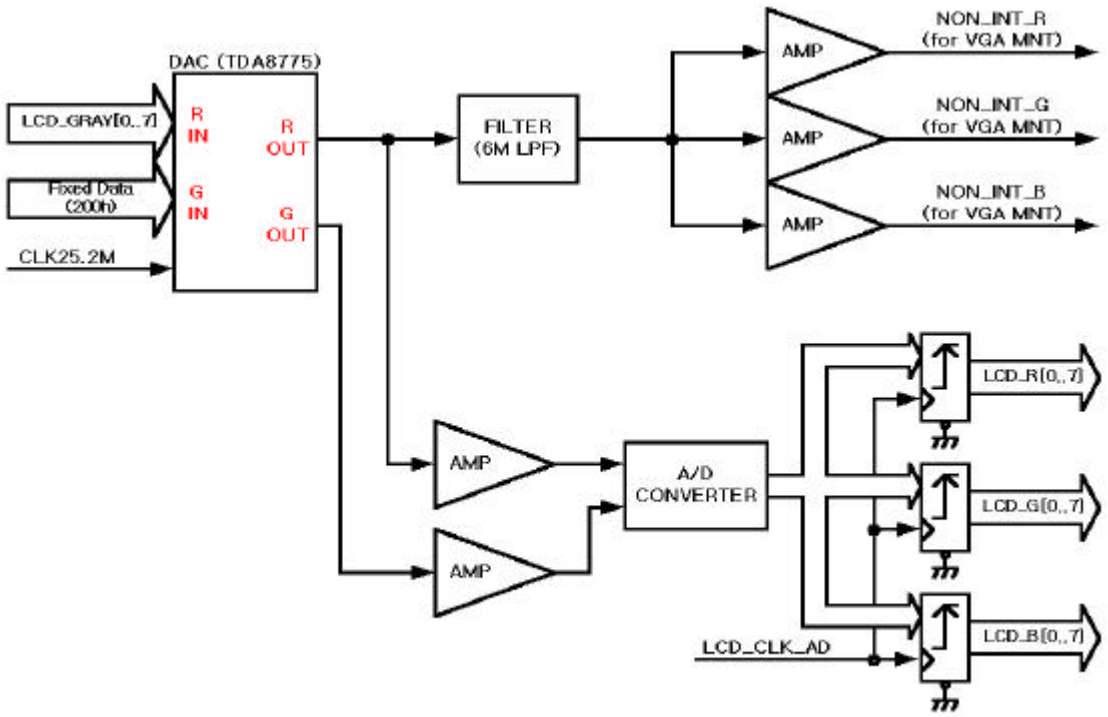
Generally it has same specification as VGA Signal. It consists of R, G, B, HS, VS.

Pin array meets a standard and a detail wiring diagram is as follows;



15 PIN HIGHDENSITY D-SUB FEMALE at the System.
15 PIN HIGHDENSITY D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED	→	Red Video (75 ohm, 0.7 V p-p)
2	GREEN	→	Green Video (75 ohm, 0.7 V p-p)
3	BLUE	→	Blue Video (75 ohm, 0.7 V p-p)
6	RGND	→	Red Ground
7	GGND	→	Green Ground
8	BGND	→	Blue Ground
13	HSYNC	→	Horizontal Sync (or Composite Sync)
14	VSYNC	→	Vertical Sync



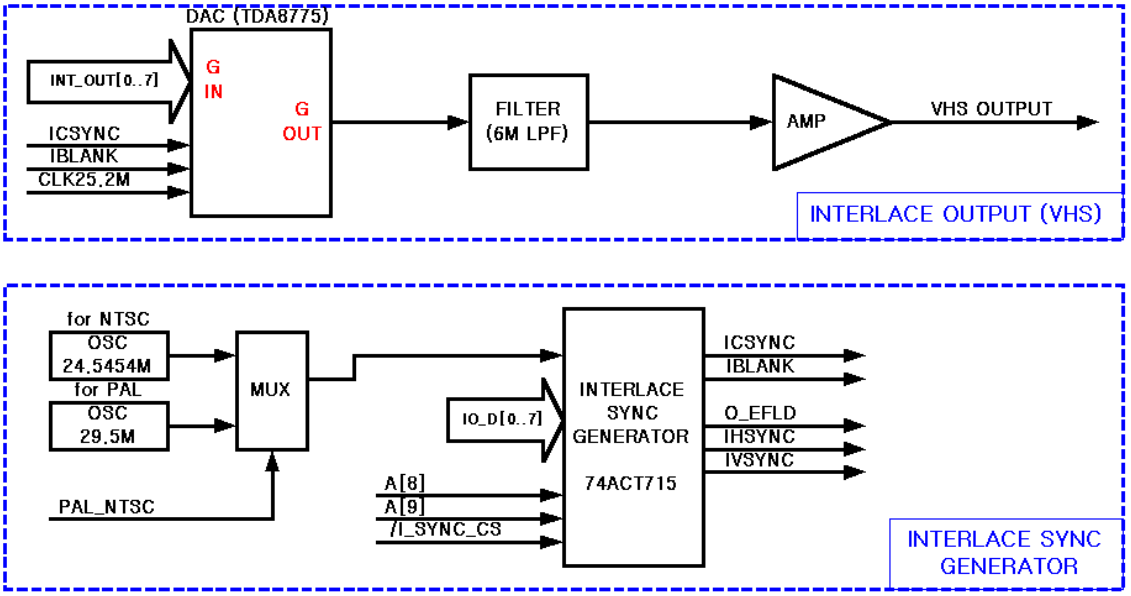
< LCD & VGA VIDEO OUTPUT PATH >

1) Video signal converted D/A at TDA8775 (DAC) transfer output signal of VGA Monitor through 6M LOW-PASS-FILTER.

2) Each value of R, G, B is amplified 1.5 times at EL4393 OP-AMP and is output.

3) HSYNC, VSYNC output the FPGA signal by Buffering through 74HCT245 without amplification.

3.4.4.3 VHS



< VHS VIDEO OUTPUT PATH >

1) Video signal converted D/A at TDA8775 (DAC) transfer output signal of VHS Monitor through 6M LOW-PASS-FILTER.

2) SYNC for INTERLACE used Programmable Sync Generator made by 74ACT715. As booting INTERLACE SYNE, CPU (8085) select the data by downloading according to VIDEO type whether it is NTSC or PAL. Please refer to below information regarding how to control it and the Table for Down Load Data.

3) The Clock used this generator is different from VIDEO type.
In case of NTSC, it is used 24.5454M. Otherwise in case of PAL, it is used 29.5M.
They are selected by muxing of PAL_NTSC signal that produced on CPU

3.4.4.3.1 Control 74ACT715

1) DATA is located in "KERNEL.SRC" SOURCE.
2) SYNC could make by programming register number set in 74ACT715.
3) DOWN LOAD DATA table is as follows.

REGISTER NUMBER	DESCRIPTION	DOWN LOAD DATA	
		NTSC	PAL
00	Status Register (Hsync, Vsync Polarity = Active H, Non-Interlace)	0580H	0580H
01	Horizontal Front Porch	0032H	00C0H
02	Horizontal Sync Pulse End (HFP+HSYNC WIDTH)	00A6H	0100H
03	Horizontal Blank Width	0118H	0260H
04	Horizontal Period	0618H	0760H
05	Vertical Front Porch	0009H	0047H
06	Vertical Sync Pulse End (VFP+VSYNC WIDTH)	0011H	004DH
07	Vertical Blank Width	002DH	0091H
08	Vertical Period (1frame)	020DH	0271H
09	Equalization Pulse End (HFP+Equalization Pulse Width)	0060H	0074H
10	Serration Pulse End (HFP+HPER/2-HSERR+1)	02BEH	0350H
11	Equalization & Serration Pulse Vertical Start	0001H	0041H
12	Equalization & Serration Pulse Vertical End	0019H	0053H
13	Vertical Interrupt Activate Time	0029H	0029H
14	Vertical Interrupt Deactivate Time	020EH	0272H
15	HGATE Delay	0026H	002EH
16	HGATE Enable (HSYNC)	009AH	00BAH
17	VGATE Delay	0001H	0001H
18	VGATE Enable (VSYNC)	0015H	0015H

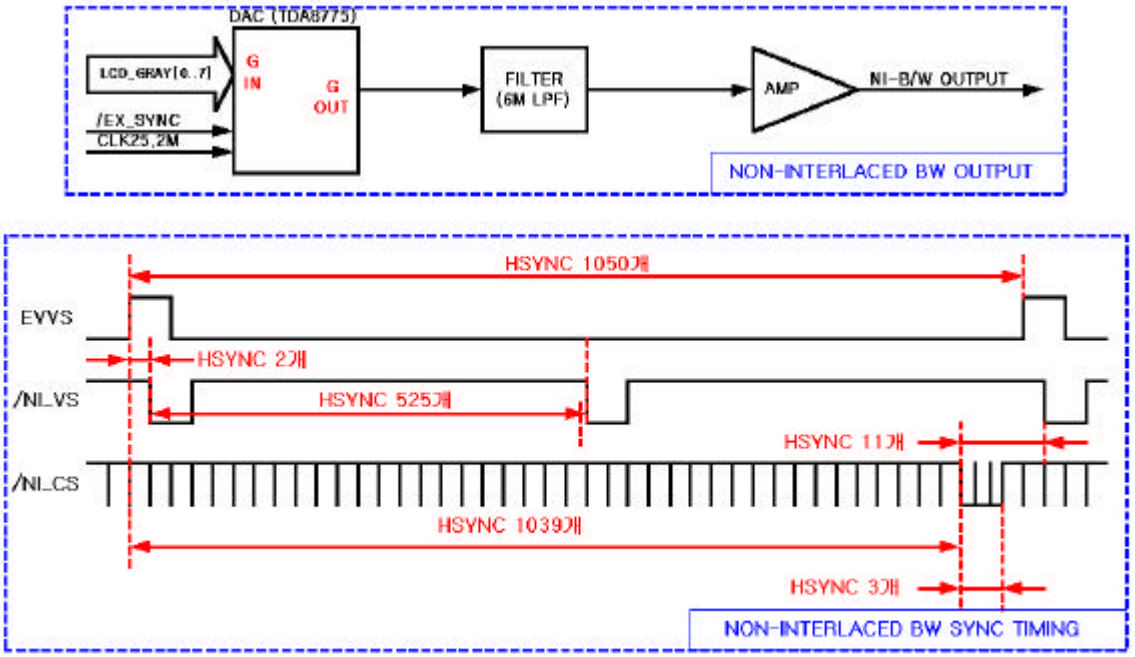
4) To make a stable initialization, do data Port Out on Register no.0 lately after Register Port Out Sequence from 1 to 18.
5) How to control horizontally the position of screen (move it left and right) :

Register 4 controls the HSYNC cycle and register 3 controls the start point of Blank (that is the begging point of image display). Change the value both of them as suitable and be careful that "No.4 register – No.3 register" is always 500H. It is to maintain the Blank width as 640 DOT constantly.

1) How to control vertically the position of screen (move it up and down):

Register 8 controls the VSYNC cycle and register 7 control the start point of Vertical Blank. Change the value both of them as suitable and be careful that “No.8 register – No.7 register” is always 1E0H.

3.4.4.4 Non-Interlaced B/W (NI-B/W)



< NON-INTERLACED B/W VIDEO OUTPUT PATH >

1) Video signal converted D/A at TDA8775 (DAC) transfer output signal of NI-B/W Monitor through 6M LOW-PASS-FILTER.

2) What is NI-B/W?

   Using the NON-INTERLACE type even though it has one signal line including both SYNC and Signal such as general INTERLACE.

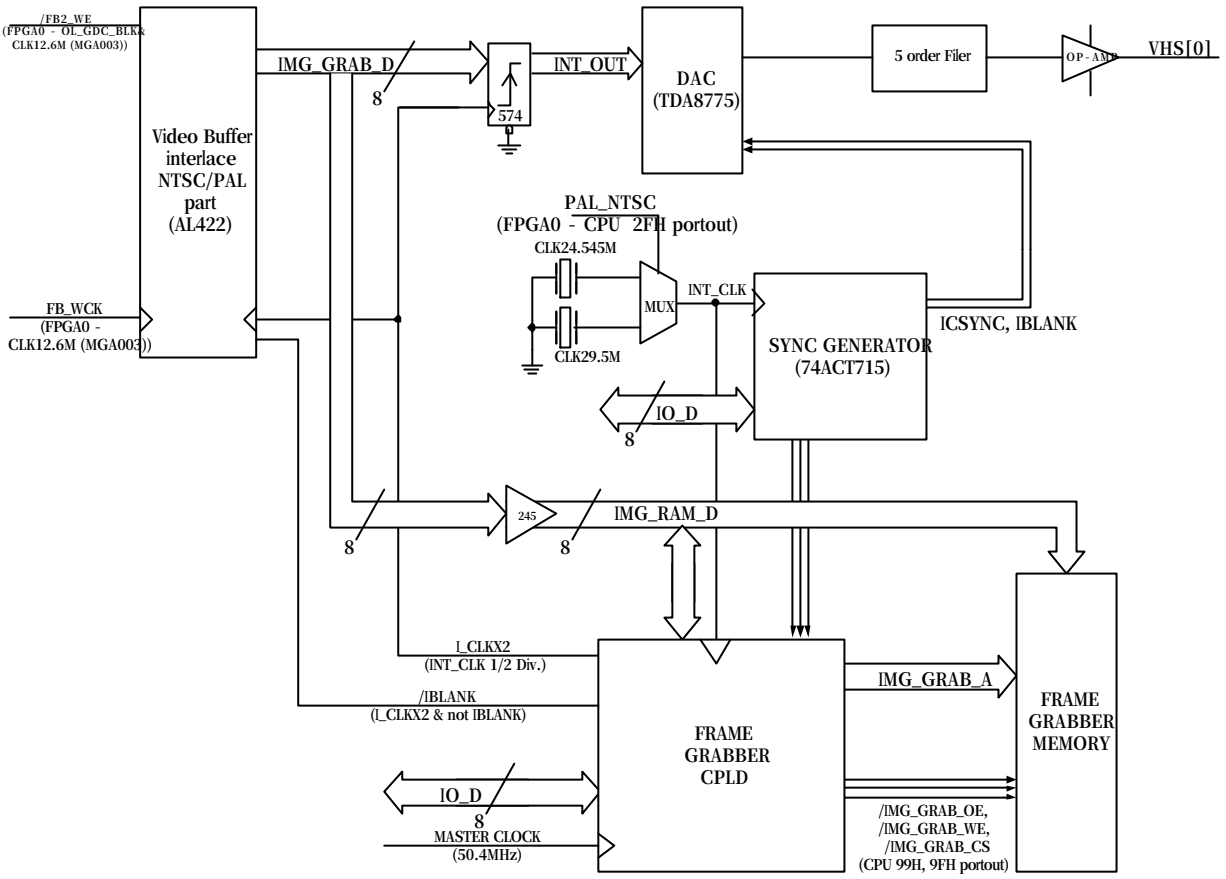
   It combines the strength each one to make less image vibration than VHS or RF Monitor and better contrast than VGA monitor.

3) Monitor is the same as SA5500 monitor. Only change the case for external usage.

4) Concept of SYNC Generation is described above figure.

   VSYNC can detect during “HSYNC 3” term of the monitor for control the image position to the center. That is to say, detect it faster than EVVS.

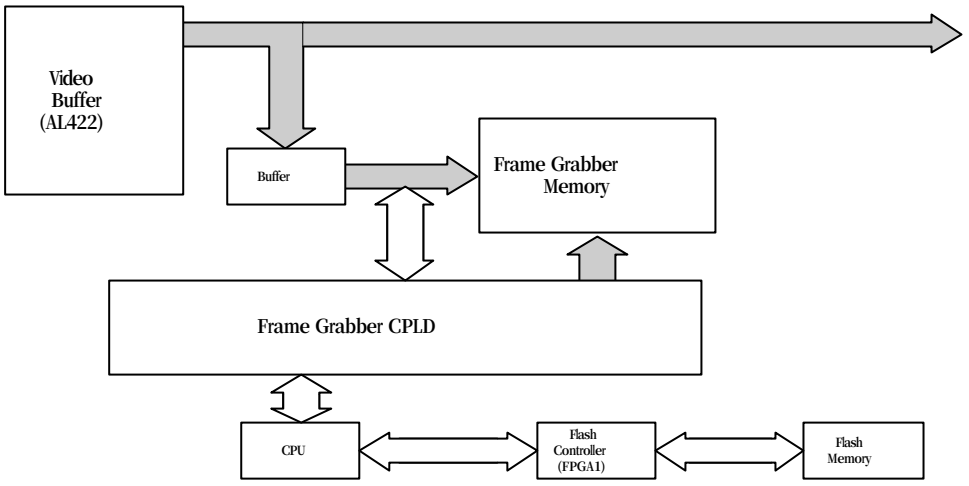
3.4.5 Interlace NTSC/PAL Display Part



Interlace NTSC/PAL Display part

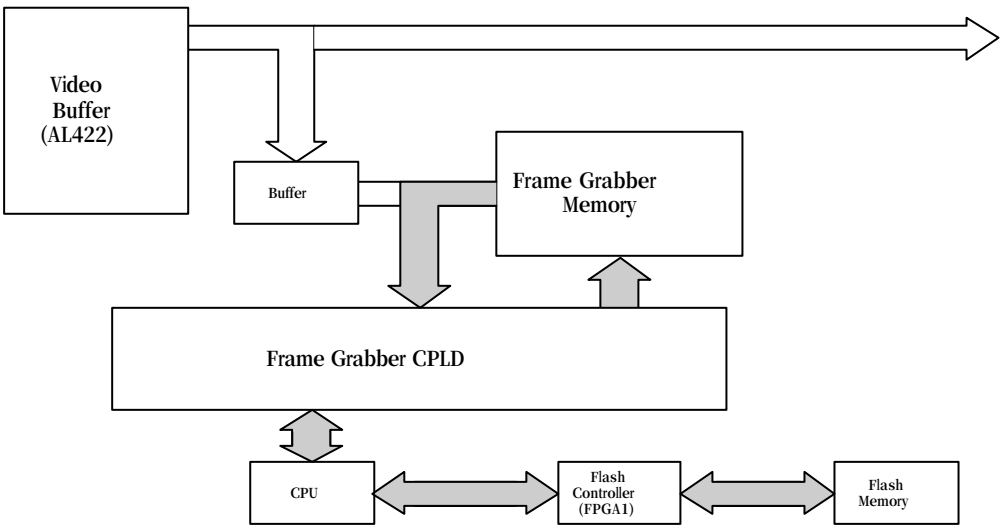
3.4.5.1 Frame Grabber CPLD & Memory

- Frame grabber continuously upgrades the data of 640X480 to FGM (Frame Grabber Memory) in real mode. When input new frame grab, stop to upgrade and change the mode to CPU access mode, then transfer the FGM data into Flash memory under controlling by CPU.



Real Mode

[Figure. Real Mode] FIGURE) Real Mode



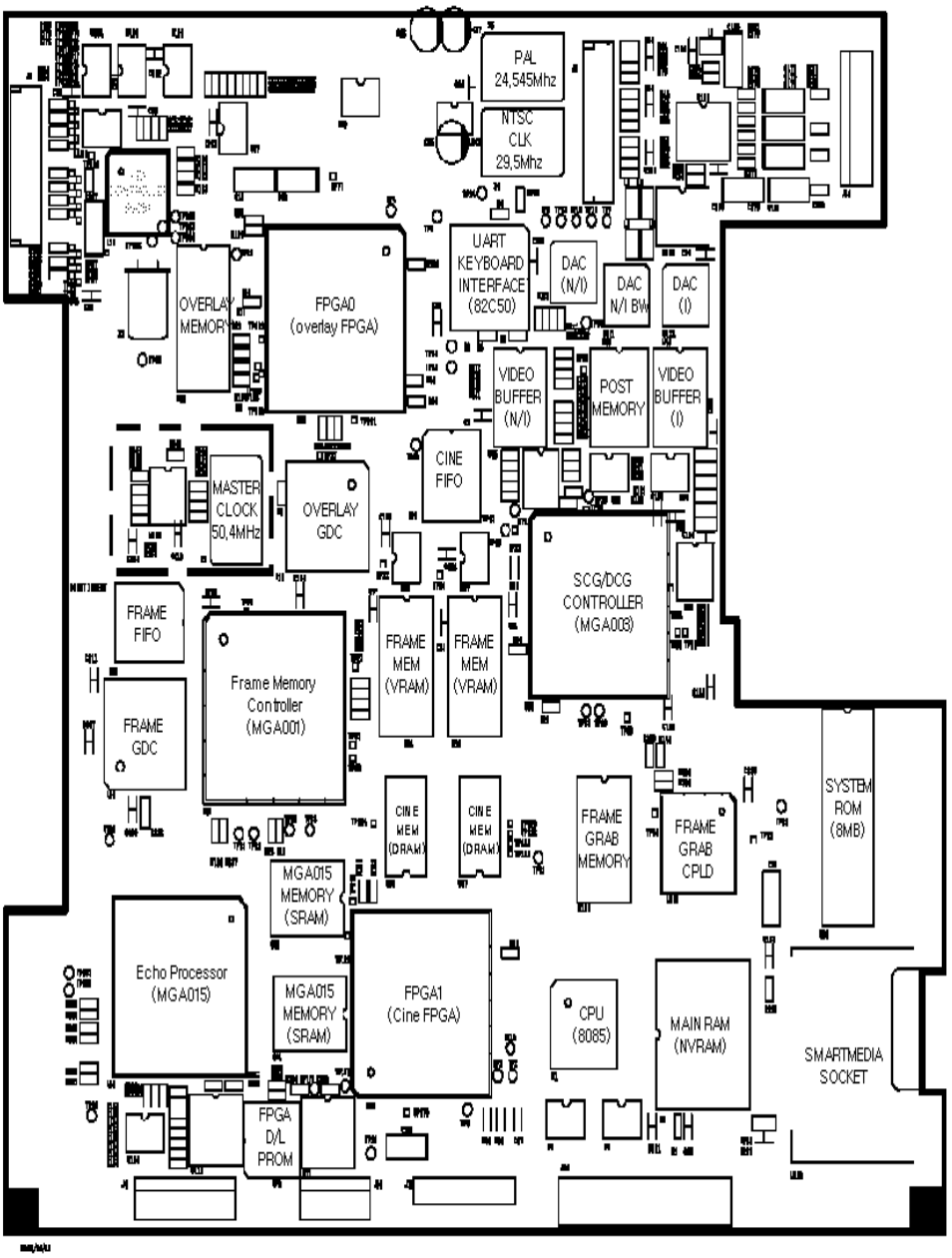
Frame Grab Mode

[Figure. Grab Mode]

3.5 PCB Board Lay Out

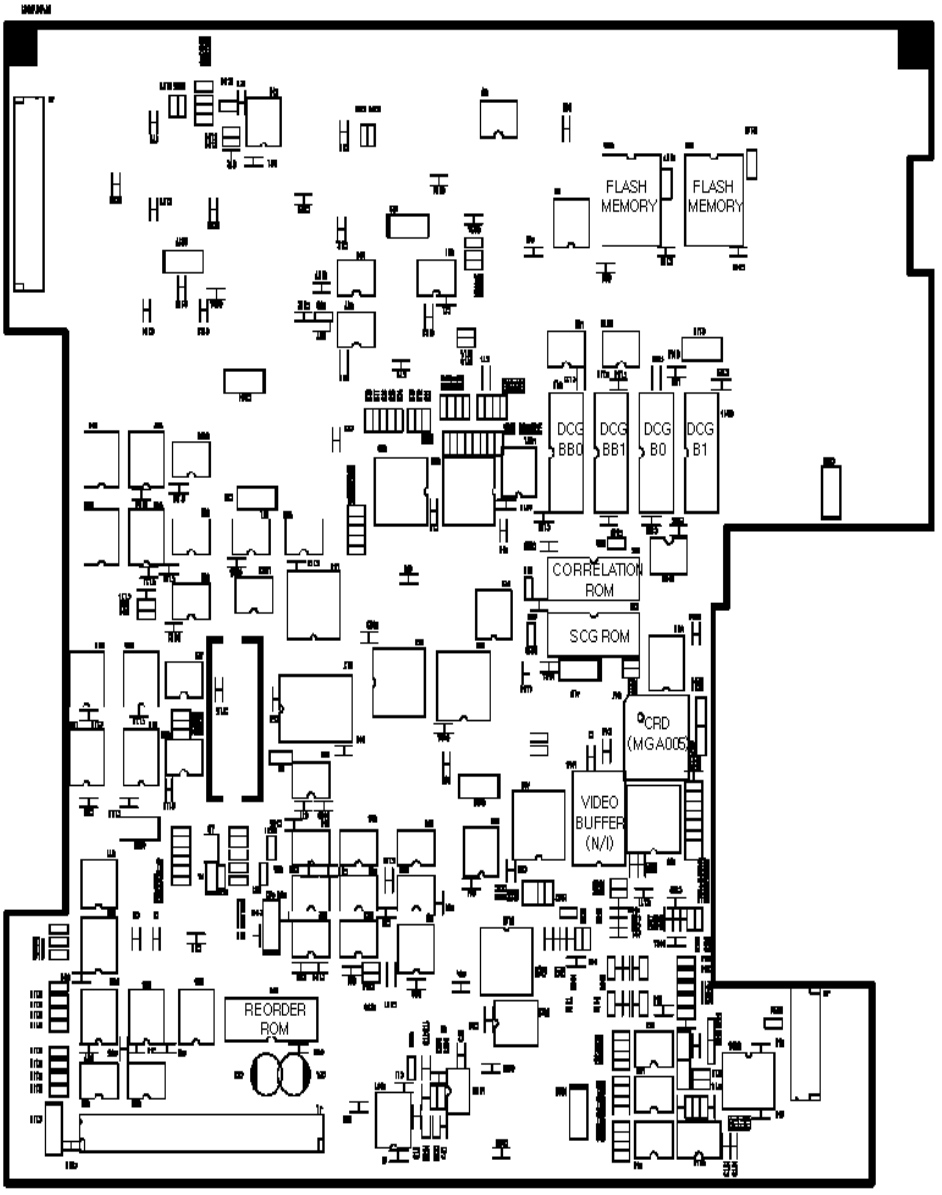
3.5.1 DSC Top Side

mysono201
DSC
FRONT
ARCHITECTURE



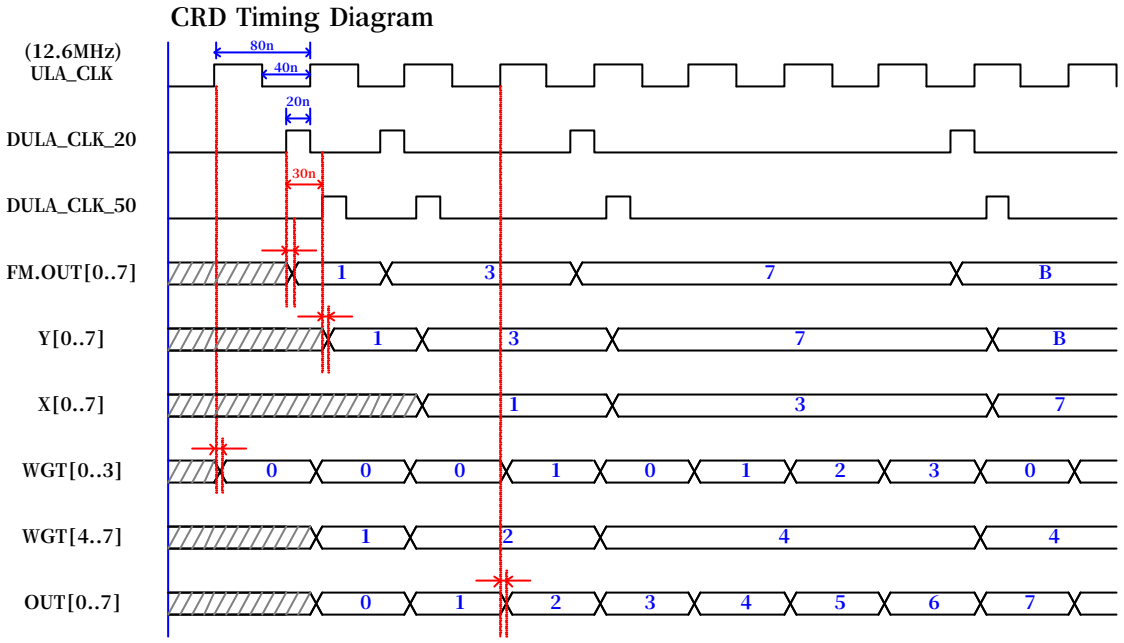
3.5.2 DSC Bottom Side

mysono201
DSC
BOTTOM
ARCHITECTURE



3.6 Timing Chart

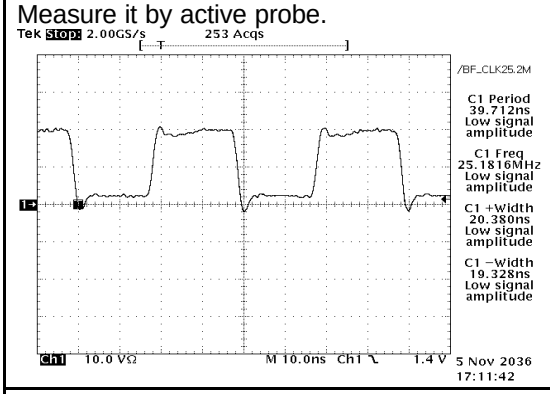
3.6.1 CRD Timing Chart



3.7 Wave Form

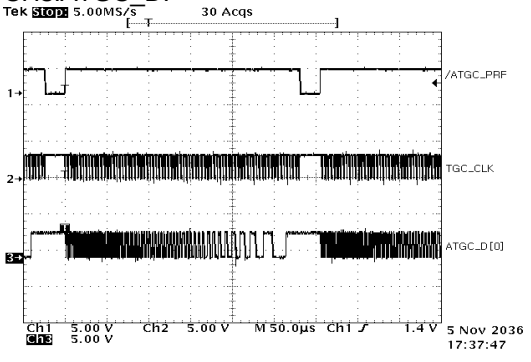
CH1: /BF_CLK25.2M

Measure it by active probe.



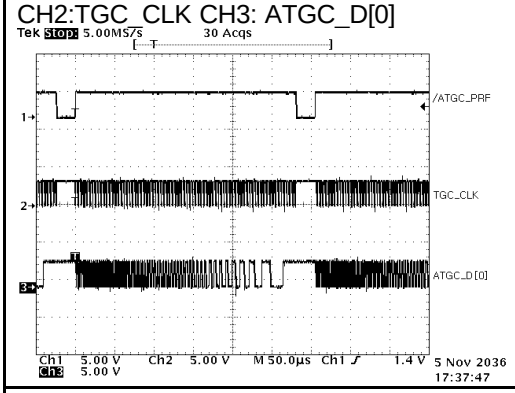
CH1:/ATGC_PRF CH2: GC_CLK

CH3:ATGC_D.



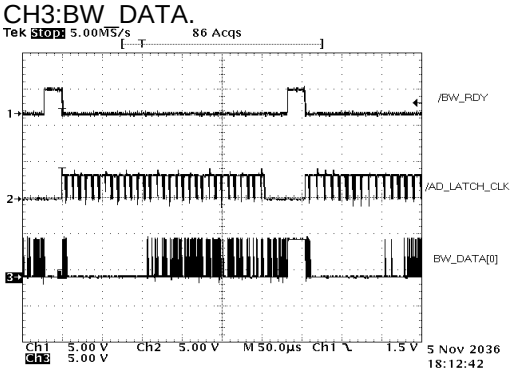
CH1:ATGC_PRF

CH2:TGC_CLK CH3: ATGC_D[0]



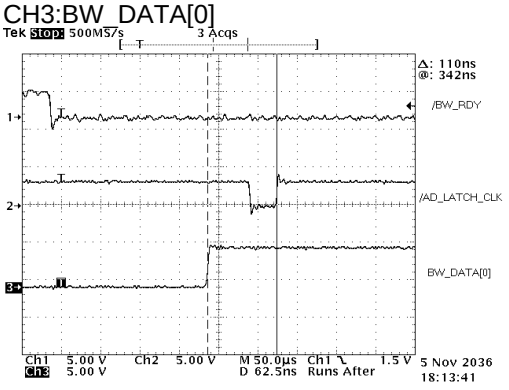
CH1:/BW_RDY CH2:AD_LATCH

CH3:BW_DATA.



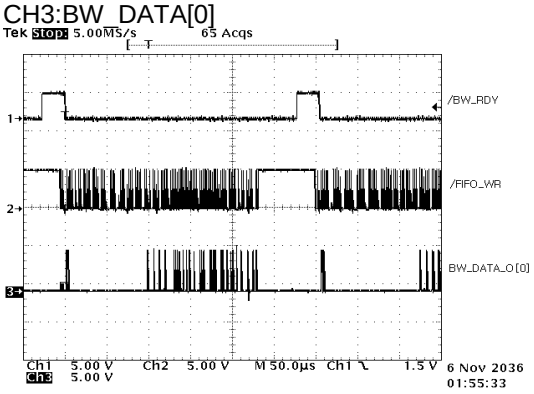
CH1:/BW_RDY CH2:/AD_LATCH_CLK

CH3:BW_DATA[0]



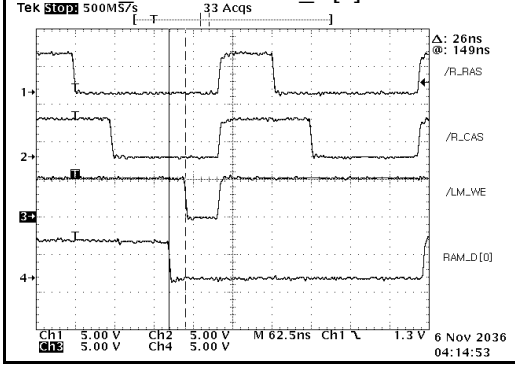
CH1:/BW_RAY CH2:/FIFO_WR

CH3:BW_DATA[0]



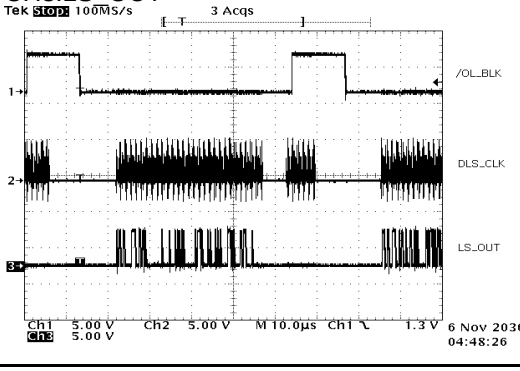
CH1:/R_RAS CH2:R_CAS

CH3:/LM_WE CH4:RAM_D[0]



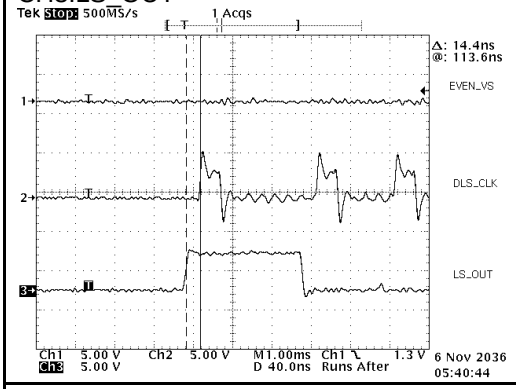
CH1:/CL_BLK CH2:DLS_CLK

CH3:LS_OUT



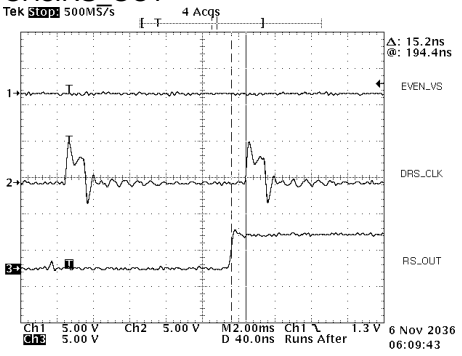
CH1:EVEN_VS CH2:DLS_CLK

CH3:LS_OUT



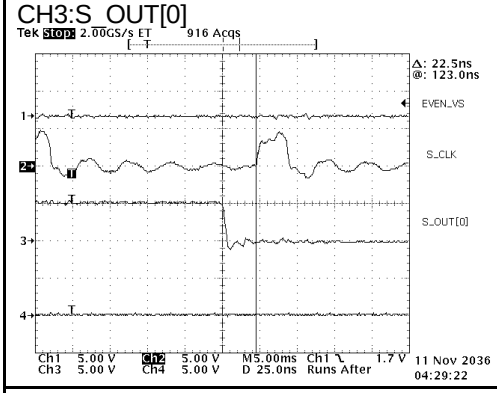
CH1:EVEN_VS CH2:DRS_CLK

CH3:RS_OUT

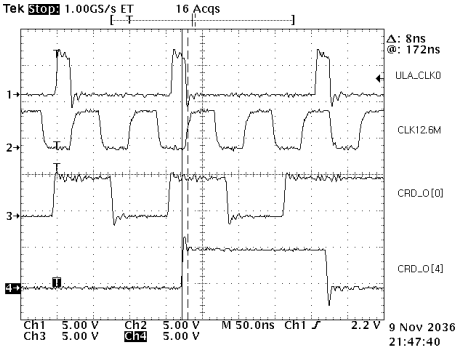


CH1: EVEN_VS CH2:S_CLK

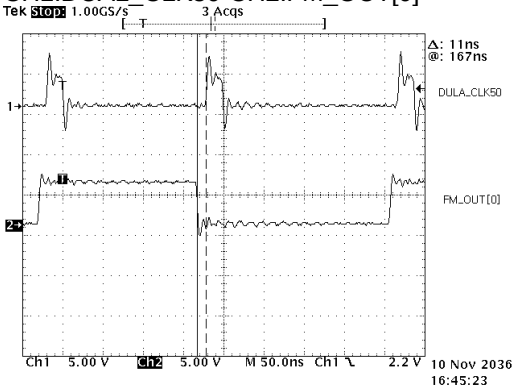
CH3:S_OUT[0]



CH1:

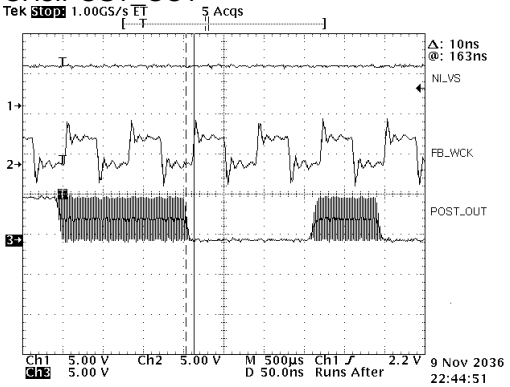


CH1:DUAL_CLK50 CH2:FM_OUT[0]



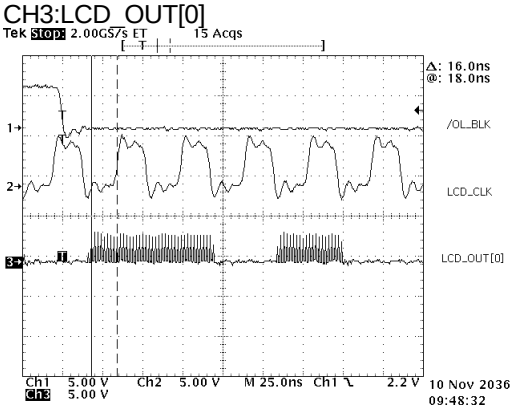
CH1:N_VS CH2FB_WCK

CH3:POST_OUT



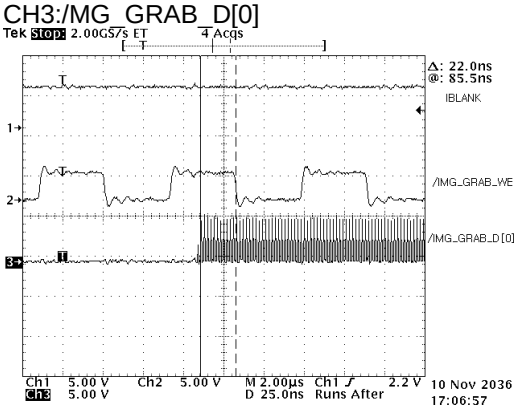
CH1:/CL_BLK CH2: LCD_CLK

CH3:LCD_OUT[0]



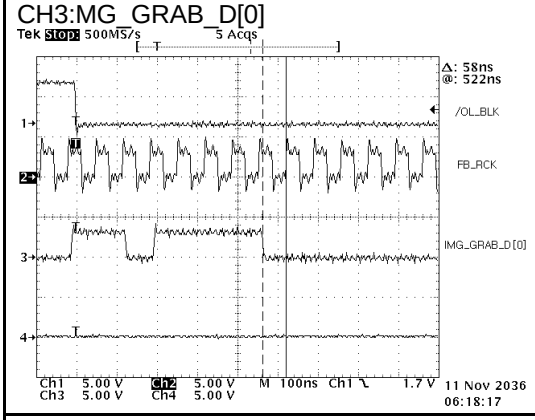
CH1:IBLANK CH2:/IMG_GRAB_WE

CH3:/MG_GRAB_D[0]



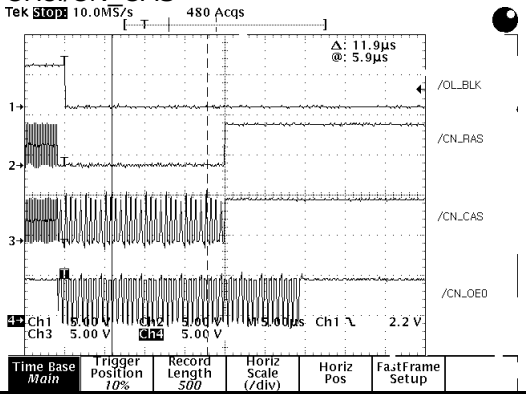
CH1:/OL_BLK CH2:FB_RCK

CH3:MG_GRAB_D[0]



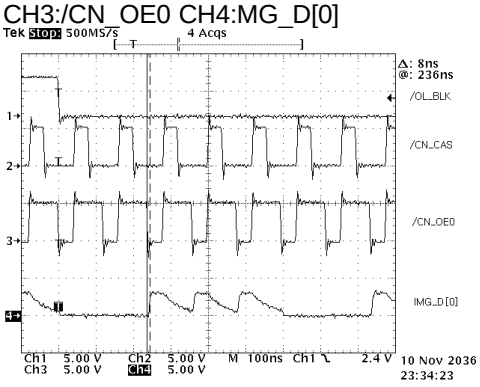
CH1:/OL_BLK CH2:/CN_RAS

CH3:/CN_CAS



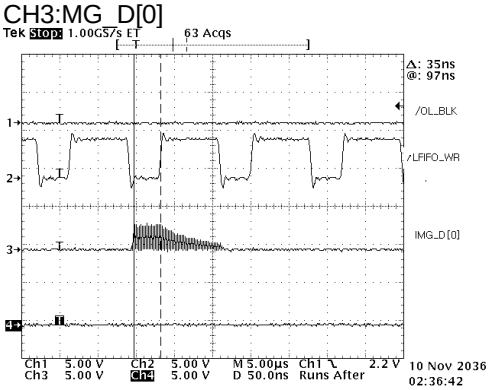
CH1: /OL_BLK CH2: /CN_CAS

CH3:/CN_OE0 CH4:MG_D[0]



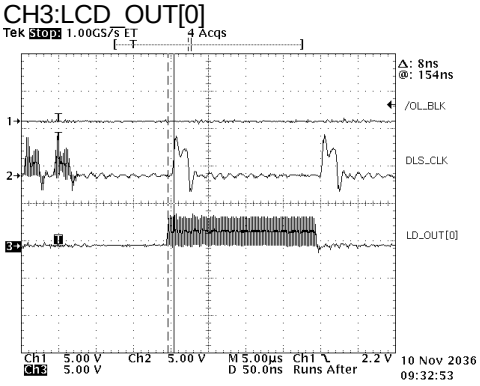
CH1:/OL_BLK CH2:/LFIFO_WR

CH3:MG_D[0]



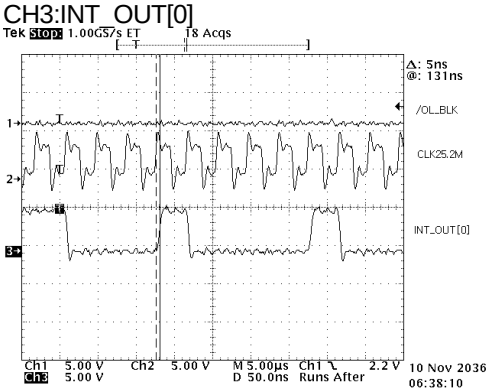
CH1:/OL_BLK CH2:DLS_CLK

CH3:LCD_OUT[0]



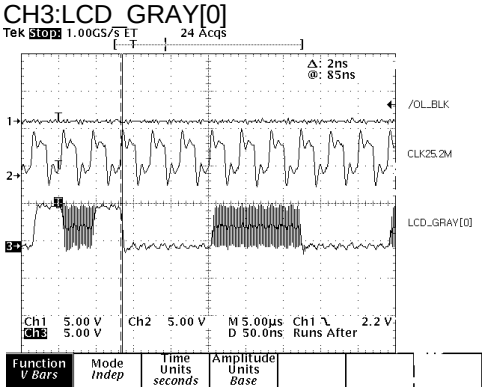
CH1:/OL_BLK CH2:CLK25.2M

CH3:INT_OUT[0]



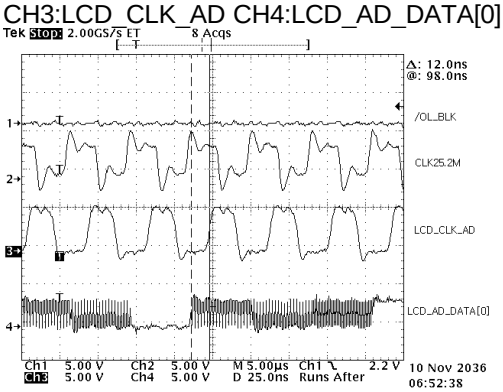
CH1:/OL_BLK CH2:CLK25.2M

CH3:LCD_GRAY[0]

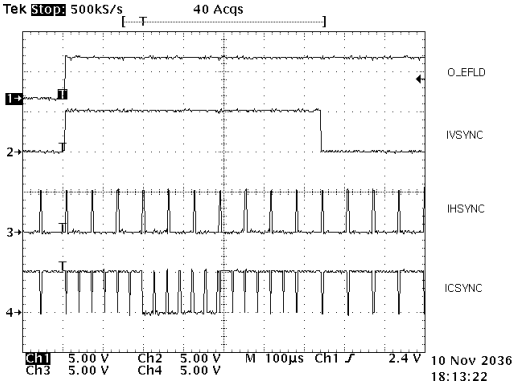


CH1:/OL_BLK CH2:CLK25.2M

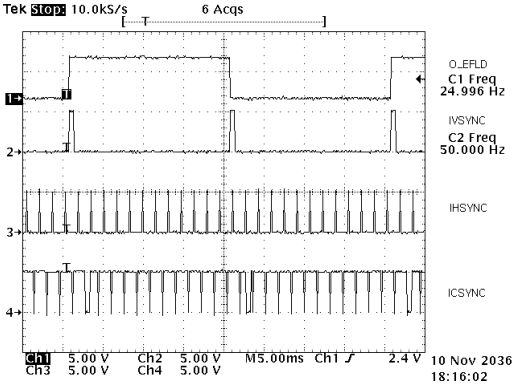
CH3:LCD_CLK_AD CH4:LCD_AD_DATA[0]



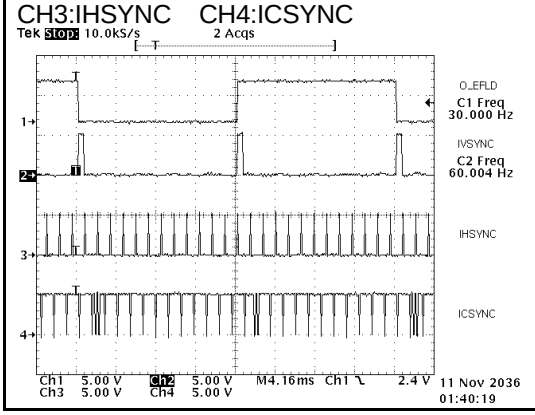
CH1:O_EFLD CH2:IVSYNC
CH3:IHSYNC CH4:ICSYNC



CH1:O_EFLD CH2:IVSYNC
CH3:IHSYNC CH4:ICSYNC



CH1:O_EFLD CH2:IVSYNC
CH3:IHSYNC CH4:ICSYNC



4. Power B/D

4.1 Specification

1) Abstract and application range

2) It is for Power supply device of Mysono201.

3) It supply DC±80V, 12V, ±5V, 3.3V, 6V to each parts of the system by converter DC16V

4) Model name : Mysono201 DC/DC

5) Input voltage - Adaptor : DC16V±1V

- Battery :12.7V ~ 10.5V

[Output voltage and current]

Output Voltage	Before loading					
	Normal	MA			DC16V+Battery	Ripple & Noise
3.3V		2.0	3.35±0.1	3.35±0.1	3.35±0.1	70㎷↓
+ 5VA		1.5	5.0±0.15	5.0±0.15	5.0±0.15	100㎷↓
- 5V		0.5A	- 5.0±0.15	- 5.0±0.15	- 5.0±0.15	100㎷↓
+ 12V		0.6A	12.0±0.3	12.0±0.3	12.0±0.3	200㎷↓
+ 80V		0.01A	80±3	80±3	80±3	500㎷↓
- 80V		0.01A	- 80±3	- 80±3	- 80±3	550㎷↓
6V		0.8A	6.0±0.2	5.8±0.2	6.0±0.2	150㎷↓

Note) * Allowable Ripple Voltage is measured by connecting both 100uF electrolytic capacitor and 0.1uF Ceramic capacitor at the edge of the probe.

* Using Scope is 100MHz Analog Scope.(50mV/0.5msec)

* Ripple Voltage = Measured value – Input Ripple Voltage

6) Alarm for Battery voltage discharge : 10.1±0.2V

7) Cutoff Voltage for Battery discharge : 9.2±0.2V

8) Battery charge Voltage : 12.45~12.75V

9) Cooling Type : Natural air cooling and forced circulation

10) Safety Standard : meet IEC60601-1.

11) Efficiency : Over 75 % (Input 16V , MAX load)

12) Using Environment

(1) Temperature range : 0℃ ~40℃

(2) Humidity range : 10% ~90%RH

13) Keeping Environment

(1) Temperature range : -15℃ ~70℃

(2) Humidity range : 10% ~95%RH

14) The others

	5V	3.3V	-5V	6V	12V	80V	–80V
OCP range	4A~6A	4A~6A	Protect Short	Protect Short	Protect Short	Protect Short	Protect Short
Setup/Off Time	Within 100㎳	Within 50㎳	Within 100㎳	Within 100㎳	Within 100㎳	Within 1.5sec	Within 1.5sec
Rising/Falling Time	Within 30㎳	Within 30㎳	Within 100㎳	Within 100㎳	Within 100㎳	Within 1sec	Within 1sec

15) Battery

(1) Maker : Saehan Industries Inc.

(2) Model name : SH-202A

16) LED Operation

(1) When Battery discharge : RED

(2) When Battery charge : Orange

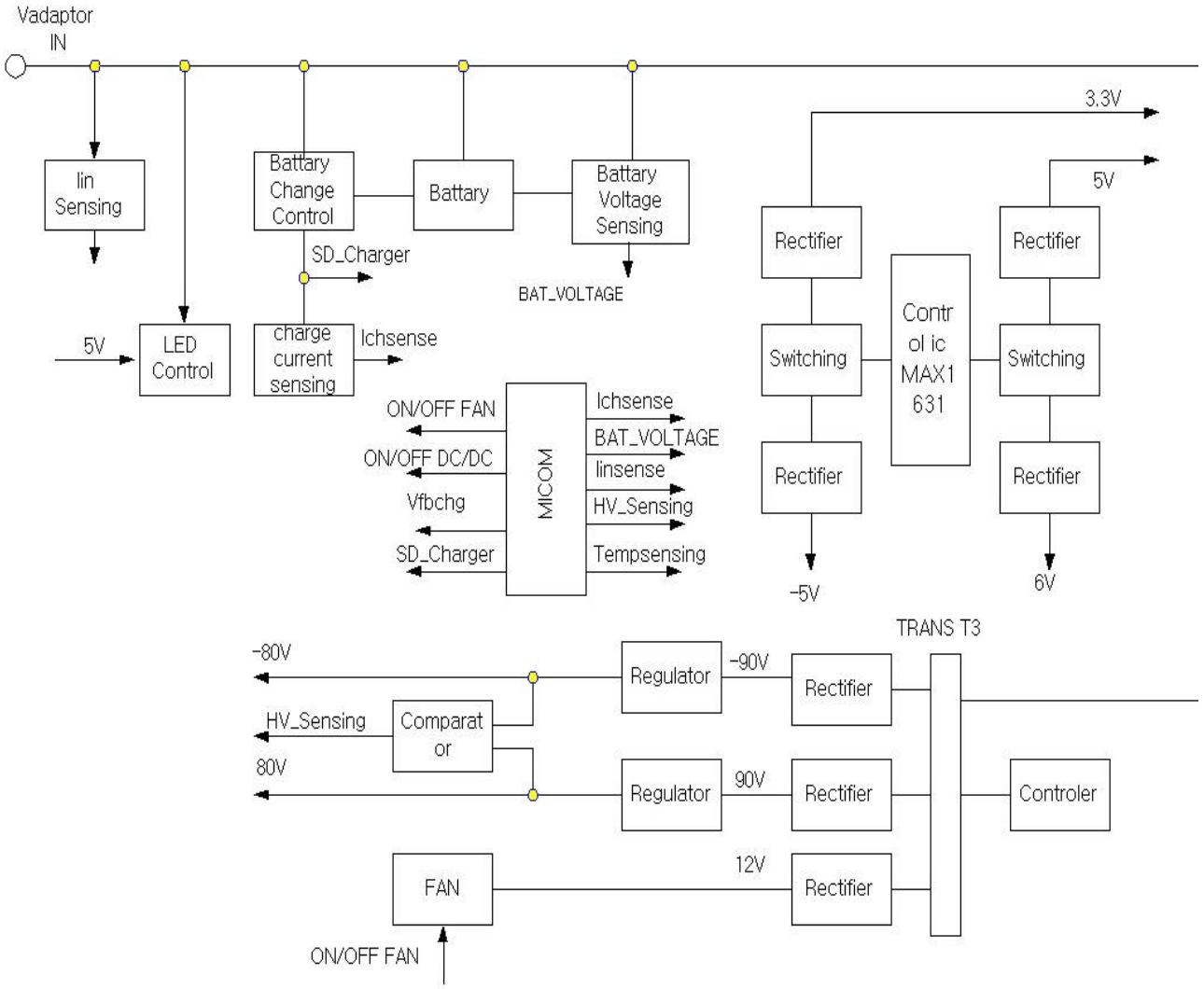
(3) When Battery charge finish : Yellow

(4) Using Adaptor (NO Battery) :No Color

17) Supply or Cutoff the power

Using Toggle function of Tack S/W (SW1)

4.2 Block Diagram



4.3 Detail Description

- Lin Sensing : supervise total current flow into DC/DC Power Board.
  Battery Charge Control : The circuit for Battery charge
  It stops to work by using SD-Charger or Vfbchg when Battery is discharged
- Charge Current Sensing : Control the charging current flow into Battery Maximum charging current is limited 3A. When charging current flow under 300mA, charger stops to charge because of recognizing as full charge. Charging current Sensing amplify the voltage measured both end of R5 and then generate that voltage level at U-Com.
- Battery Voltage Sensing : Check Battery voltage.

When insert Battery to the system, recognize the condition whether Battery need to charge or not.

When recognized Battery voltage is under 12V, start to charge until the voltage value reach to 12.6V.

But after reaching 12.6V, it check Charge Current Sensing and then continuously charge Battery until the Charging current reach to about 300mA.

- Control IC Max 1631 : DC/DV Control IC for output 3.3V, 5V by using BUCK S/W type.
  IC works when high voltage input into Pin 23(ON/OFF DC/DC) of IC and starts to switching.

By rectifying each value, it gains output as 3.3V, 5V. The constant voltage such as 3.3V, 5V drive the output voltage and then pass a feedback signal to FB3 (3Pin) and FB5 (12Pin). Also –5V and 6V are proportioned each coil rate and print out by winding.

- 80V,-80V,12V Output : This value can be gained by Flyback circuit consist of U13(KA3843), Q17, and circumstance control circuit. At this time, the basic voltage is 12V and its value is output as ±87V proportioned to rate of coil. And also ±80V is output through the constant voltage circuit when the output is ±87V.
- Comparator : Its reference value is about 2.6V under the standard setting output is ± 80V.
  If the standard setting output reduce below 60V at any side of ±80V, the reference value could be down. And the down voltage can sensing by U-Com and finally cutoff ±80V by HV_SHDN on it.
- Color display of LED
  1) Using only Adaptor : No Color.
  2) Under Charging : Orange.
  3) Under Discharging : Red.
  4) Finishing the recharge: Yellow
- Working description of U-Com :
  1) ON/ OFF (5Pin): Input terminal to control a hole Power Board by Toggle S/W
  2) PWM (6Pin) : Control the Battery charging current by On/Off Duty
  3) ON/ OFF FAN (8Pin) : Fan work by recognizing “H” signal from the output of 14Pin

when a temperature around LM35 increase over the standard temperature.

4) SD_Charger (10Pin) : When the charging circuit dose not work, control LED and shutdown it by moving 1PIN of U3 to Low.
5) BAT_WARNING (11Pin) : Warning display when the Battery Voltage decrease below 9.2±0.2V.
6) HV_SHDN (12Pin) : It could be off when the output voltage of ±80V is wrong.
7) Temp_Sensing (14Pin) : Fan work by recognizing 0.1mV/1℃ when a temperature around LM35 increase over the standard temperature.
8) HV_Sensing (15Pin) : Checking the output of ±80V whether its value is good or not.
9) Iin_Sensing (16Pin) : Checking and Limiting the inflow current from outside.
10) BAT_Voltage (17Pin) : Checking and Limiting the charging voltage of Battery
11) Ich_Sense (16Pin) : Checking and Limiting the charging current of Battery
12) Vad_EN : Check IN/OUT of adapter.

- Battery Alarm sound: When the battery voltage drops to 10.2V, Alarm sounds each 10sec to notice about it.
- Battery Cutoff Voltage: When Battery voltage drops to 9.2V, the system cut off it. As the result, the battery voltage increases to about 10V.

5.Probe

5.1.General Description

The probe element is the same as a standard probe of SA600, Sa9900 with 96 elements.

When apply the probe with 128 elements to the system, only use 96 elements among them.

There is 16 channel type and embody 1x6 Mux switch with HV20220 as main device.

Probe box consists of PB_Main board , PB_Odd board and PB_Even board to separate the element as odd or even.

5.2. Detail description

Probe ID connects to the system with Pull up resistance at 3.3V. To make ID bit Low, short between ID bit and Ground. The signal that probe connect with the system is pull up in system inside and the Probe insert signal is set as ground at probe. Thus when /PRB_INS is low, High Voltage also turn 0V into +/- 80 V and it is possible to firing. 5V TTL drive HVSW HV20220 Control signal. The signal is buffering at PB_main board and divides PB_Odd and PB_Even. Some of ultrasound signals, Echo 0,2,4,..,14, connect to PB_Odd, and some of them, Echo 1,3,5,..,15, connect to PB_Even.

5.3 Probe Connector Pin Define

Using ITT Cannon 60 Pin Male Connector its array is 6x10 matrix.

The bottom of left under take a view of Female connector connected the system is 1A pin.

The define of each pin is as bellows;

	1	2	3	4	5	6
A	ECHO 0	GND	ECHO 1	GND	ECHO 2	GND
B	GND	ECHO 3	GND	ECHO 4	GND	ECHO 5
C	ECHO 6	GND	ECHO 7	GND	ECHO 8	GND
D	GND	ECHO 9	GND	ECHO 10	GND	ECHO 11
E	ECHO 12	GND	ECHO 13	GND	ECHO 14	ECHO 15
F	N.C.	N.C.	GND	+ 80 V	+ 80 V	GND
G	GND	- 80 V	- 80 V	GND	+ 5 V	GND
H	/DAT0 0	/DATA 1	GND	/DATA 2	/DATA 3	GND
J	Remote	HVSW_CLK	/HVSW_LE	N.C.	N.C.	PRB_ID 0
K	PRB_ID 1	PRB_ID 2	GND	PRB_ID 3	PRB_ID 4	/PRB_INS

5.4 Signal Definition

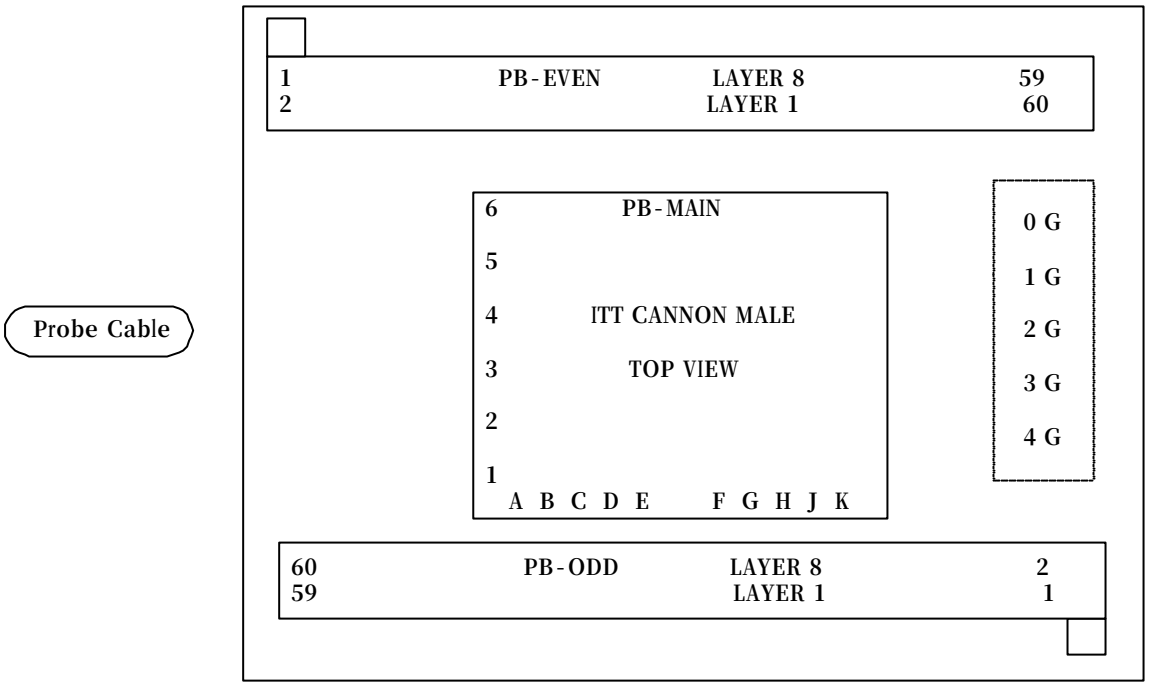
Name	I/O	Description
Echo [0-15]	I/O	Pulser Output & Echo Signal
TEMP_DXP	O	Not use even it define as temperature Sensor. (Pin 1F)
TEMP_DXN	O	Not use even it define as temperature Sensor. (Pin 2F)
+ 80V	I	High voltage power
- 80V	I	High voltage power
+ 5V	I	TTL power
/DATA[0-3]	I	HVSW Control Data Buffer the data from PB_main board to Not Gate
HVSW_CLK	I	3.15MHZ Clock 24 ea
/HVSW_LE	I	Latch the data in HVSW inside by changed to Low when input the last 24^{th} data
Remote	O	The switch on the probe is using for toggle. Using for Freeze : Press it short Using for Store : Press it long (about 3 seconds)
PRB_ID[0-4]	O	Probe Identity Number Default: High (To change Low, short it with Ground terminal) To distinguish probe type, use PRB_ID 4' - Convex : Low - Linear : High
/PRB_INS	O	Ground It is pull up as follows to check whether the probe connect with system or not. Default in system, Ground in PB_main board

5.5 Probe ID

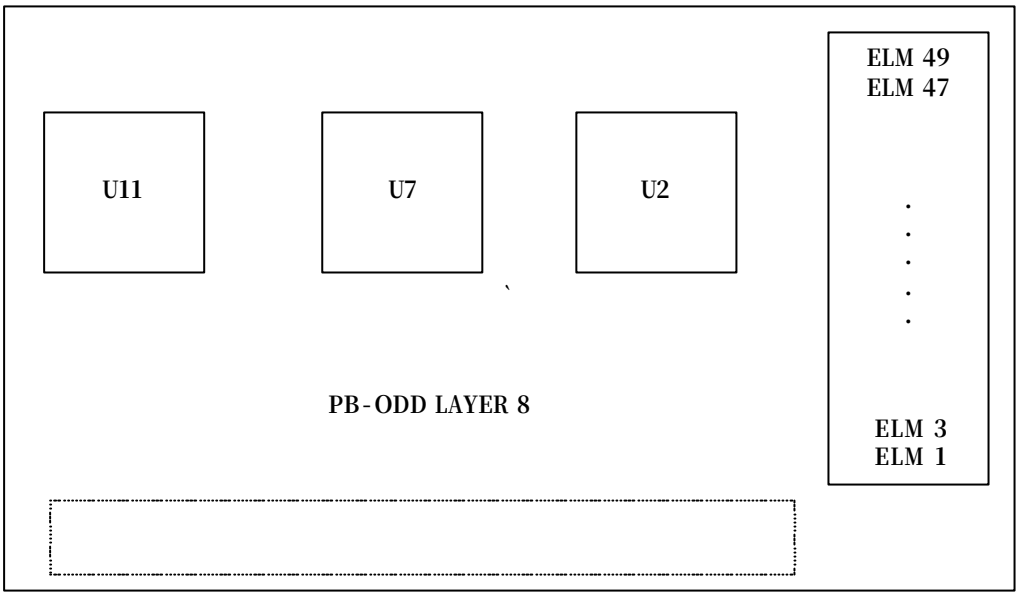
ID	Bit 4 3 2 1 0 ○ : Open ● : Short	Probe Name	BF Delay data	BF Rom	Mid Rom	Triple Rom
0x10	○ ● ● ● ●	L2-5/120CD	0xFF9B	K16	K17	K18
0x11	○ ● ● ● ○	L2-5/150CD	0xFF9B	K19	K20	K21
0x12	○ ● ● ○ ●	L4-7CD	0xFF9B	K22	K23	K24
0x13	○ ● ● ○ ○	L5-9CD	0xFF9B	K25	K26	K27
0x14	○ ● ○ ● ●	L5-9/60CD	0xFF9B	K28	K29	K30
0x15	○ ● ○ ● ○	L2-5/170CD	0xFF9B	K31	K32	K33
0x16	○ ● ○ ○ ●	LV4-7AD	0xFF9B	K34	K35	K36
0x17	○ ● ○ ○ ○	LV5-9AD	0xFF9B	K37	K38	K39
0x00	● ● ● ● ●	C2-5/60BD	0xFFE0	K40	K41	K42
0x01	● ● ● ● ○	Reserved	0xFFE0	K43	K44	K45
0x02	● ● ● ○ ●	C4-9/10ED	0xFFD0	K46	K47	K48
0x03	● ● ● ○ ○	C4-7BD	0xFFD0	K49	K50	K51
0x04	● ● ○ ● ●	C4-9/13CD	0xFFD0	K52	K53	K54
0x05	● ● ○ ● ○	C5-8BD	0xFFE0	K55	K56	K57
0x06	● ● ○ ○ ●	Reserved		K58	K59	K60
0x07	● ● ○ ○ ○	Not supported				

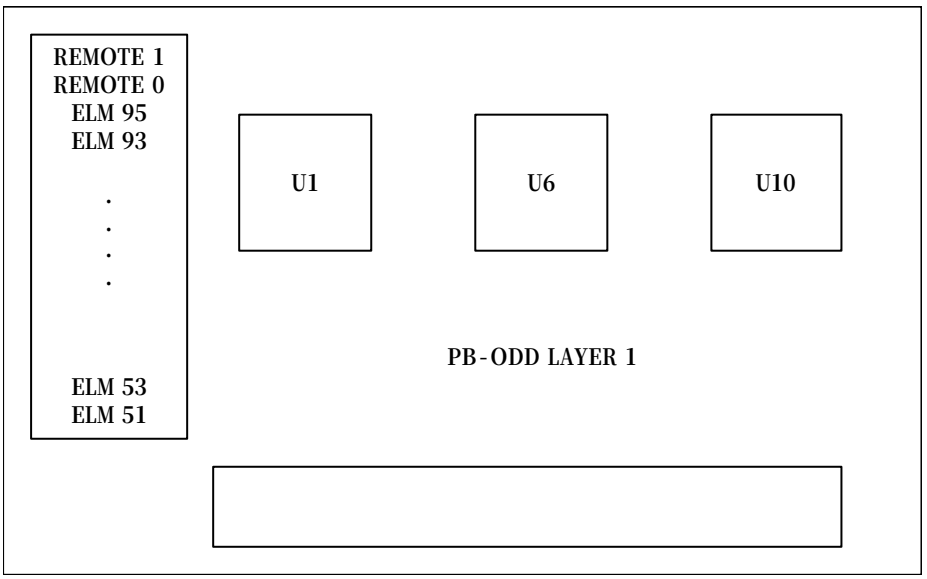
5.6 PCB Lay Out

5.6.1 PB Main Top Side

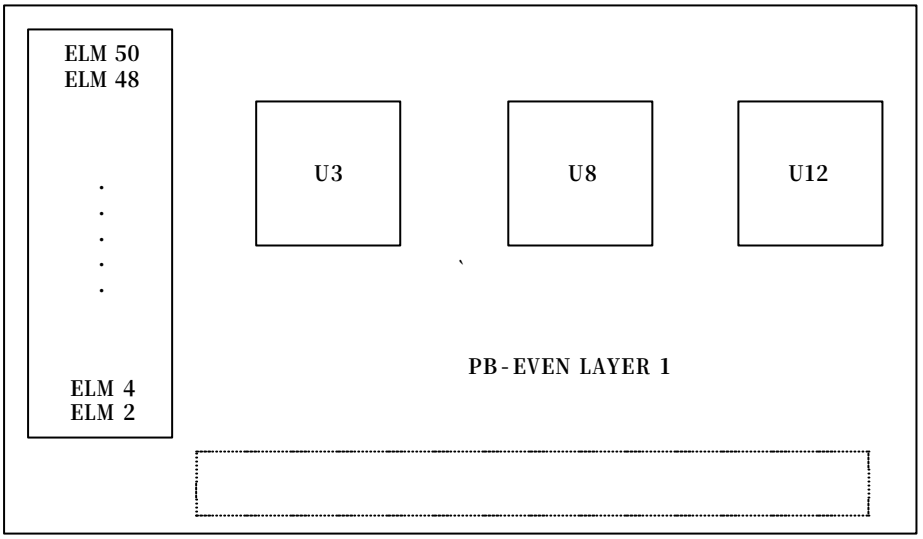


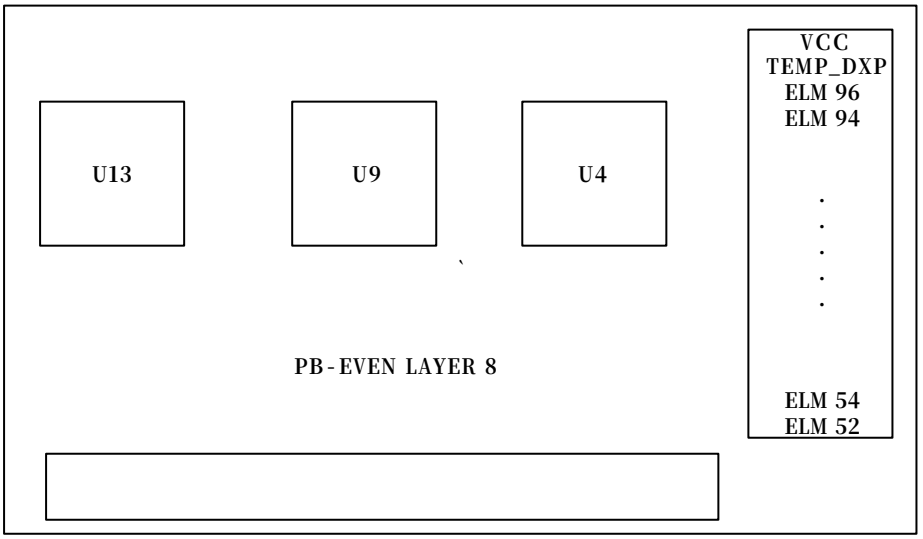
5.6.2 PB_ODD Top/Bottom Size





5.6.3 PB_EVEN Top/Bottom Size





6. ASIC Data Sheet

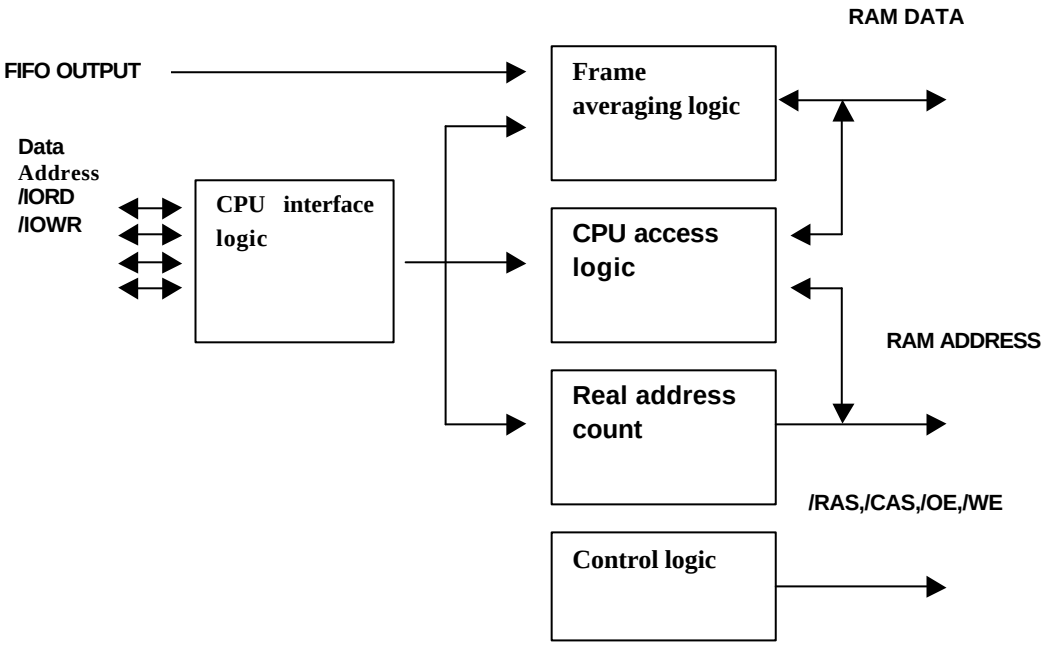
6.1 MAGA0010A Manual: Frame Memory Controller

6.1.1 Description

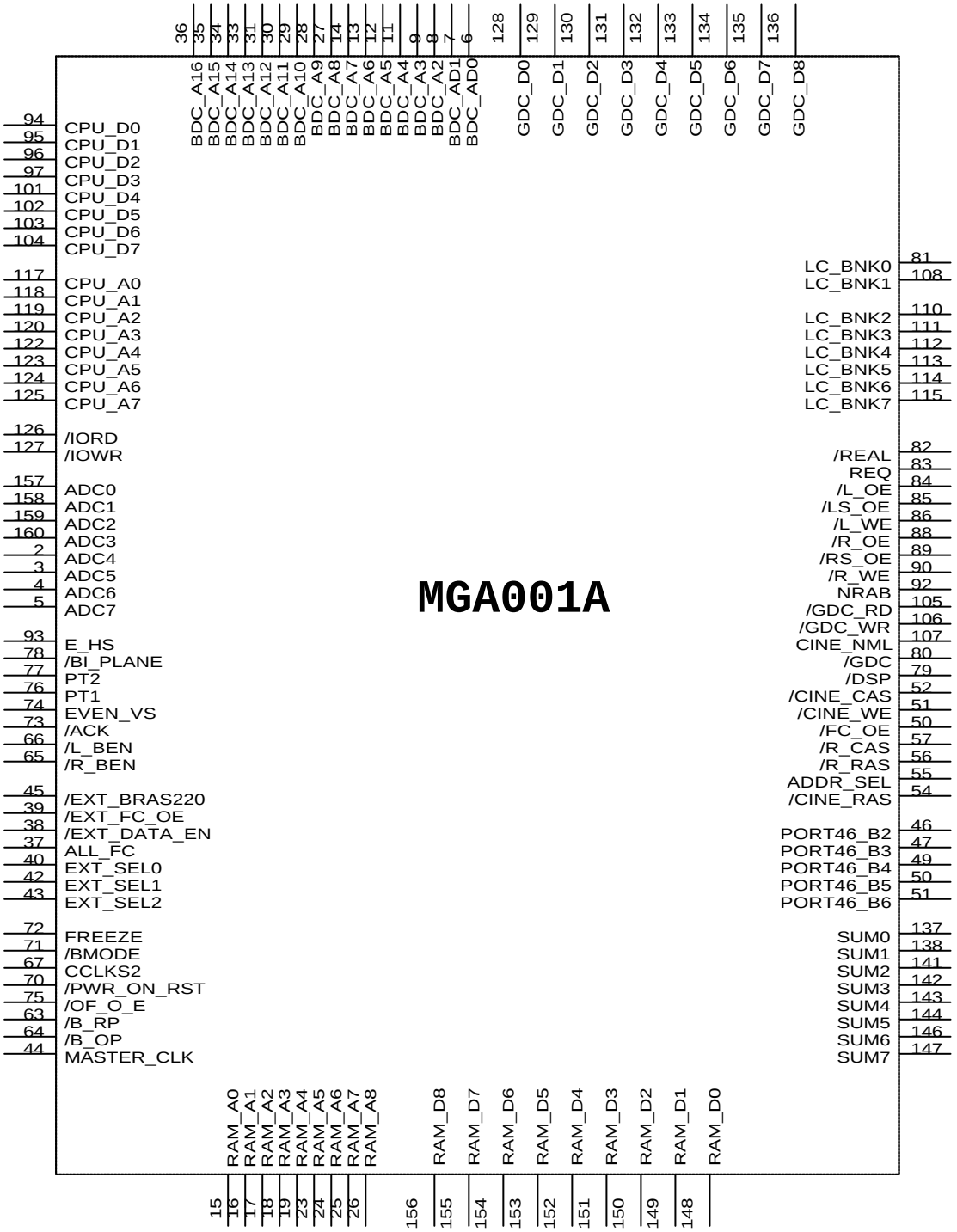
MGA001A is ASIC for FMC use only and design to make a various signal under ASIC Technology.

The signal related with Frame memory is Data and Address bus, Control signal such as /RAS ,/CAS, /OE, /WE, etc.

Total Frame Average Factor is 6ea since Data Bus in Frame memory connect with Frame Average Logic at chip inside. Mysonon201 use only 4ea among them.



6.1.3 Pin Diagram



6.2 MAGA003A Manual :Clocks Generators

MGA003A: Gate Array designed by ASIC technology

About 7500 gates

208 pin QFP package

6.2.1 Description

MGA 003A is composed of 5 different parts such as Sampling Clock Generator (SCG), Display Clock Generator (DCG) , Gray Bar Display (GBG) , Constant Rate Display (CRD) control logic , and address decoding logic.

6.2.2 Main Features

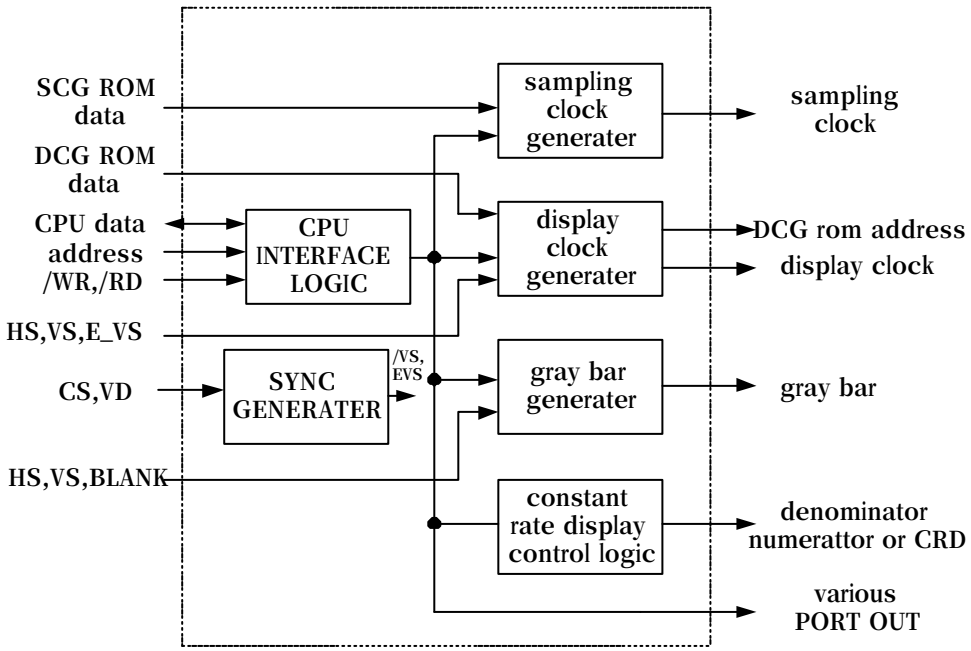
- SCG (Sampling Clock Generator) : Basically sampling clock is generated from ROM data containing LOOK-UP table which is the clock – map .

These data are composed BASE - value , CORRECTION – value , and BLANK – value .

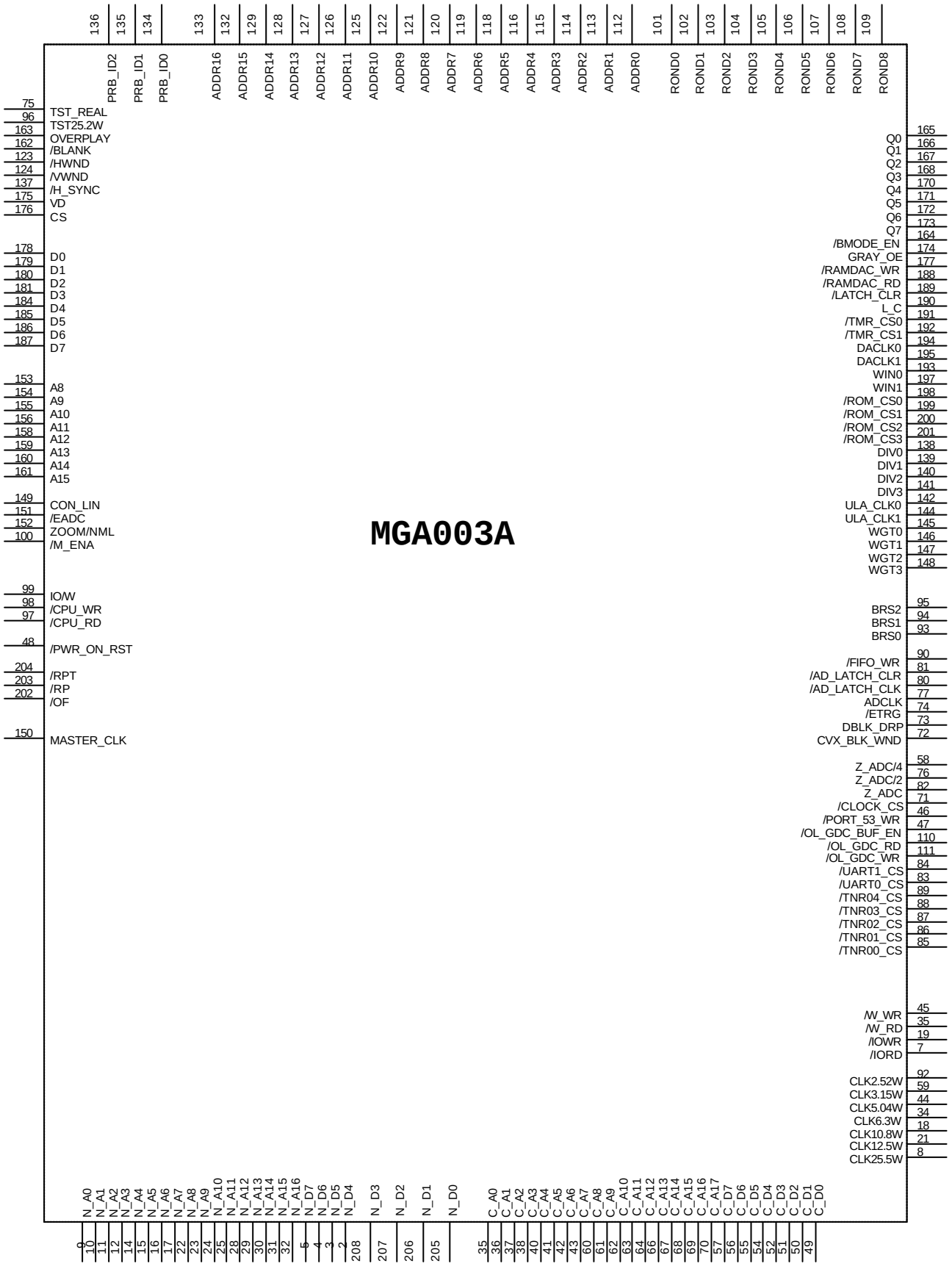
The correction data has AD clock pattern (map) and 2048 deferent clocks can be made.

- DCG (Display Clock Generator) : Display clock is generated by using the ROM's data of display clock having this bit pattern. Mysono201 support 8 different display clock for each liner and convex probe.
- GBU (Gray Bar Generator) : To make gray bar and overlay shadow by using hardware.
- Adrress decoding logic : The many kinds of I/O ports used in DSC are decoded in this logic.
- CRD (Constant Rate Display) : Supply Read Clock of Frame Memory

6.2.3 Block Diagram



6.2.4 Pin Diagram

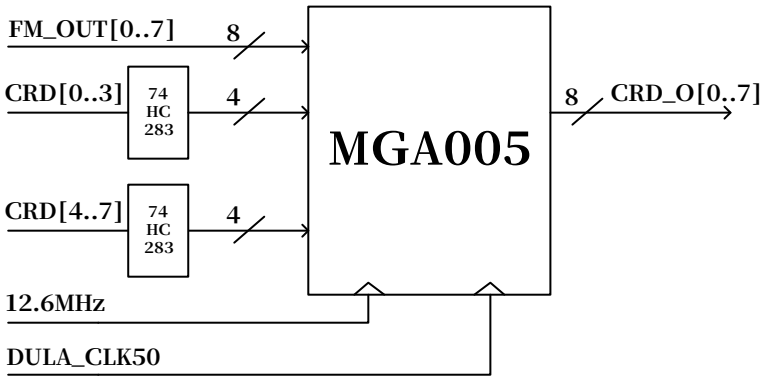


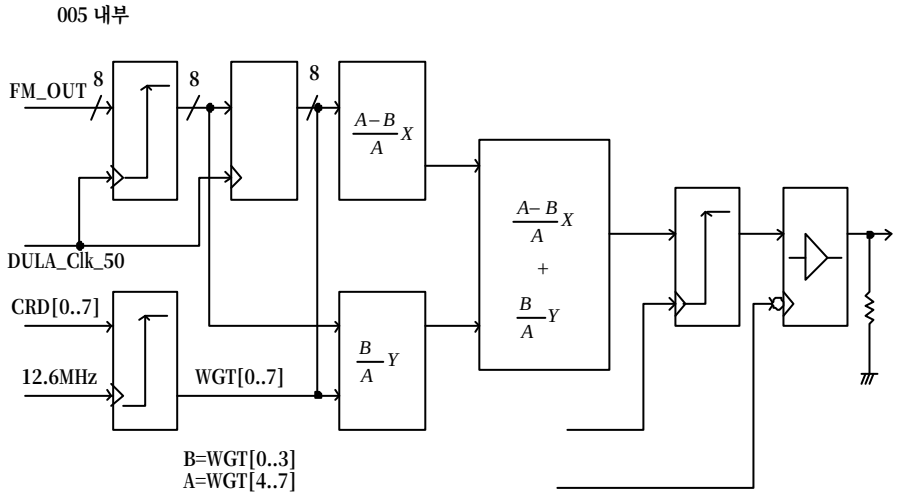
6.3 MAGA005 Manual

6.3.1 Description

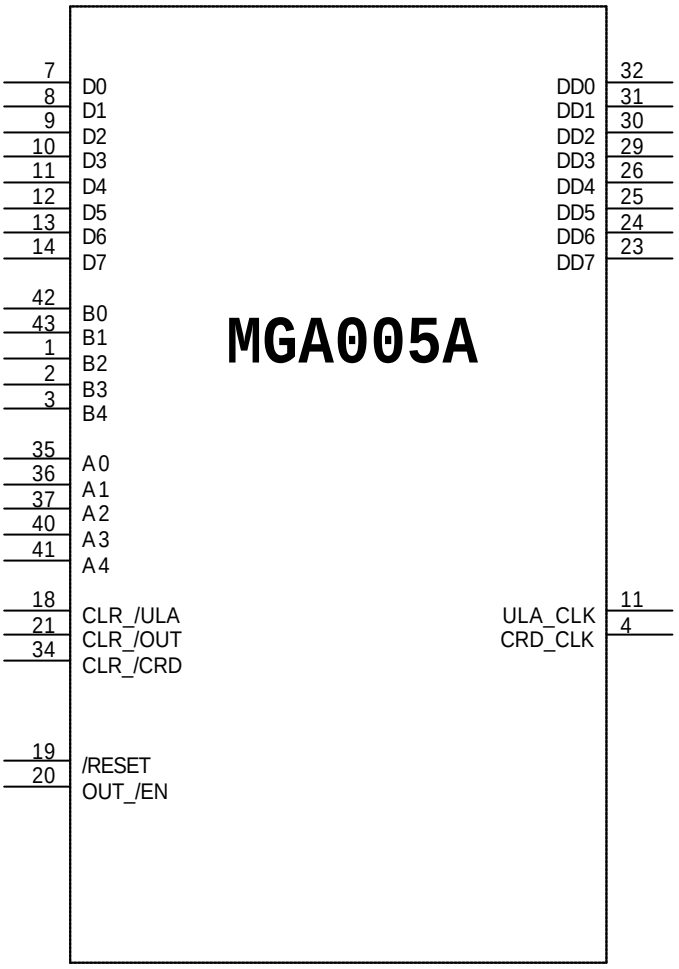
- To display the ultrasound image of the Convex probe on the monitor, system recognize and read the data of Frame memory by Display clock that generated on DCG (Display Clock Generator).
- One scanline will be interpolated to the Horizontal Sync (HSYNC) as fixed Scanline number from the system and the frequency of interpolation DCG Clock will be changed whenever the HSYNC is generated according to the Vertical Sync (VSYNC). The image from Far-Field is interpolated as low frequency DCG Clock and there is a possibility of mosaic problem on actual display.
- The CDR Logic uniformly converts the frequency of signal as 12.6 MHz that input to the Monitor by 1D interpolation to horizontal axis for the data that is interpolated from the Frame Memory as Monitor Dot Clock 12.6 MHz.

6.3.2 Block Diagram





6.3.3 Pin Diagram

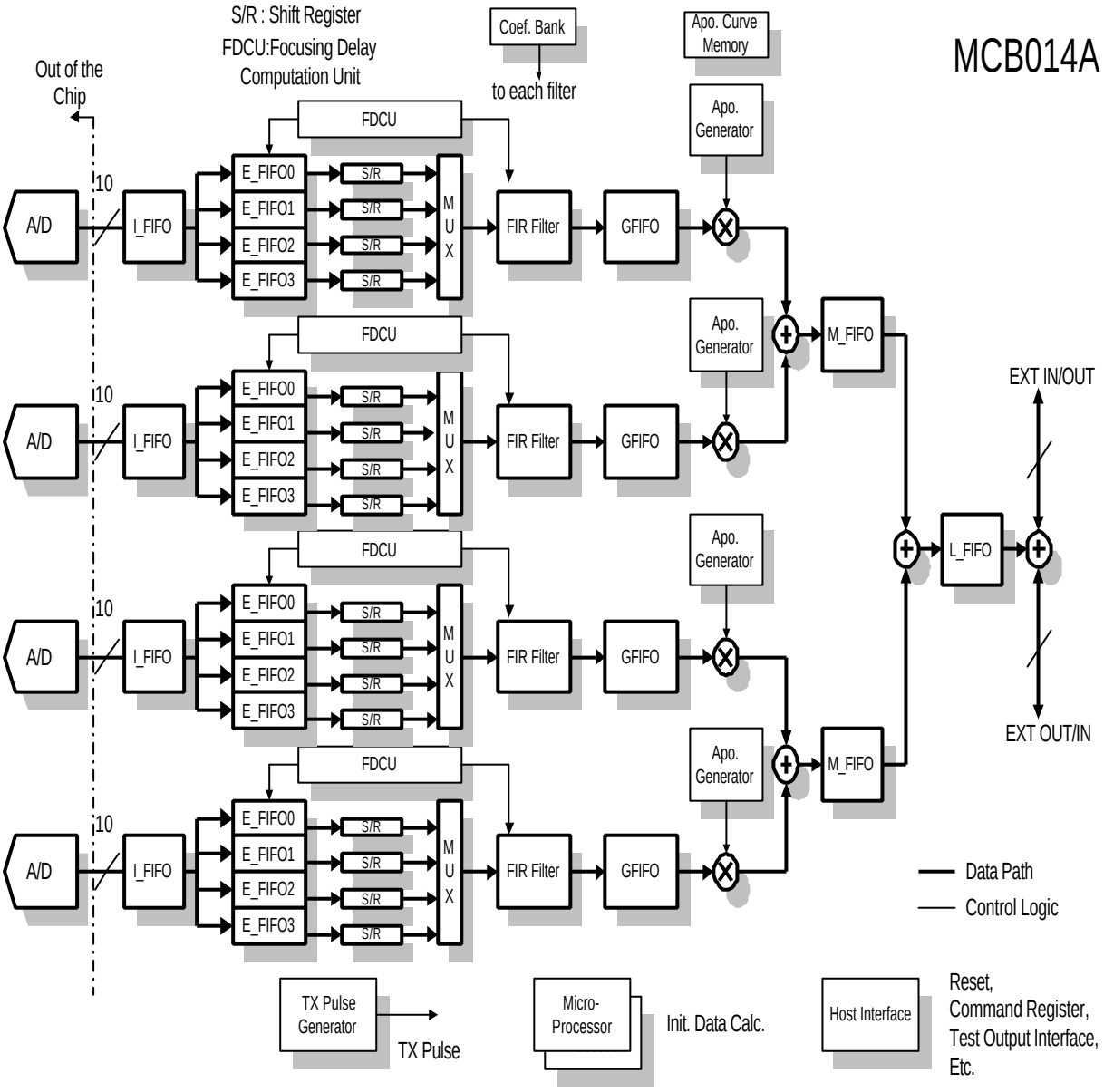


6.4 MCB014 Manual

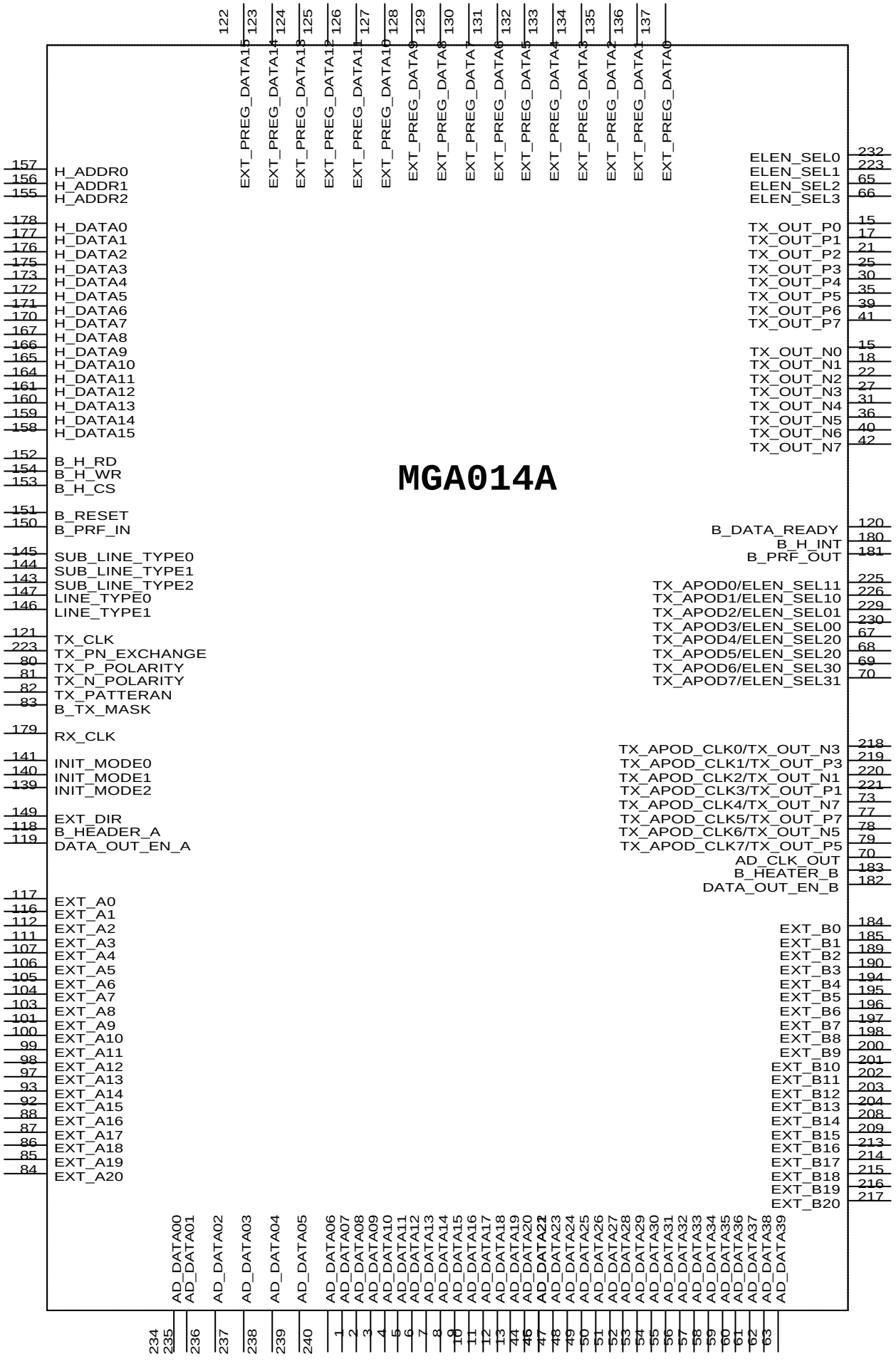
6.4.1 Main Features

- 4 Channel RX & 8 channel TX in one chip
- Up to 4 parallel beam receiving in each RX channel
- Full TX function including TX apodization, Coded exitation
- Throughput up to 62 MSPS
- Extended accuracy focusing delay: RX: Up to±3ns, TX: Up to ±4ns
- Internal small micro-processor for internal initialization data computing
- Reduced initialization data sets for external initialization
- Initialization data loading (or computing) while running
- Powerful board debugging functions
- +3.3V Power Supply

6.4.2 Block Diagram



6.4.3 Pin Diagram

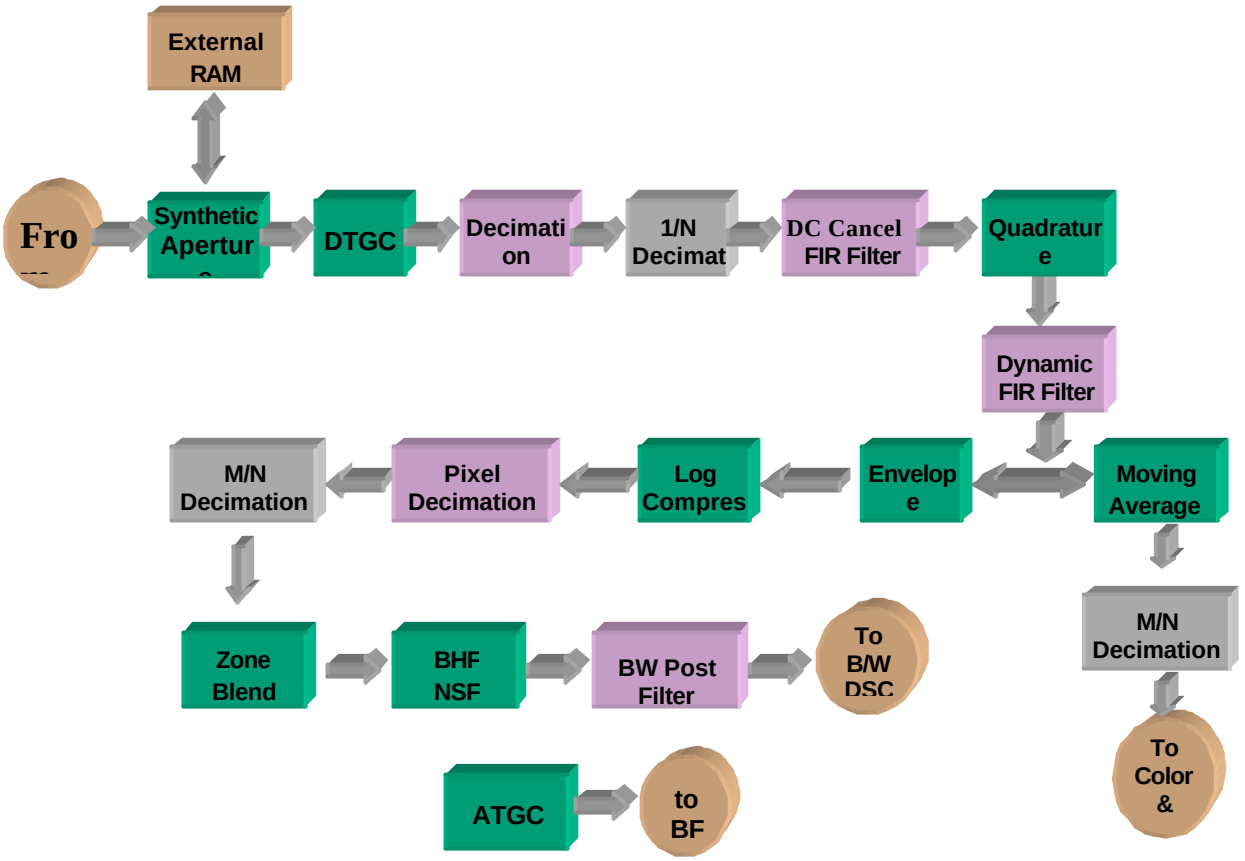


6.5 MGA015A Manual

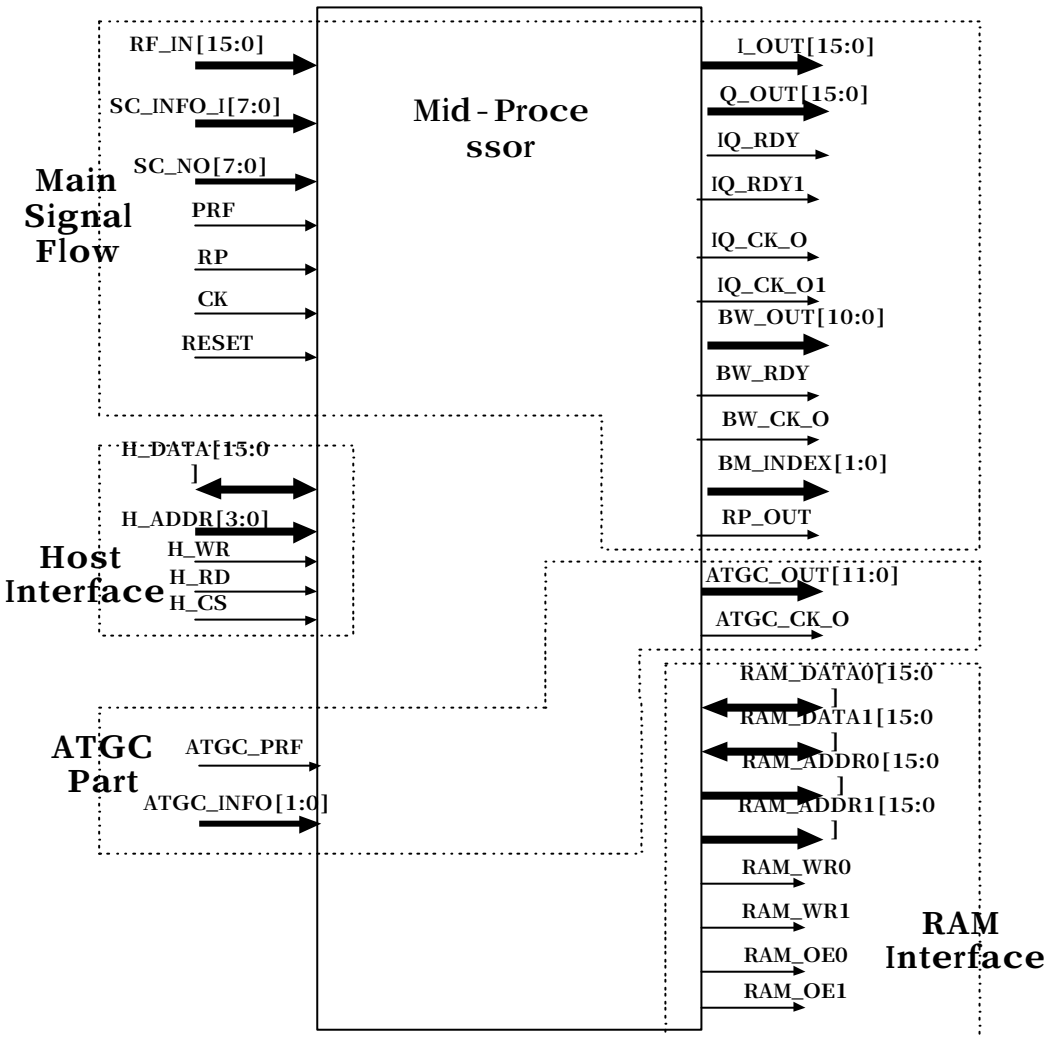
6.5.1 Main Features

- Synthetic Aperture summing and Multi-beam demultiplexing (external RAM needed)
- Digital TGC, SGC (scan-line gain compensation)
- RF Decimation Filter and Decimation
- DC Cancelling Filter
- Mixer with variable frequency NCO(Numerically Controlled Oscillator)
- Dynamic FIR Filter
- Moving Averager
- N/M nearest decimation for I/Q
- Envelope Detector using Square-Root and Square
- Log Compression
- Decimation Filter for B/W and N/M nearest decimation for B/W
- Zone Blend
- Non-linear Black-Hole Filling & Noise Suppression Filter for B/W
- Anti-Aliasing and/or Edge Enhence filter for B/W
- Analog TGC (including analog SGC) data for Beamformer

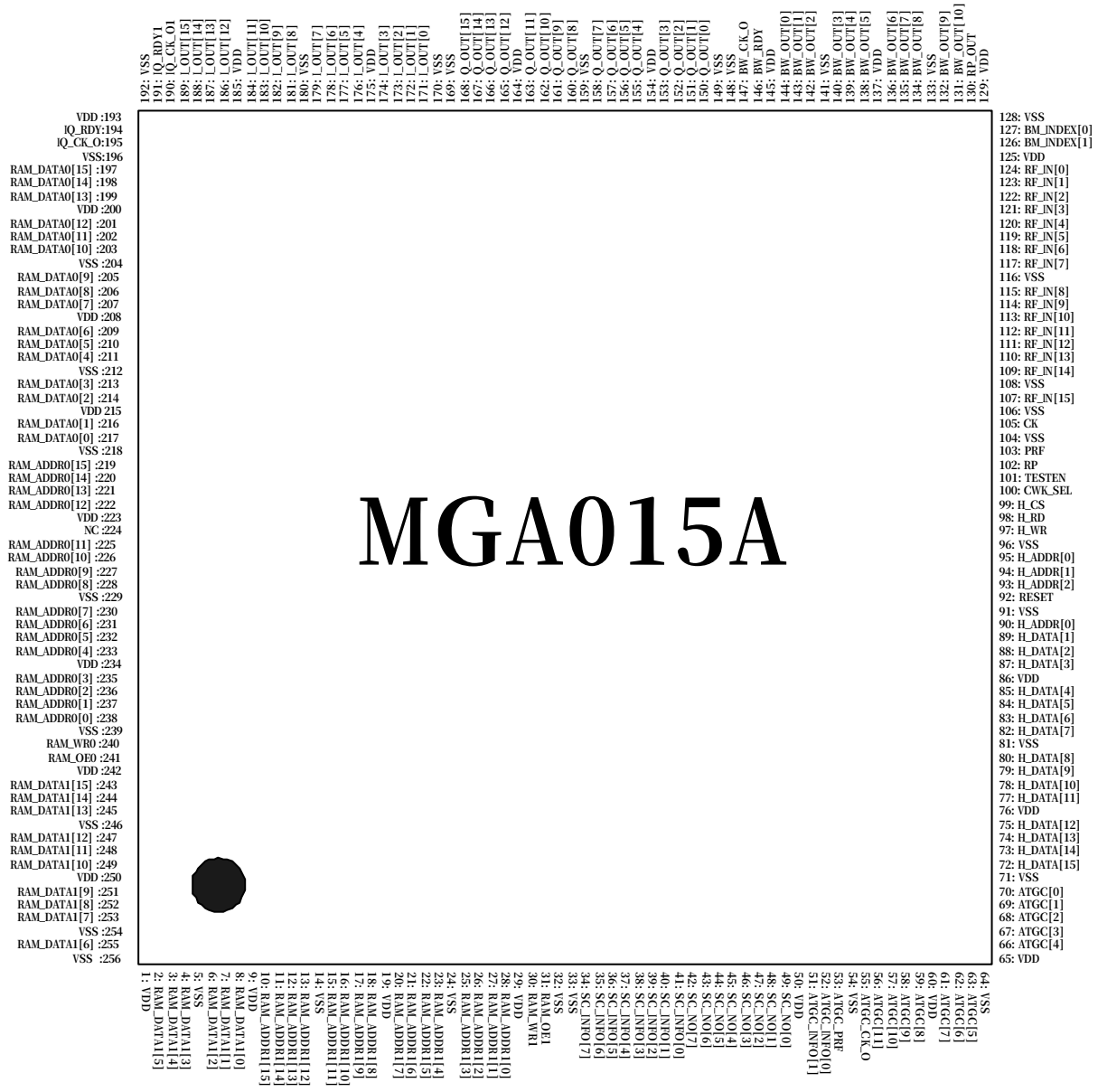
6.5.2 BLOCK DIAGRAM



6.5.3 I/O Signal Overview



6.5.4 Pin Diagram



7. I/O Map

I/O PORT	DESCRIPTION
10H	TIMER 01 start address /OF, /RPCLK -> rate pulse blank
14H	Timer 01 start address /RP1,/ DELAY OF, /EADC1; /EADC1
18H	Timer 02 start address /RP2, DELAY OF /EADC2, /EADC2
1CH	Timer 03 start address /RP3, DELAY OF /EADC3, /EADC3
20H	Timer 04 start address /RP4, DELAY OF /EADC4, /EADC4
2CH	Analog gain control on MYSONO201 ;Write only port ; bit [4..7] : Gain
2DH	DFC curve Offset & Triple Freq. control ; on MYSONO201 ; Write only port ; bit [0..3] : DFC curve Offset ; bit [6..7] : Triple Frequency
2EH	B/B mode control port for scg on SA5000II ; Write only port ; bit 0 : High --> BB mode on ; Low --> BB mode off
2FH	Video format control port on SA5000II ; Write only port ; bit 0 : High --> NTSC method ; Low --> PAL method
30H	MGA003A PORT Bit [1..0] : Image Scale(Magnification) data for SCG(Sampling Clock Gen.) ; 00 .... most zoom-out image ; 01 ; 10 ; 11 .... most zoom-in image
31H	MGA003A PORT ; bit [4..0] : Probe ID data for SCG(Sampling Clock Gen.) ; 1xxxx .. linear probes ; 0xxxx .. convex probes
40H..41H	Frame momory GDC access ports
I/O PORT	DESCRIPTION
42H	Bit 0 : bank0 /bank1 selection flag [0/1] Bit [1..7] : reserved
43H	Frame memory column address Offset data
44H	Frame memory raw address Offset data

45H	Bit 0 : B-mode raw address Offset data bit 8 Bit 1 : B-mode raw address counter Down/Up flag[1/0] Bit [2..4] : Frame average Factors 000 … 1:0 001 … 1:0.33 010 … 1:0.6 011 … 1:1 100 … 1:1.67 101 … 1:3 Bit 5 : Ping-Pong On/ Off flag[1/0] Bit 6 : Double/Single scan flag[1/0] [1/0] sector mode only /default Bit 7 : Dual/Single mode flag [1/0] [1/0] right/ left memory GDC access
46H	Bit 0 : Cine/normal mode flag [1/0] Bit 1 : B-mode direction left/right change flag[1/0] Bit [2..6] : Reserved Bit 7 : You can not use this bit
47H	Test port of MGA001A [read/write] You can test the CPU address and data lines of MGA001A using this test port.
48H	; bit 0 : video display On/Off flag [1/0] ; (only image data) ; bit 1 : Linear/Convex flag [1/0] ; bit 2 : image Up/Down flag [1/0] ; bit 3 : memory selection flag ; [Bank0/Bank1 - 0/1] ; bit [5..4] : mode flag bits [1..0] ; 00 - B-mode ; 01 - M-mode ; 10 - B/B-mode ; 11 - B/M-mode ; bit 6 : B/B or B/M mode initialization ; On/Off flag [1/0] ; bit 7 : You can not use this port.
49H	bit [1..0] : image scale (Magnification) for DCG (Display Clock Gen.) ; control bits [1..0] ; bit [5..2] : probe ID bits [5..2] ; bit 6 : Normal/Fast mode flag [1/0] ; bit 7 : gray bar On/Off flag [1/0]
4AH	Display clock data ; ROM Offset address ; [left image in B/B mode]
4BH	Display clock data ; ROM Offset address ; [right image in B/B mode]
4CH	; Bit [2..0] : BRS[2..0] of RAMDAC ; bit [7..3] : You can not use these bits.

4DH	You can not use this port
4EH	BT478 RAM ADDRESS (B/W)
4FH	MGA003A TEST PORT
50H	Timer 0 start address - VERTICAL WINDOW delay of /VWND ;,clk=HS, gate=/VS, ; /VWND ;,clk=HS, gate=delay of /VWND ; reserved
54H	Timer 1 start address - HORIZONTAL WINDOW ; delay of /HWND ;clk=CLK6.3M, gate=/HS, ; /HWND ;clk=CLK6.3M, gate=delay of /HWND ; reserved
58H	Battery Voltage A/D convert port ; B0 : BAT_AD_CLK ; B7 : /BAT_AD_EN
59H	Host Address ; Bit[3:0] - Address Area ; Bit[5:4] : 11-Mid_Processor_CS(Default/disable:0) ; : 0-MCB014 0_CS, 1_CS select(Default/0) - ? ; : 1-F/E_CPLD_CS(Default/disable:0) ;>>> MID porcessor control address ; 30~37H - h_addr0~7(p_bfic_addr0~7) ;>>> BFIC & F/E board control address ; 00~07H - h_addr0~7(p_bfic_addr0~7) ; 21H - CPU_mode_addr(p_dbf_CPUmode) ; 22H - board_ver_read_addr(p_dbf_version) ; 23H - board_buf_en_addr(p_dbf_bufferenable) ; 24H - bfic_select_addr(p_dbf_bficselect) ; 25H - bfic_reset_addr(p_dbf_reset) ; 26H - txmask_initmode_addr(p_dbf_txmask_init)
5AH	Host Data Low[7:0]
5BH	Host Data High[15:8]
5CH	; B7 : LCD control ; B0 : LCD_ENABLE(default enable)
5DH	POST_WR, POST_RD
5EH	* When this port is written, ; Post address will be reset. ; B1 : POST_OVL(default disable) ; B2 : POST_MENU(default disable) ; B7 : /POST_EN(default disable)

5FH	Probe element output only port ; B1..0 : Probe element ; 0 : 64el ; 1 : 80el ; 2 : 96el ; 3 : 128el ; B7..3 : Probe ID ; B7 : 1=LINEAR, 0=CONVEX ; B6 : 0 ; B5 B4 B3 = PROBE ID
60H	Overlay GDC parameter & status port
61H	Overlay GDC command port
62H	POST MEMORY ADDRESS SELECT PORT ; B0..B4, 32 post memory
63H	Period out port ; 3EH .... 0.8 MHz probe ; 18H .... 2 MHz probe ; 0DH .... 3.5 MHz probe ; 09H .... 5 MHz probe ; 06H .... 7.5 MHz probe ; 04H .... 10 MHz probe ; 03H .... 12.5 MHz probe ; Freq = (50.4Mhz)E-1 ;= 19.84ns
70H	SCAN LINE data
71H	; bit [2..0] : Low Pass Filter selection data 600CINE ; bit [4..3] : Triple Frequency
72H	; bit 0 : Probe Selection flag ; If cart unit is not exist, This bit is not mean. ; bit [3..1] : Focal point ID data ; 000 .... nearest point ; 111 .... farest point ; 00, 01, 10, 11 ; FP1 FP2 FP3FP4 ; bit [7..4] : Dynamic Range control data [DR]
73H	; read only port ; bit 0 : clock second bit ; bit 1 : NTSC/PAL selection flag [0/1] ; bit 2 : Probe disconnection flag ;[No_probe/Probe..1/0] ; bit [7..3] : Probe ID data ; 1xxxx .... linear ; 0xxxx .... convex

74H	; only bit[2..0] is used ; bit 0 : Character display enable flag ; [Enable/Disable..1/0] ; bit 1 : Graphic display enable flag ; [Enable/Disable..1/0] ; bit 2 : Mark display enable flag ; [Enable/Disable..1/0] ; bit 3 : Menu display enable flag ; [Enable/Disable..1/0]
75H	; bit [5..0] : ; Program memory bank selection data ; for access of 0000H -- BFFFH ; (i.e. A15..A14 ==> 00,01,10), ; [EX_A19..EX_A14==> 000000] ; for access of C000H -- FFFFH ; (i.e. A15..A14 ==> 11), ; Bit [5..0] : [EX_A19..EX_A14] ; B6 : reserved ; B7 : Gate Enable flag of /RP2 timer [Disable/Enable..1/0]
76H	High Voltage control data ; 00h .... : 55V ; 10H ; 7Fh .... : 65V ; : ; FFh .... : 75V ; 70H
77H	M-mode column address (write only)
78H	; Before /MENA 0 ; after /MENA 1 ; Generate /SCG_RP, /LOAD_OF
79H	; Doubling flag : ON = 0 ; 1 ; by falcon 94.11.07 ; OFF = 1 ; 0 ; by falcon 94.11.07
7AH	Focal Point Id Map ; bit1,bit0 ... 1st Focal Point Id ; bit3,bit2 ... 2nd Focal Point Id ; bit5,bit4 ... 3rd Focal Point Id ; bit7,bit6 ... 4th Focal Point Id
7BH	F/M test port ; bit4..0 : increment of counter ; bit5 : 0=off/1=blink function ; bit6 : 0=row/1=col ; bit7 : 0=off/1=on
7CH	; Focal point

7EH	; test port of Xilnx4003H You can test the CPU address and data lines of Xilinx4003H using this test port.
7FH	test port of Xilnx4003H You can test the CPU address and data lines of Xilinx4003H using this test port.
80H	Clock_cs READ port
090H	Flash Momory Command port ; B0: ALE ; B1: CLE ; B2: Flash Chip Enable 1=Enable, 0=Disable ; B3: Smart Midea Chip Enable ; B4: Flash2 Chip Enable ; B5: ECC generation mode 1=512B, 0=256B ; B6: ; B7: Flash, Smart, Flash2 Spare Area Enable 0=Enable
091H	Flash Memory Data Port
092H	CINE DRAM ADDR ROW
093H	CINE DRAM ADDR COL
094H	CINE DATA port
095H	CINE Access frame (1frame :256x256) ; B[6..0] : Frame # ; B7 : 1=high block, 0=low block ;ROW addr : 256-512, 0-255 <--- only concept
096H	VIDEO Access Mode ; B1: 1=noninterace V_buffer read stop on, 0=off ; B2: 1=noninterace or interace V_buffer write hold on, 0=off
097H	FLASH MEMORY ; B0: Flash Ready/Busy ; B1: Smart Media Ready/Busy ; B2: Flash2 Ready/Busy ; B[3..6]:Reserved ; B7: Smart media insert 1=insert, 0=not insert

099H	SRAM Command ;B0: SRAM addr16 ;B1: SRAM addr17 ;B2: SRAM addr18 ;B[3..6]: reserved ;B7: 1=CPU access, 0=SYSTEM access ;B2&B1 B0 ; 0 x : Frame grabber addr space ; 1 0 : OS_buff front, for smart media ; 1 1 : OS_buff back, for temp memory
09AH	CINE Command Port ; B0: Cine on command 1: Cine on, 0: Cine off ; B1: FM_CINE Select command 1:FM Display, 0: Cine Display ; B2: 1=CPU access to DRAM, 0=SYSTEM access to DRAM ; B3: mode change LOW-->HIGH-->LOW One shot pulse
I/O PORT	DESCRIPTION
09BH	CINE Current Writing Frame ; B[6:0] ; B7: Cine Full Flag
09CH	CINE Current Reading Frame ;B[6:0]
09DH	CINE Status ; B0: ; B1: Clear_on_off 1:Clear On, 0:Clear End ; B2: ; B3: REAL WT ON 1:real 0:not real ; B4: CINE RD ON 1:CINE read, 0:not CINE
09EH	; B[0..7]: SRAM Addr
09FH	; B[0..7]: SRAM Data
0A0H	UART2 Chip [8250 used for PC interface] on MYSONO201
0A8H	Status write & read port in MYSONO201 status write port on MYSONO201 ; bit0 - Probe not_exist/_exist ; bit1 - BB/_B mode flag for SCG on MYSON201 ; bit7 - Print on status read port in MYSONO201I ; bit0 - RSTSI - for keyboard ; bit1 - RSTSE - for Remote controller ; bit2 - RSTSP - for PC interface

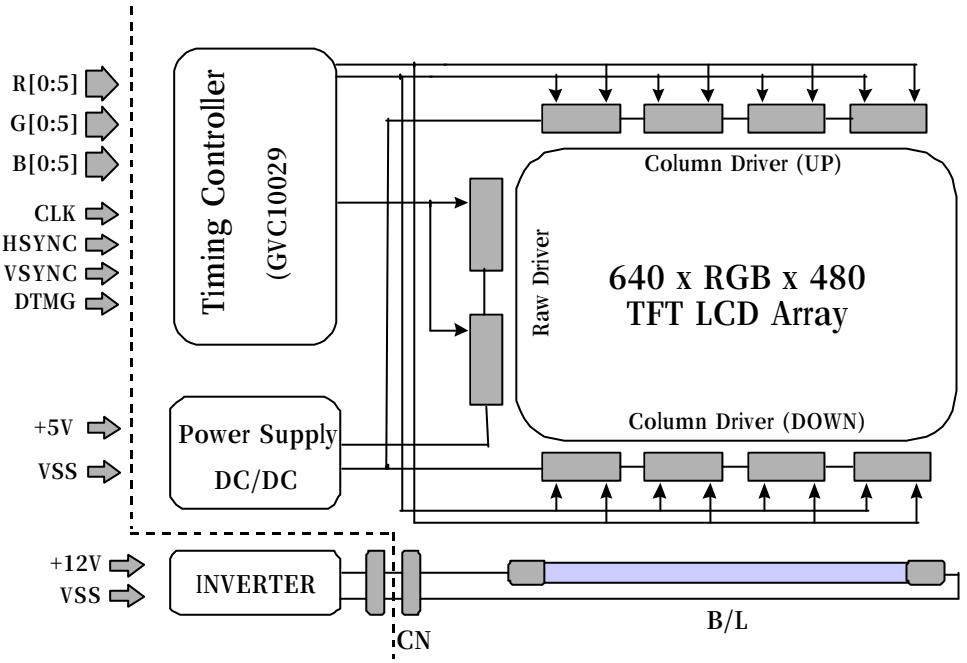
0B0H	74ACT715 Programmable Video Sync Generator Address Register
0B1H	Data Low : Temporary BIT
0B3H	Data High : Temporary BIT
0B4H	Modified M-mode ETRG length
0B5H	M-mode Fixed /ETRG Window Trigger Signal for FPGA
0B7H	B5 : EVEN V-SYNC
0B8H	BATTERY RELATIVE STATE OF CHARGE 1-100 ; B7 - 1 : battery exist, 0 : no ; B5 - 1 : transition exist, 0 : no ; B4..B0 : state of charge
0B9H	B0 : beamforming ETRG enable ; 1 : start download trigger ; 0 : end download trigger ; B1-B7 : Not used
0E0H	Clock Chip [RP5C01]
0F0H	UART0 Chip [8250 used for key interface]
0F8H	UART1 Chip [8250 used for remcon unterface]

1.LCD

1.1General Description

The LG LCD model LP064V1 LCD is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Tube (CCFT) back light system. The matrix employs a-Si Thin Film Transistor as the active element.

It is a transmissive type display operating in the normally white mode. This TFT-LCD has a 6.4 inch diagonally measured active display area with VGA resolution (480 vertical by 640 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a pallete of more than 262,144 colors.The LP064V1 LCD is intended to support applications where low power consumption, weight and thickness are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP064V1 characteristics provide an excellent flat panel display for office automation products such as portable computers and NTSC application.



1.1.1General Display Characteristics

The following are general feature of the model LP064V1 LCD;

Active display area	6.4 inches(cm) diagonal
Outsize dimensions	168W x 123 H x 9.0D mm Typ.
Pixel pitch	0.204 mm * 0.204 mm
Pixel format	640 hor. By 480 ver. Pixels
	RGB stripe arrangement
Color depth	6-bit
Display operating mode	transmissive mode, normally white
Surface treatment	hard coating(2H), anti-glare treatment of the front polarizer

1.2 Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1 Absolute Maximum Rations

Parameter	symbol	Values		Units	Notes
		Min.	Max.		
Power Input Voltage	V_{DD}	-0.5	+5.5	Vdc	at 25℃
Logic Input Voltage	$V_{L/H}$	0	V_{DD}+0.5	Vdc	at 25℃
Operating Temperature	T_{OP}	0	+50	℃	1
Storage Temperature	T_{ST}	-20	+60	℃	1

1.3 Electrical Specifications

The LP064V1 requires two power inputs. One is employed to power the LCD electronics and to derive the voltages to drive the TFT array and liquid crystal. The second input which powers the backlight CCFT, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2 Electrical Characteristics:

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
MODULE:						
Power Supply Input Voltage	V_{DD}	4.5	5.0	5.5	Vdc	
Power Supply Input Current	I_{DD}	-	180	280	mA	1
Ripple/Noise	-	-	-	60	mV	
Logic Input Level, High	V_{IH}	$0.7V_{DD}$	-	VDD	Vdc	2
Logic Input Level, Low	V_{IL}	Vss	-	$0.3V_{DD}$	Vdc	2
Power Consumption	P	-	0.9	1.54	W	1
BACKLIGHT						
Backlight Input voltage	V_{BL}	-	355	385	V_{RMS}	3
Backlight Current	I_{BL}	3.0	5.0	9.0	mA	
Lamp Kick-Off Voltage		-	-	680	V_{RMS}	25±2℃
		-	-	860		0℃
Operating Frequency	F_{BL}	35	55	80	KHz	

1.4 Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0º. Appendix A presents additional information concerning the specified characteristics.

Table 2 Optical Characteristics

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
Contrast Ratio	CR	100	-	-		1
Surface Brightness, white(IBL=5.0mA)	SB_{WH}	100	120	-	cd/m^2	2
Brightness Variation	SB_V	-	-	1.4		3
Response Time						
Rise Time	Tr_R		20	50	msec	4
Decay Time	Tr_D	-	35	50	msec	4
CIE Color Coordinates						
Red	x_R	0.557	0.587	0.617		5
	y_R	0.322	0.352	0.382		5
Green	x_G	0.254	0.284	0.314		5
	y_G	0.522	0.552	0.582		5
Blue	x_B	0.114	0.144	0.174		5
	y_B	0.092	0.122	0.152		5
White	x_W	0.292	0.322	0.352		5
	y_W	0.289	0.319	0.349		5
Viewing Angle(CR>10:1)						
x axis, right (Φ=0º)	θ			40		6
x axis, left(Φ=180º)	θ			40	degree, °	
y axis, up(Φ=90º)	θ			10		
y axis, down (Φ=270º)	θ			30		

1.5 Interface Connections

This LCD employs two interface connections, a 31 pin connector is used for the module and a three pin connector is used for the integral backlight system. The electric interface connector is a model DF9B-31P-1V, manufactured by Hirose. The mating connector part number is DF9-31S-1V or equivalent. The pin configuration for the connector is shown in the table below.

Table 3 Module Connector Pin Configuration

Pin	Symbol	Description	Notes
1	Vss	Ground	Connect to Vss, see Note 1
2	CLK	Main clock	
3	Hsync	Horizontal sync.	
4	Vsync	Vertical sync.	
5	Vss	Ground	Connect to Vss, see Note 1
6	R0	Red data	Red data least significant bit(LSB)
7	R1	Red data	
8	R2	Red data	
9	R3	Red data	
10	R4	Red data	
11	R5	Red data	Red data most significant bit(MSB)
12	Vss	Ground	Connect to Vss, see Note 1
13	G0	Green data	Green data least significant bit(LSB)
14	G1	Green data	
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data	Green data most significant bit(MSB)
19	Vss	Ground	Connect to Vss, see Note 1
20	B0	Blue data	Blue data least significant bit(LSB)
21	B1	Blue data	
22	B2	Blue data	
23	B3	Blue data	
24	B4	Blue data	
25	B5	Blue data	Blue data most significant bit(MSB)
26	Vss	Ground	
27	DTMG	Data Timing Signal	
28	Vdd	Power(+5V)	Connect to Vdd, see Note 2
29	Vdd	Power(+5V)	Connect to Vdd, see Note 2
30	OAS	O/A, A/V Selection	see Note3
31	NC	No Connection	

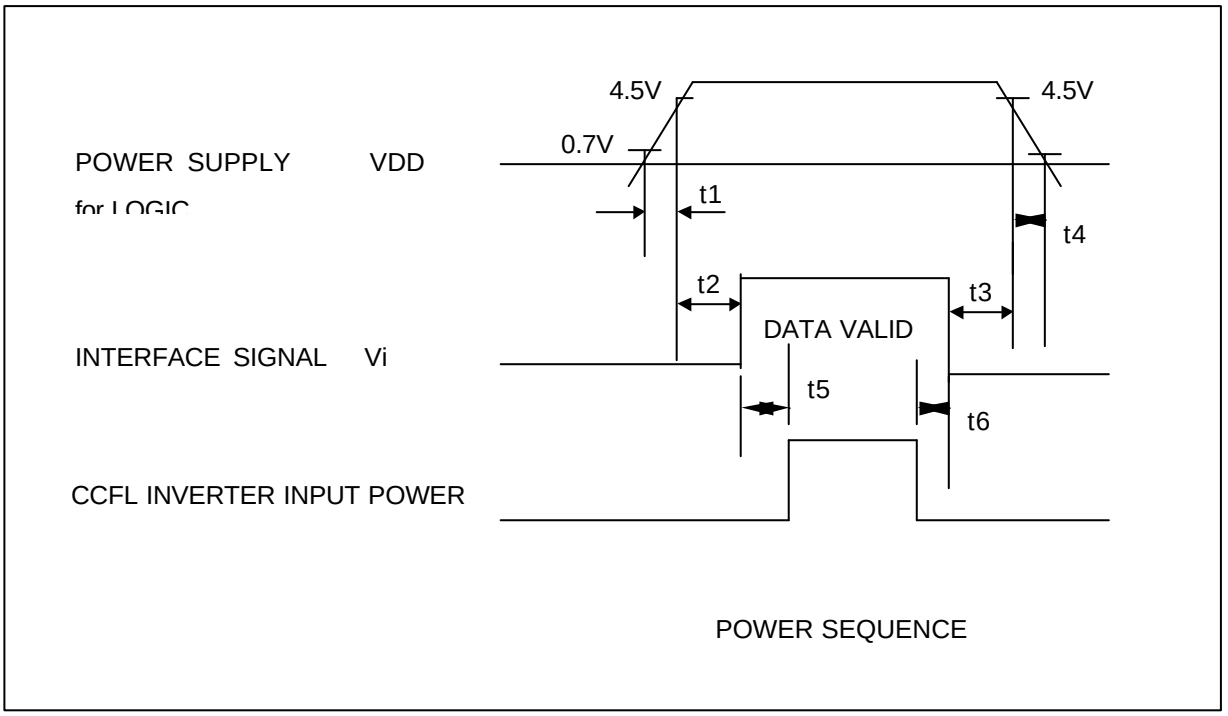
The backlight interface connector is a model BHR-03VS-1, manufactured by JST. The mating connector

part number is SM02(8.0)B-BHS-1-TB or equivalent. The pin configuration for the connector is shown in the table below.

Table 4 Backlight Connector Pin Configuration

Pin	Symbol	Description	Notes
1	HV	Lamp power input	1
2	NC	No connect	
3	LV	Ground	

1.6 Power Sequence



t1≤40msec, 0<t2≤50msec, 0<t3≤50msec, t4<1sec, 0< t5≤2 sec, 0<t6≤2sec

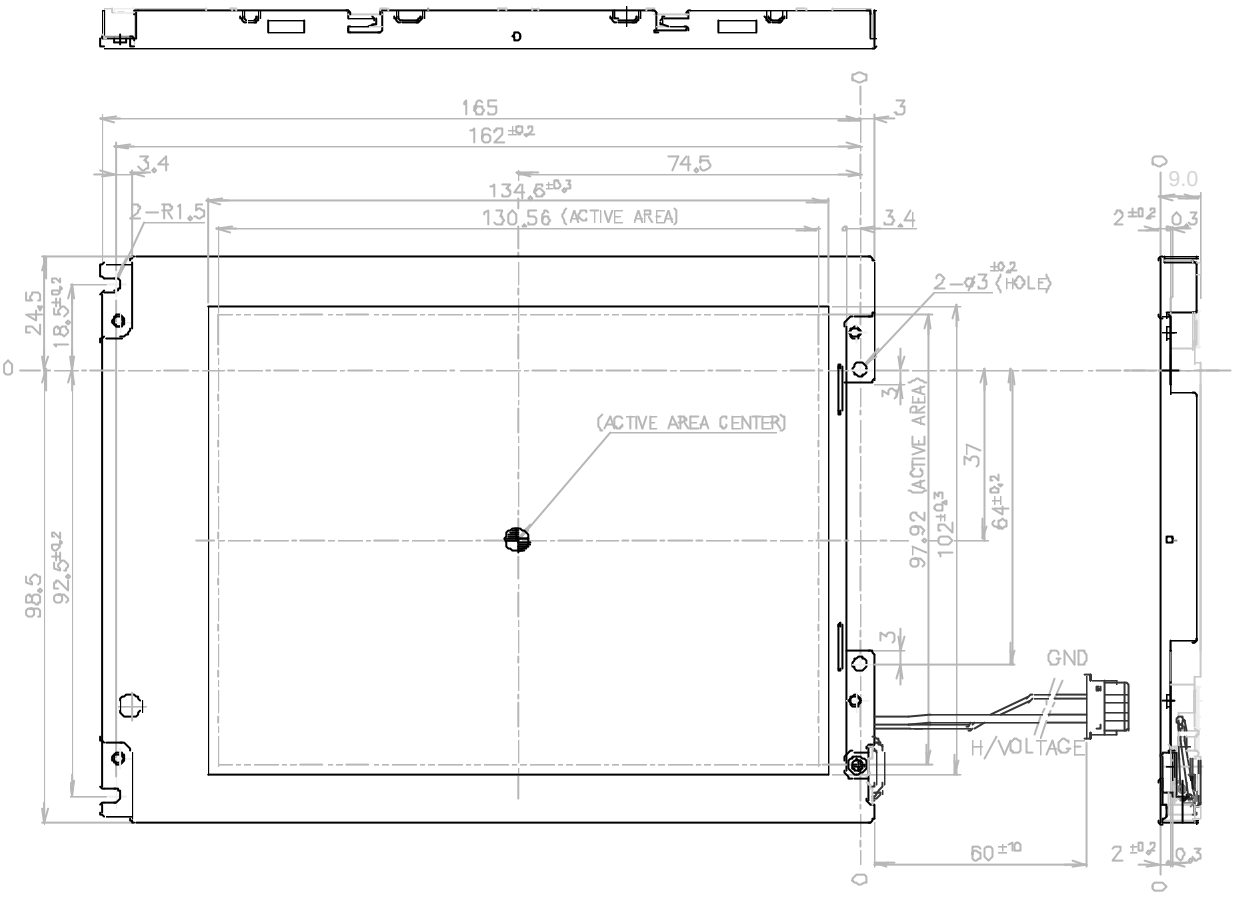
* Set 0 Volt < Vi(t) ≤V_{DD}(t)

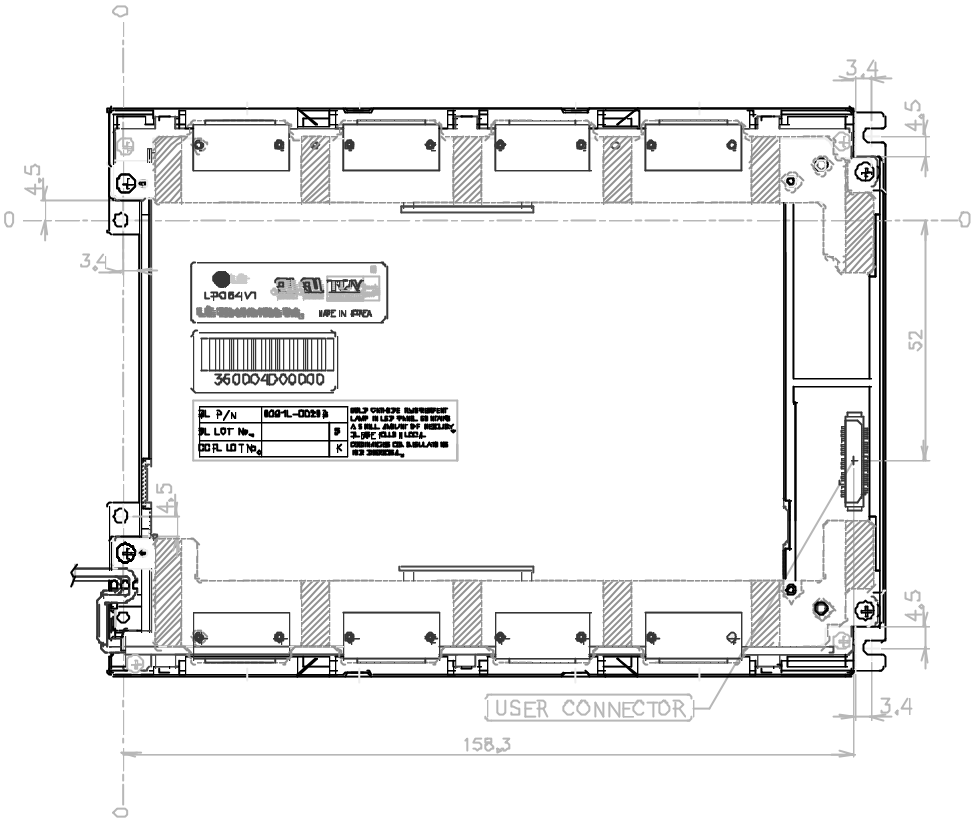
Here Vi(t), V_{DD}(t) indicate the transitive state of Vi, V_{DD} when power supply is turned ON or OFF

1.7 Mechanical Characteristics

The chart below provides general mechanical characteristics for the model LP064V1 LCD. The surface of the LCD has an anti-glare coating to minimize reflection and a 2H hard coating to reduce scratching. In addition, the figure below is a detailed mechanical drawing of the LCD. Note that dimension is given for reference purposes only.

Outside dimensions	Width	168 mm
	Height	123 mm
	Thickness	9.0 mm
Active Display area	Width	130.56 mm
	Height	97.92 mm
	Diagonal	163.2 mm
Weight (approximate)		230 g Typ.


165
162±0.2
3.4
74.5
134.6±0.3
130.56 (ACTIVE AREA)
2-R1.5
3.4
3
9.0
2±0.2
0.3
2-ø3±0.2 (HOLE)
24.5
18.5±0.2
(ACTIVE AREA CENTER)
97.92 (ACTIVE AREA)
102±0.3
37
64±0.2
98.5
92.6±0.2
GND
H/VOLTAGE
60±10
2±0.2
0.3


3.4
4.5
4.5
3.4
52
4.5
4.5
3.4
USER CONNECTOR
158.3

1.8 International Standards (TBD)

1.8.1. Safety

UL1950 "Safety of Information Technology Equipment Including Electrical Business Equipment.

Third Edition" Underwriters Laboratories, Inc. 1995

CAS C22.2 "Safety of Information Technology Equipment Including Electrical Business Equipment.

Third Edition" Canadian Standards Association, 1995

EN 60950 "Safety of Information Technology Equipment Including Electrical Business Equipment."

European Committee for Electro technical Standardization(CENELEC), 1995

Ref. No. EN 60950: 1992 + A1: 1993 + A2: 1993 + A3: 1995 E

(IEC 950: 1991 + A1: 1992 + A2: 1993 + A3: 1995, modified)

1.8.2. EMC

ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and

Electronic Equipment in the Range of 9kHz to 40GHz."

American National Standards Institute(ANSI),1992.

C.I.S P.R "Limits and Methods of Measurement of Radio Interference Characteristics of D.Information

Technology Equipment."International Special Committee on Radio Interference

EN 55 022 "Limits and Methods of Measurement of Radio Interference Characteristics of Information

Technology Equipment."European Committee for Electro technical Standardization

(CENELEC),1988

1.9 Handling Precautions

Please pay attention to the followings when you use this TFT/LCD module with Back-light unit.

1.9.1. Mounting Preacaution

1) You must mount Module using mounting holes arranged in 4 corners.
   Be sure to turn off the power when connecting or disconnecting the circuit.
2) Note that the polarizers are easily damaged. Pay attention not to scratch or press this surface with any hard object.
3) When the LCD surface become dirty, please wipe it off with a soft material. (ie.cottonball)
   Protect the module from the ESD as it may damage the electronic circuit (C-MOS).
   Make certain that treatment person's body are grounded through wrist bend.

4) Protect the module from the ESD as it may damage the electric circuit(C_MOS). Make certain that treatment person's body are grounded through wrist bend.
5) Do not disassemble the module and be careful not to incur a mechanical shock that might occur during installation. It may cause permanent damage.
6) Do not leave the module in high temperatures, Particularly in areas of high humidity for a long time.
7) The module not be expose to the direct sunlight.
8) Avoid contact with water as it may a short circuit within the module.

1.9.2. Operating Precaution

1) The spike noise causes the mis-operation of circuits.
   Be lower the spike noise as follows :
   VDD=±200mV, V1=±200mV(Over and under shoot voltage.)
2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
   And in lower temperature, response time (Required time that brightness is stable after turn on) becomes longer.
4) Be careful for condensation at sudden temperature change. Condensation make damage to polarizer or electrical contact part. And after fading condensation, smear or spot will occur.
5) When fixed pattern are displayed at long times, remnant image is likely to occur.
6) Module has high frequency circuit. If you need to shield the electromagnetic noise. Please do in yours.
7) When Back-light unit is operating, it sounds.
   If you need to shield the noise, please do in yours.

1.9.3 Electrostatic Discharge Control

Since module is composed with electronic circuit, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through list band etc.. And don't touch I/F pin directly.

1.9.4 Precaution For Strong Light Exposure.

Strong light exposure causes degradation of polarizer and color filter.

1.9.5 Storage

When storing module as spares for long time, the following precautions are necessary.

1) Store them in a dark place: do not expose then to sunlight or fluorescent light. Keep the temperature between 5 and 35 at normal humidity.
2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

1.9.6 Handling Precautions For Protection Film

1) When the protection film is pealed off, static electricity is generated between the film and the polarizer. This film should be pealed off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition. etc.
2) The protection film is attached the polarizer with a small amount of glue.If some stress is applied to rub the protection film against the polarizer during the time you peal off the film, the glue is apt to remain more on the polarizer. So please carefully peal off the protection film without rubbing it against the polarizer.
3) When the module with protection film attached is stored for long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is pealed off. Please refrain from storing the module at the high temperature and high humidity for glue is apt to remain in these conditions.
4) The glue may be taken for the modules failure, but you can remove the giue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with Normal-hexane.

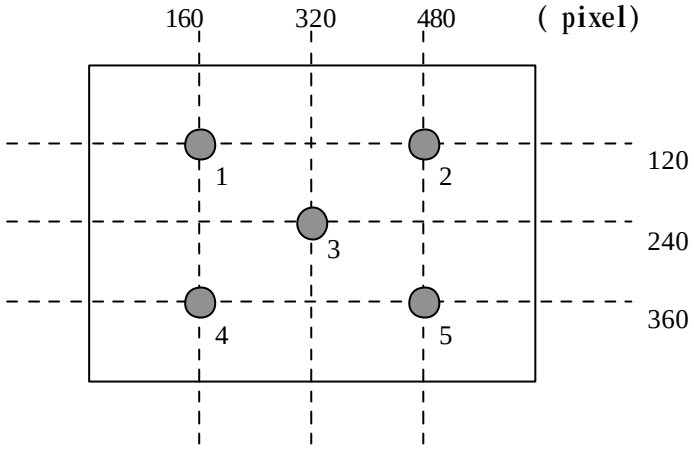
1.9.7 Safety

1) If module is broken, be careful to handle not to injure. (TFT/LCD and lamp are made of glass)

   Please wash hands sufficiently when you touch the liquid crystal coming out from broken LCDs.
2) As it is possible for PCB or other electronic parts of module to small to smoke and to take fire because of the short circuit. Please design the circuit of your instrument not to flow the electric current to TFT/LCD module more than 500mA. (by apply the fuse for example)
3) As Back-light unit has high voltage circuit internal, do not open the case and do not insert foreign materials in the case.

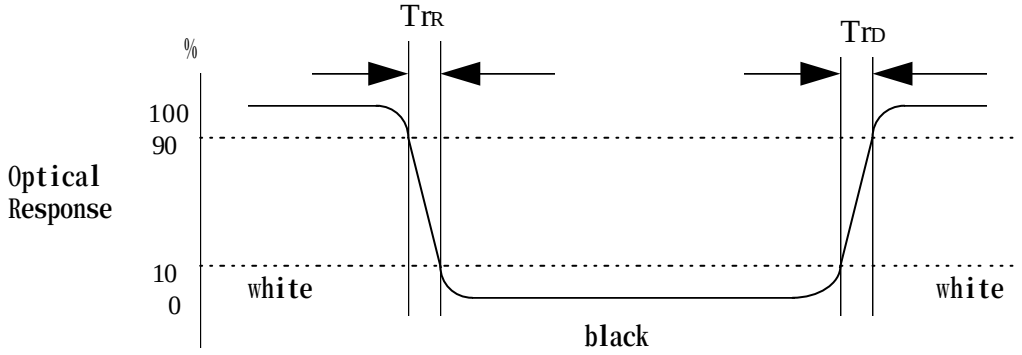
A-1 Brightness

<measuring point>



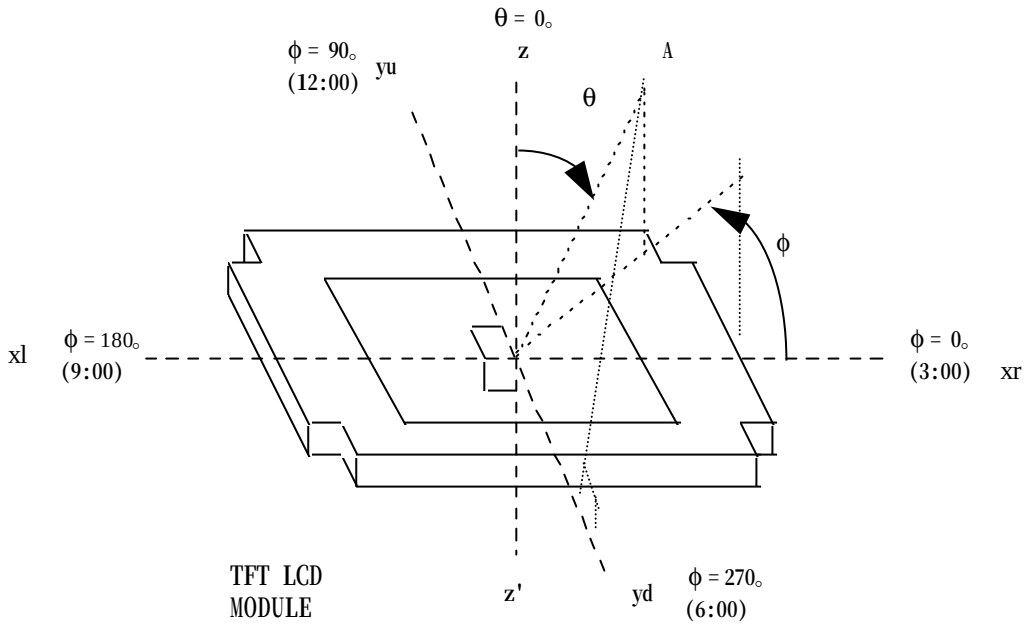
A-2 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



A-3 Viewing angle

<Definition of viewing angle range>



2.Apapter

2.1 SPEC. and Application Range

It is electric power supply of myso201, and the output is DC16V which is supplied by AC power source.

- Model Name : MYSONO201 ADAPTOR
- Inputting voltage and frequency : 50/60Hz±3Hz AC 90V – 264V
- Inputting current : Max 1.3A
- Outputting voltage and a rated current

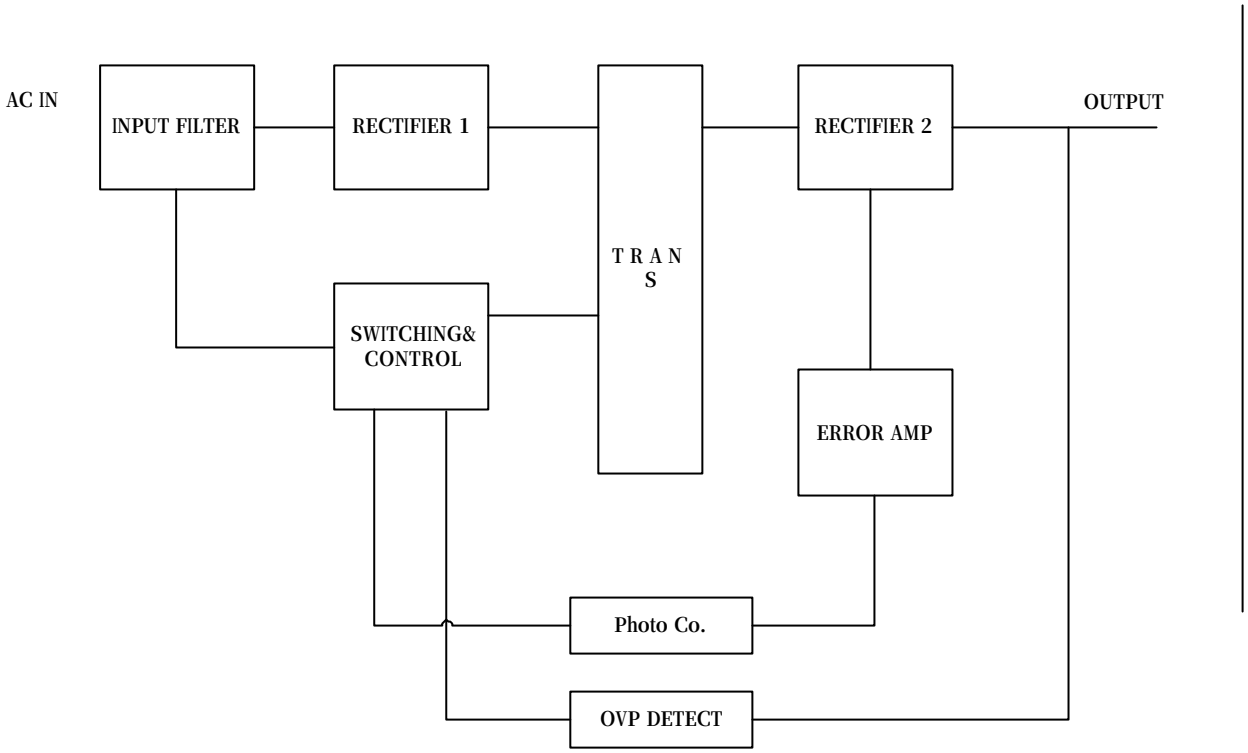
Voltage / Current	Min.	Normal	Max.	Ripple & Noise
	Non-load	2.3A	3.3A	
Output	16V±1	16V±1	16V±1	400 mV

notice)

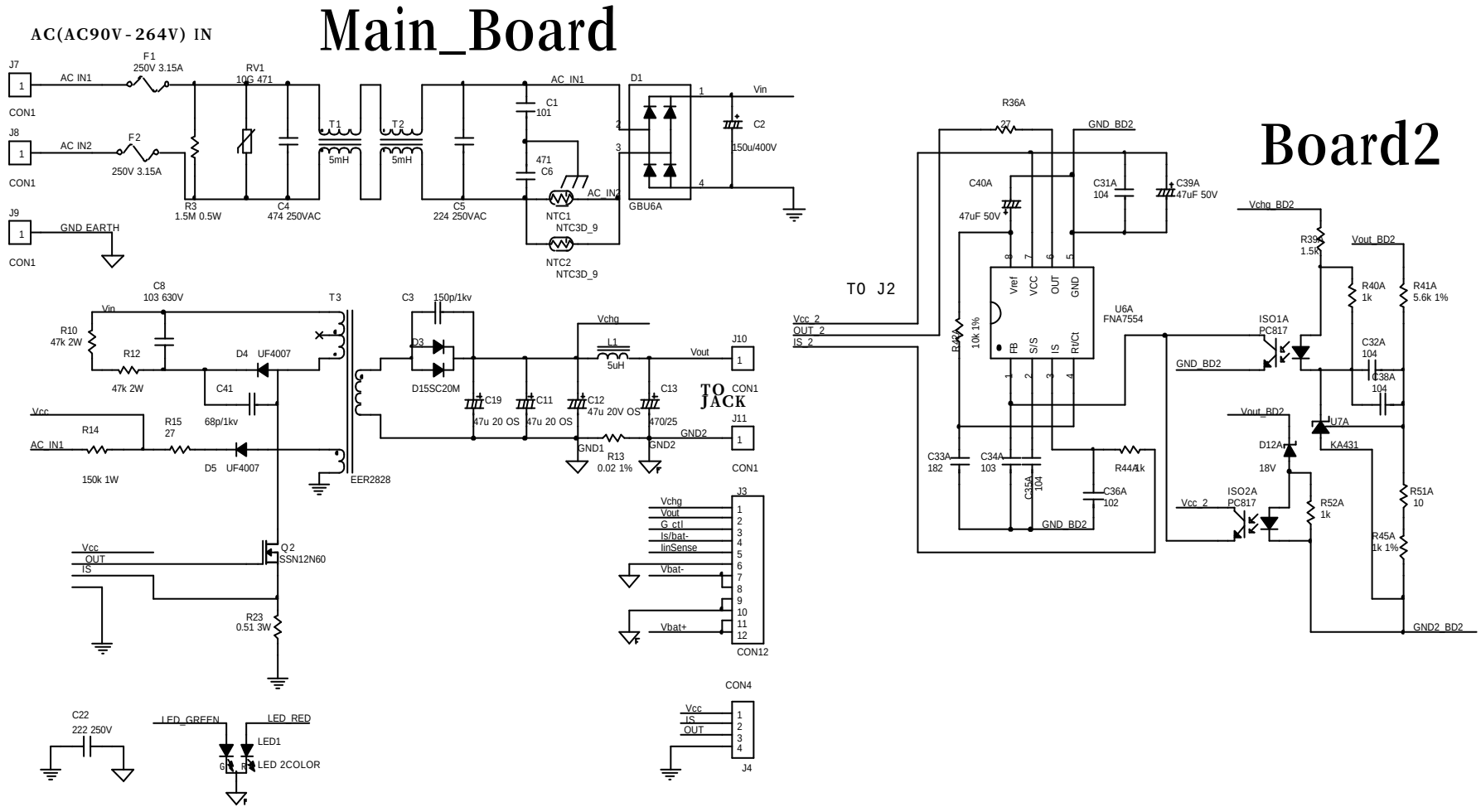
1) For measuring Allowed Ripple Voltage, 100uF electrolytic condenser on end of Probe and 0.1uf Ceramic condenser are closely connects with load.
2) measurement Scope is 100MHz Analog Scope.(50mV/0.5msec)

- cooling method : natural air cooling
- safety, electric wave, standard : satisfies IEC60601-1
- efficiency : the above 75 % (inputting 220V , MAX load standard)
- Environment of operation
  1) the range of temperature : 0℃ ~40℃
  2) the range of humidity : 10% ~90%RH(be careful dewdrop)
- Environment of storage
  1) the range of temperature :-15℃ ~70℃
  2) the range of humidity :10% ~95%RH(be careful dewdrop)
- the range of OCP 1) 16V :6A~10A
- the range of OVP 1) 16V :18A~21A
- Setup/Off Time(basis of Max Load)
  1) AC260V : below 2 sec
  2) AC90V : below 6 sec
- Rising/Falling Time
  1) 16V : below 30㎳
- Inrush current 1) Max 70A
- Over/Undershoot 1) below 3% output

2.2 Block Diagram

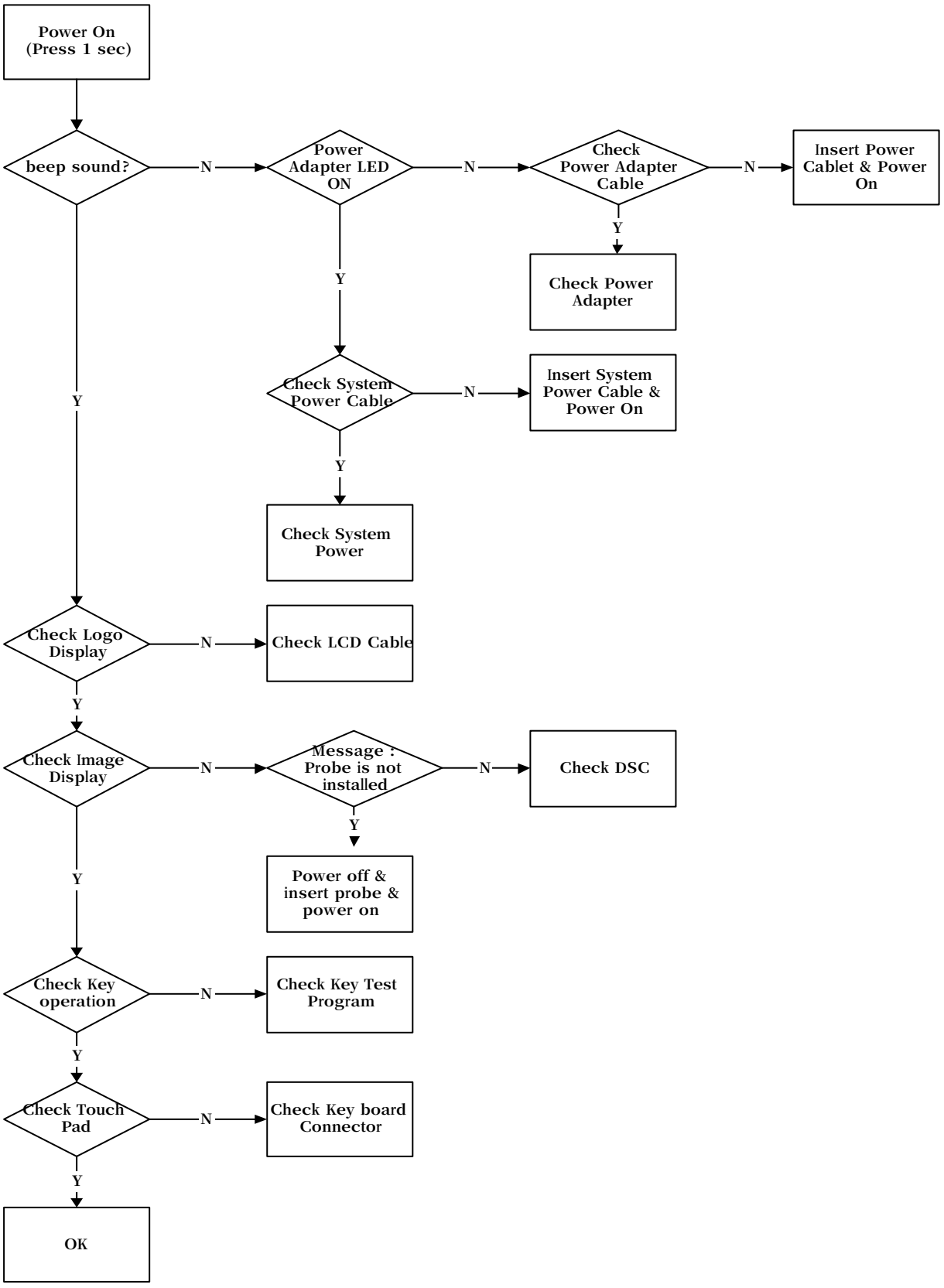


2.3 Schematic Diagram

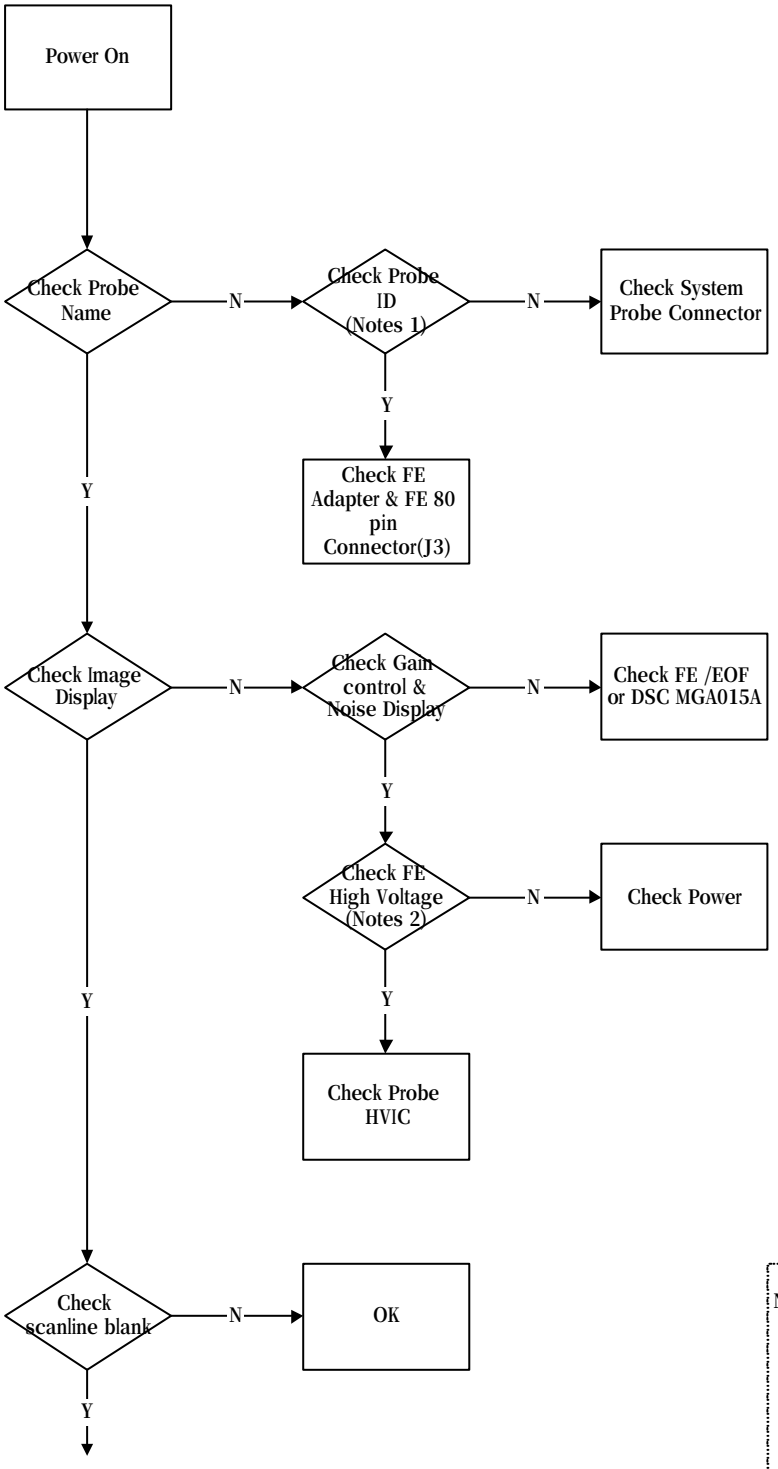


1. Trouble shooting

1.1System Booting Diagnosis



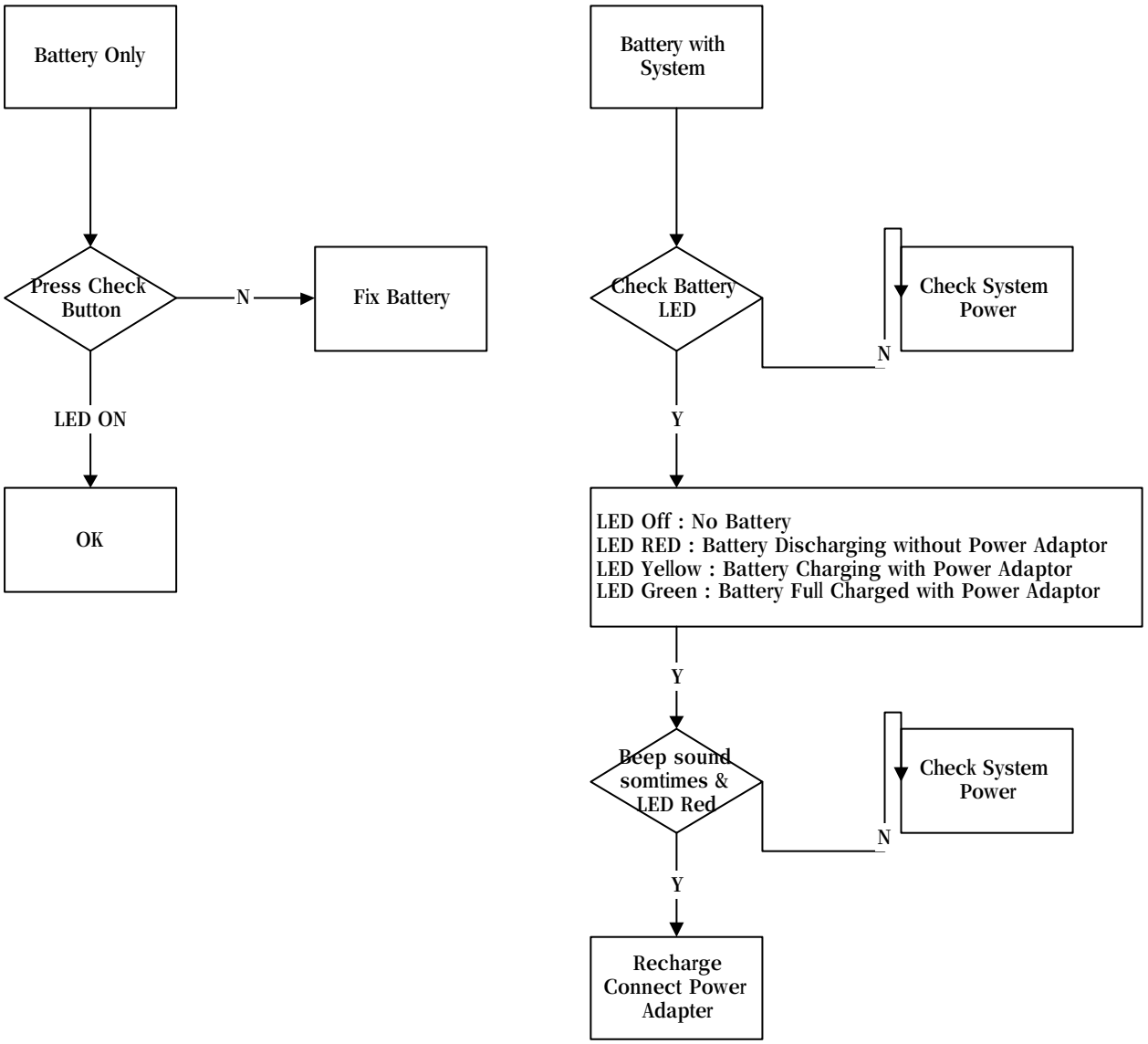
1.2 Image1 Diagnosis



Notes 1 : Probe Pin 1A is left bottoam
ID4 -- 5K
ID3 -- 4K
ID2 -- 2K
ID1 -- 1K
ID0 -- 6J
GND -- 3K
short means low
open means high

Notes 2 : +HV -- 4F,5F
-HV -- 2G,3G
GND -- 6F
/PRB_INS and ground must be shorted

1.3 Battery Diagnosis

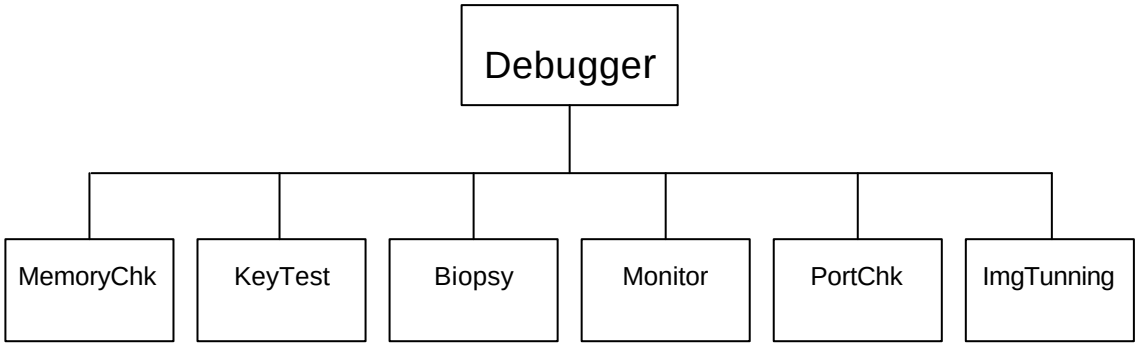


1.4 Etcetera Diagnosis

Defect symptom	Help index
System is no booting	1. Does the image appear on the screen? (only LCD does not display) ➔ Y : check the bad connecting with keyboard and main body. 2. Does parts get damaged? (Overlay GDC, CPU, FPGA, PROM, SYSTEM ROM..etc) ➔ Y : Change the parts
The image is not appeared	1. Does DSC board and F/E board connector is normal? ➔ N : check the connector connecting 2. When inputting image pattern in Debug mode, Does pattern appear are normal? ➔ Y : hardly output data from F/E board. /
The image is appeared as frosty	1. Does DSC board and F/E board connector is normal? ➔ N : check the connector connecting 2. Does Frame Memory is normal? ➔ N : change the FM
The image is appeared as frosty in Cine mode	Does Cine memory is normal? (or peripheral buffer) ➔ Change the Cine memory (0~15, 16~31)
M-mode image is not appeared or broken	Does Right Frame Memory is normal? (or peripheral latch) ➔ N : change the Memory and Latch
Keyboard defectiveness	Does some part of Key test is not working? ➔ Y : check the bad connecting with Keyboard and Main body and check the Key Rom
Not able to recognize Probe	1. Does Probe is normal?(recognize Probe ID) ➔ change the Probe 2. Do SPC and FE connector or F/E and DSC connector are normal? ➔ check the connector connecting 3. Does F/E CPLD is normal? ➔ change the parts
The image not be able to save or li-view does not working	1. How much space Does Flash memory have? ➔ N : image all delete and initialize 2. Does flash memory is normal? ➔ N : change the Flash memory ➔ Y : check the Flash memory controller(FPGA1)

2. Debug Mode

2.1 Debug Menu



MemoryChk Connect the Memory test mode

KeyTest Connect the Keyboard test mode

Biopsy Connect the Biopsy setting mode

Monitor Connect the Monitor display test mode

PortChk Connect the CPU I/O port test mode

ImgTunning It is Reserved mode. Not in use.

2.2 Image Memory Debugger Menu

IMAGE MEMORY DEBUGGER

1) Read 1 page from SRAM

From Image Grabber SRAM of special address, read the data as the unit of 1page(512 bytes).

3 bytes write :1st byte bit7 = 1 : cpu access, bit7=0 : system access

1st byte bit5..3 not used

1st byte bit2..0 address

2nd, 3rd byte address

ex1) From 800000 – 00000H, read 512 data.

ex2) From 870000 – 70000H, read 512 data.

2) Write 1 page to SRAM

On Image Grabber SRAM of special address, write the data as the unit of 1page.

4 bytes write : 1st, 2nd, 3rd is same with reading data.

4th data increment

ex1) write the 512 data such as 80000001 – ffh, 00h, 01h, 02h, … .

ex2) write the 512data such as 80000002 – ffh, 01h, 03h, 05h, … .

3) DUMP RAM

CPU memory(ROM, RAM) area was read as the unit of 128 bytes.

RAM area is by a000h~bfffh.

ROM area is 0000h~ffffh except RAM area.

ex1) From 0000 – 0000h address, read 128 bytes data.

ex2) From a000 – a000h address, read 128 bytes data.

4)CLEAR RAM

After Clear CPU NVRAM, initialize the system.

After initialize, user must perform Erased All Flash certainly.

5) Read 1 page from FLASH

From Flash memory of special area, read data as unit of 1page.

ccXXYY :

1) cc is chip number, 01=1, chip, 02=2, chip, 04=smart media

2) XXY is block address(0~1023)

3) Y is page address(0~15)

ex1) 010000 – read the 0 page among the first flashe memory 0th black.

ex2) 02000a – read the a(10) page among the second flash memory.

ex3) 04000f – read the f(15) page among the smart media 0th block.

ex4) 010014 – read the 4th page among the first flash memory 1th block.

6) Write 1 page to FLASH

On Flash memory of special area, write data as the unit of 1page.

ccXXYYii :

1) ccXXYY is such as reading.

2) ii is increment value of writing data

.

7) Read 1 page from DRAM

Read data as the unit of 1page on special range of Cine DRAM.

ffXX :

1) ff means frame number, 0~31

2) XX means row address, 0~256

ex) Read row data in 0000 – 0 of frame

8) Write 1 page to DRAM

Write data as the unit of 1page on range of special in Cine DRAM.

ffXXii :

1) ffXX is such as read

2) ii is increment value of writing data

ex) 050002 – 5번 frame, 0번 row에 2씩 증가하는 data를 write함

9) Initialize FLASH

Initialize the flash memory. Not in use.

10) Erase all FLASH

Delete all data in flash memory. But remain the biopsy data.

11) HOST Chip Select

When choose the 014, 015 chip, HOST Chip Select is used.

XY :

X : 0 = first 014, 1 = second 014, 2 = 015

Y : 0 = internal memory, 1= external memory

ex1) 00 – It is for access to first 014 internal memory .

ex2) 20 – It is for access to 015 internal memory.

12) HOST Address Select

- Choose 014, 015 internal or external memory address.

ex) 12f4h : choose the 01f4h address

13) HOST Data Write

This function is to write data of 2byte on selected address.

ex) 1155h – Write 1155h data from Selected chip 12f4h address.

14) HOST Data Read

This function is to read data of 2bytes on selected address.

ex) dd77h – Read data of 2bytes from selected chip 12f4h address.

15) HOST Data Dump

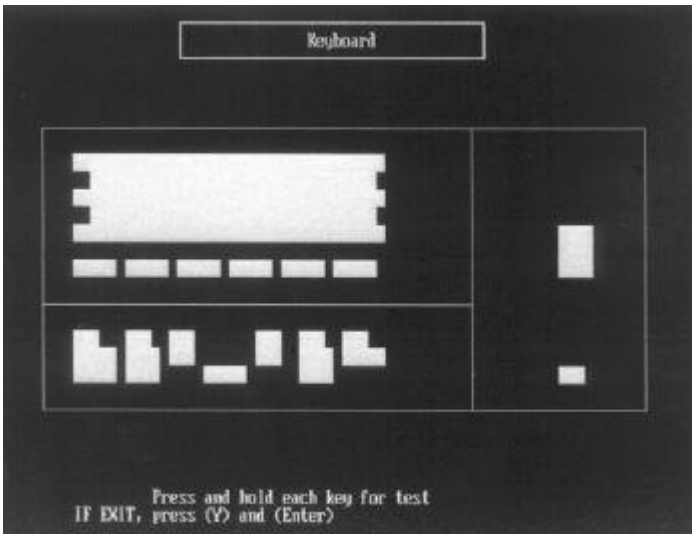
This function is to read data of 128bytes from selected address.

16) HOST Halt mode off

This function is to return to real mode, If this function is not work, Press “R” key which is short cut.

2.3 Keyboard Menu

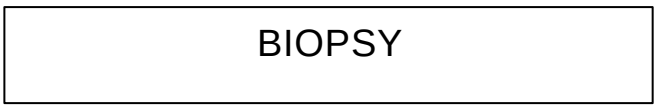
KEYBOARD



It is Keyboard test mode. When press the special key, appear and flick the letter on pressed key.

And In upper left, appear the scan code value applicable to the key. If user want to go out this mode, press the ”y” button, next press the enter button.

2.4 BIOPSY Menu



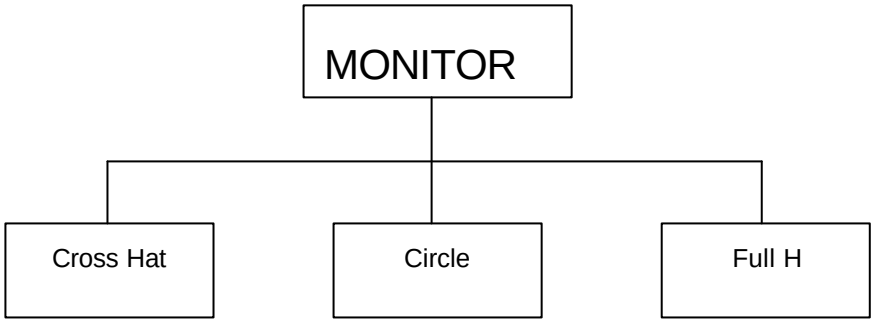
" Addition sight which has the line"

It is Biopsy setting menu. Biopsy supply 3 type and every one biopsy take 3 biopsy line on the screen. Middle-line is throughway of biopsy niddle and both side-line indicate a range of allowable error on throughway of niddle. Biopsy line information is saved in flash memory. Flash memory does not delete absolutely, unless user delete on purpose. Although some flash memory was broken, biopsy line is working normal because save the same information at three place on the flash memory.

When draw up a Biopsy line, It have to be applied to each 4 depth. When operate the direction and inverter function, user must check that whether niddle follow biopsy line or not.

When Choose the Setup button, appear sub-menu, Press the biopsy button in the sub-menu. There is Biopsy line on/off function in the biopsy menu. That function button is toggle key. If biopsy line is on, it is not deleted absolutely without mode change condition.

2.5 MONITOR Menu



"Addition 3 display mode"

Cross Hat Display overlay data as a checkered on the screen.

Circle Display overlay data as a circle on the screen.

Full H Display fill up the "H" letter on the screen.

2.6 8085 I /O DEBUGGER Menu

8085 I /O DEBUGGER

1) LOOPING READ I/O PORT
   - Repeat reading the data on special CPU I/O.
2) LOOPING WRITE I/O PORT
   - Repeat writing the data on special CPU I/O.
3) LOOPING WRITE/READ I/O PORT
   - Repeat reading and writing the data on special CPU I/O.
4) READ I/O PORT ONCE
   - Read data on special CPU I/O port, only one time.
5) WRITE I/O PORT ONCE
   - Read data on special CPU I/O port, only one time.
6) READ RAM MEMORY
   - Not in use.
7) WRITE TO RAM MEMORY
   - Not in use.
8) OVL ++, X. OVL –
   - Not in use.
9) READ RAM MEMORY
   - Not in use.
10) SCANLINE FIX
   - Print one scanline after fixed to change All scanline as one scanline.
11) SCANLINE NORMAL
   - It is made normal scanline printed condition.
12) SET PARM2.
   - Fix the writing value on the frame memory.
13) FM/WR COL ADDR
   - Fix the column address on the frame memory.
14) FM/WR ROW ADDR.
   - Fix the row address on the frame memory.
15) WRITE F/M STEP
   - Not in use.
16) FILL F/M BANK0
   - Fixed parameter value fill up on the Frame memory.

1.Spare Parts Assembling Diagram

1.1 TFT LCD Monitor Replacement Method

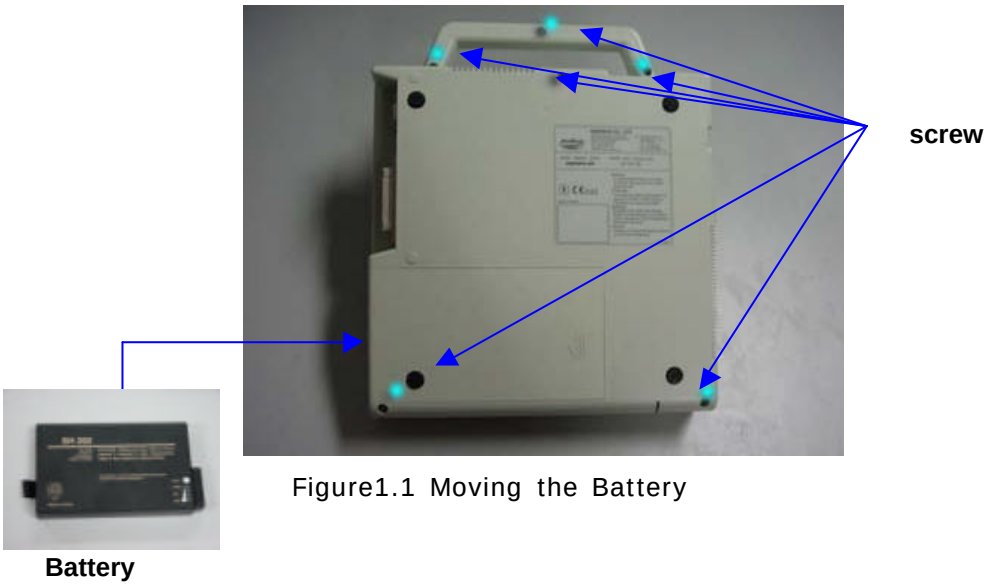


Figure1.1 Moving the Battery

1) Remove battery.(option)

2) To remove 6 screw on the cover body bottom, use “+” screwdriver.

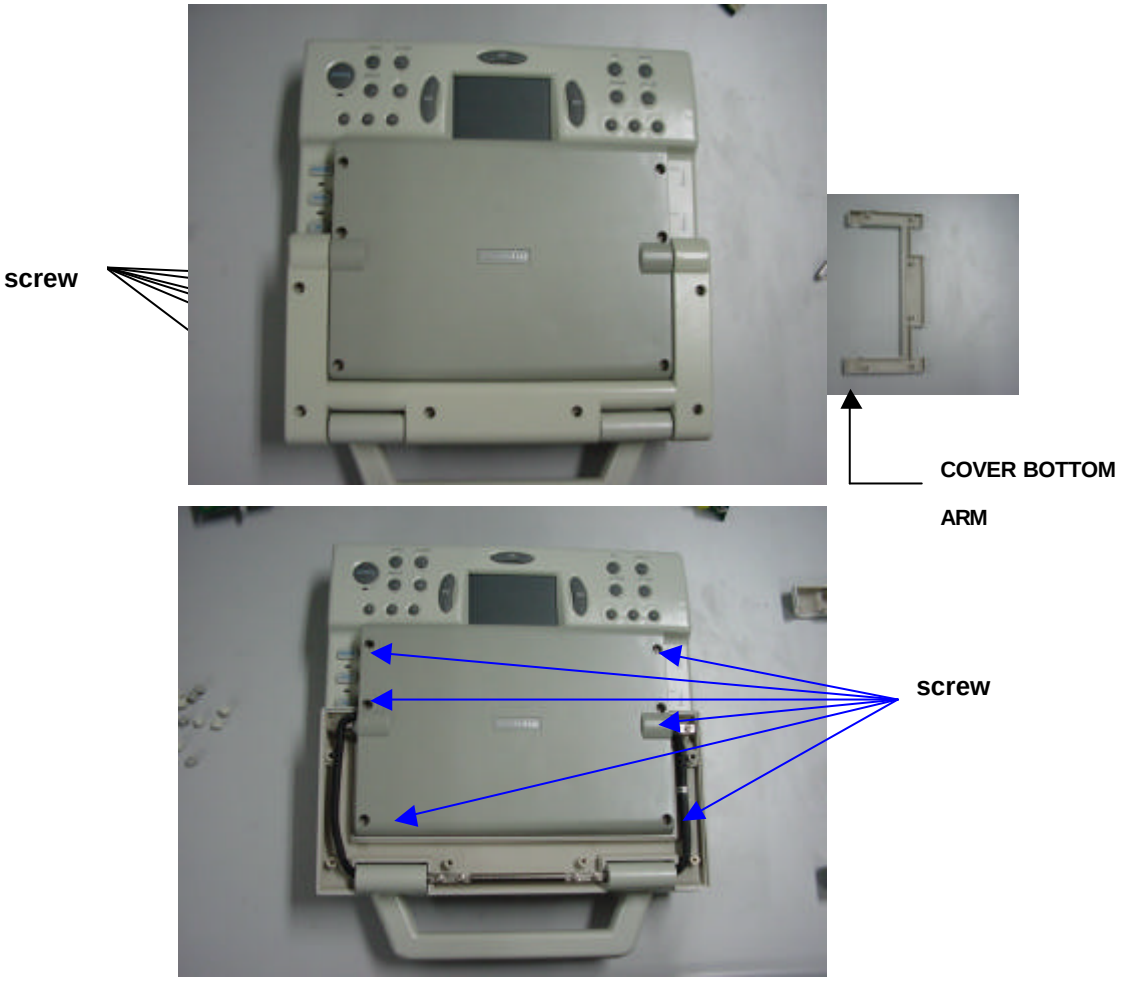
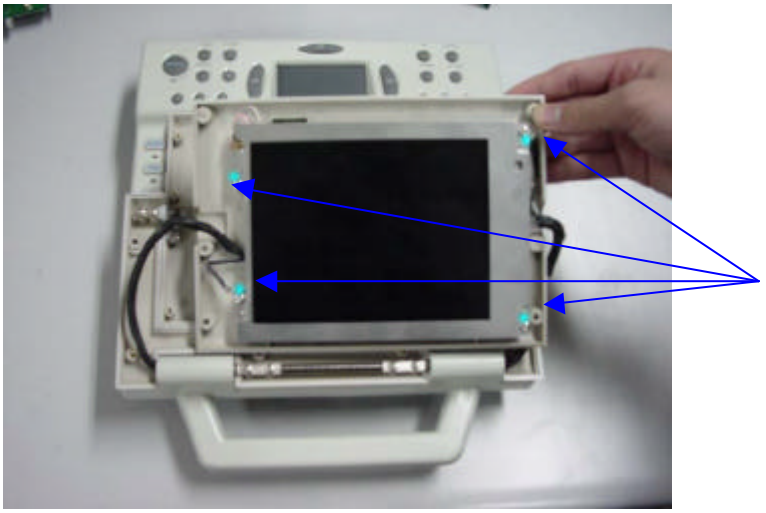
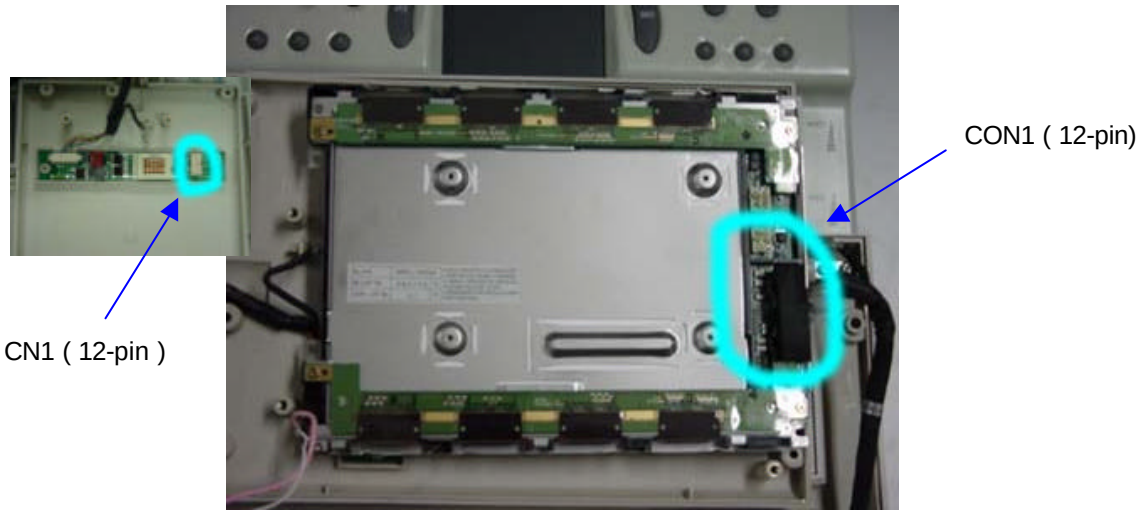


Figure1.2 Moving the LCD monitor

3) To remove 6 screw on the COVER BOTTOM ARM, use “+” screwdriver.

4) To remove 6 screw on the LCD monitor cover, use ”+” screwdriver.



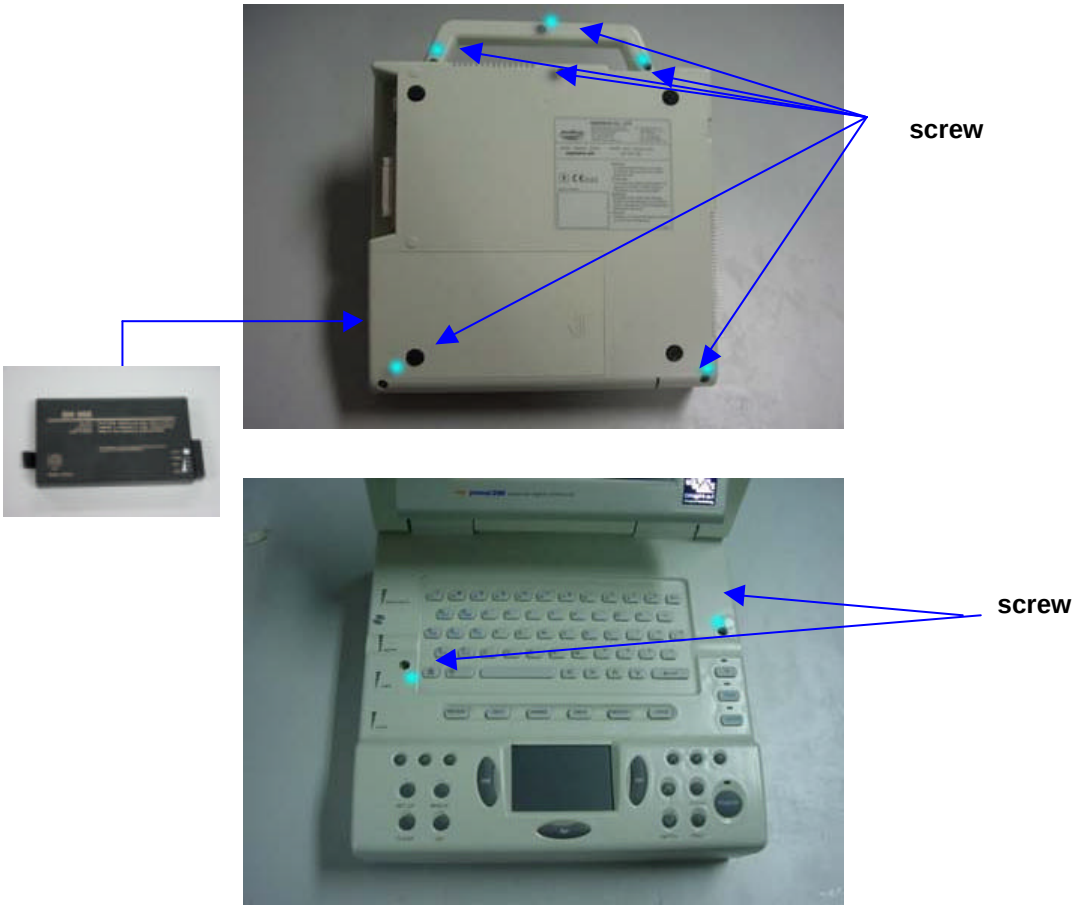


5) Remove 4 screw on the LCD monitor.

6) Disconnect with CN1(12pin) on the LCD INVERT board and CON1(31 pin) on the LCD main board.

7) Replace the LCD Display.

1.2 Key Matrix PCB Replacement Method



1) Remove battery on the cover body bottom.
2) Remove 6 screw on the cover body bottom.
3) When remove 2 screw on the cover body front, upper body cover is disconnected.
4) Disconnect Trackball & KEY MATRIX PCB J2 (8-pin flex circuit).
5) Disconnect J5, J6 on the KEY MATRIX.
6) To remove 21 screw, use “+” screwdriver.
7) Key Matrix PCB Replacement.

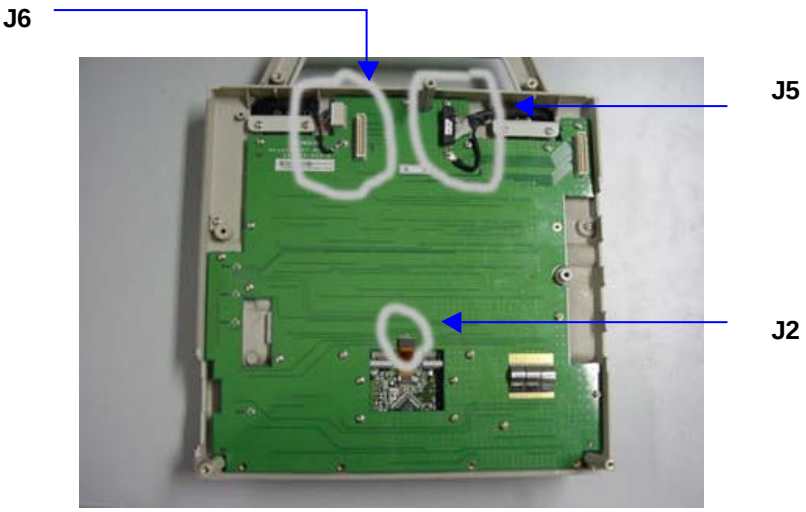
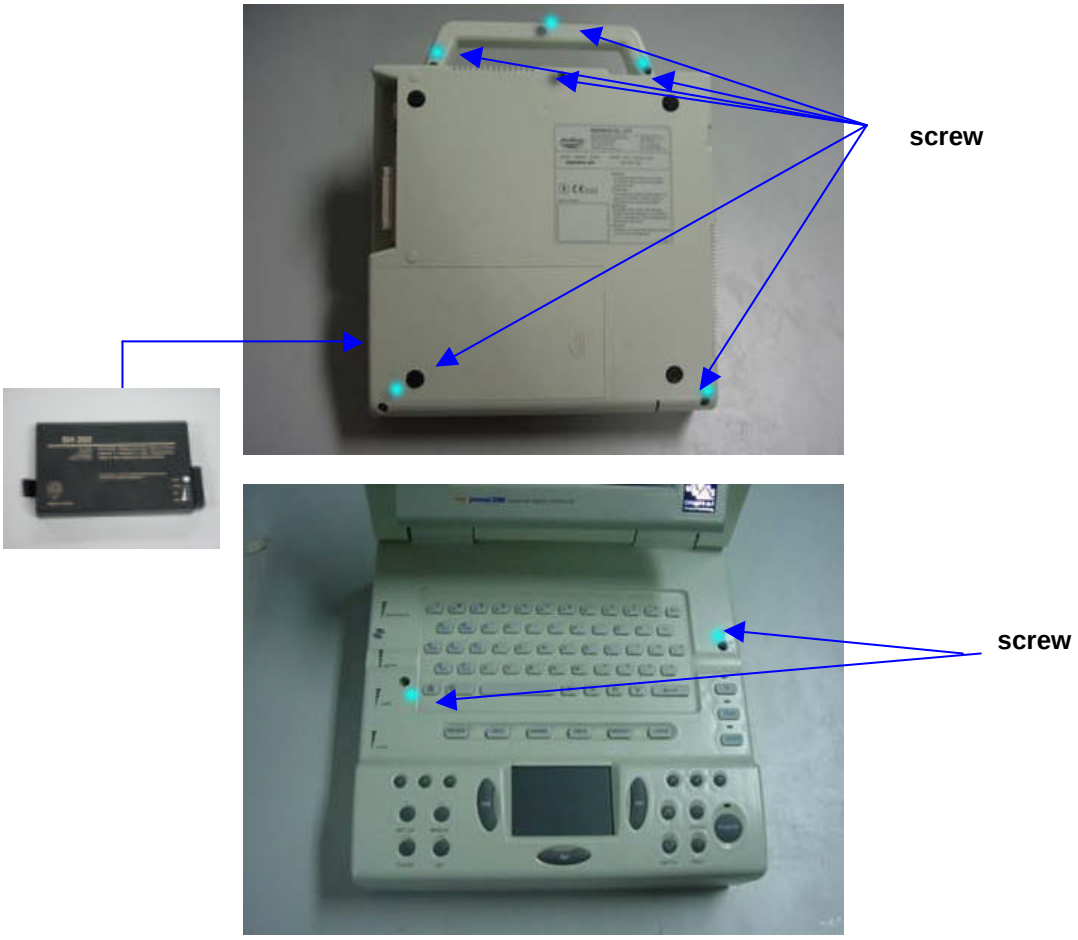
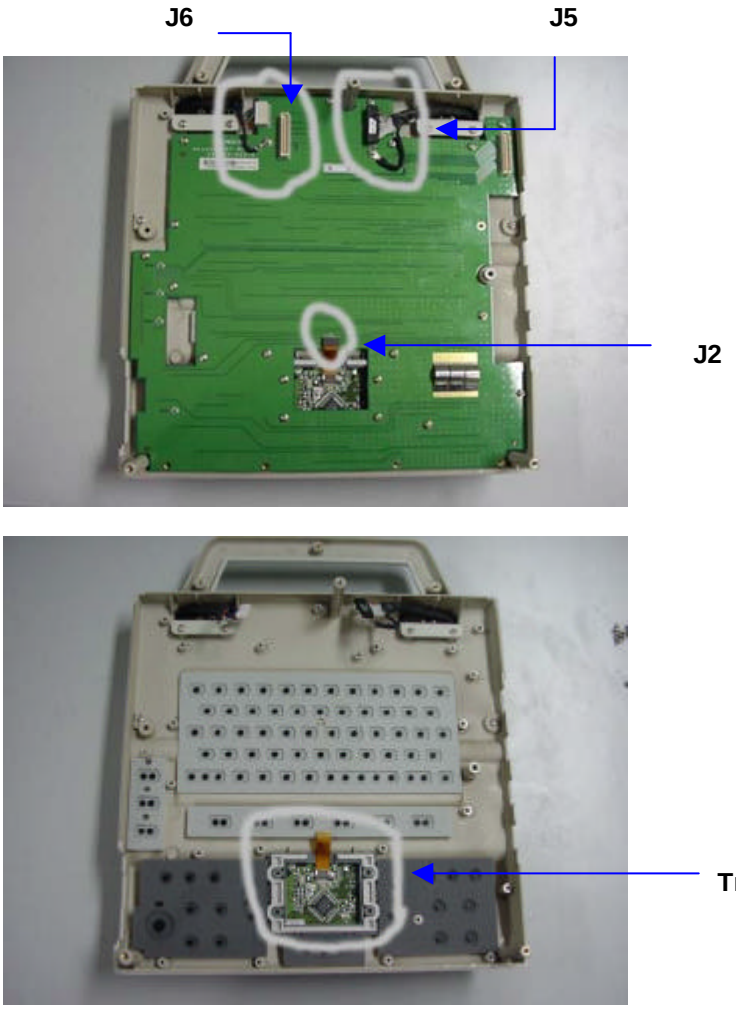


Figure 1.3 Removing the KEY MATRIX PCB

1.3 Trackball Replacement Method



1) Remove battery.
2) When remove 6 screw on the cover body bottom, upper body cover is disconnected.
3) When remove 2 screw on the cover body front, upper body cover is disconnected.



4) Disconnect J5, J6 on the KEY MATRIX PCB.
5) Remove 21 screw, use “+” screwdriver.
6) Disconnect Trackball & KEY MATRIX PCB J2 (8-pin flex circuit).

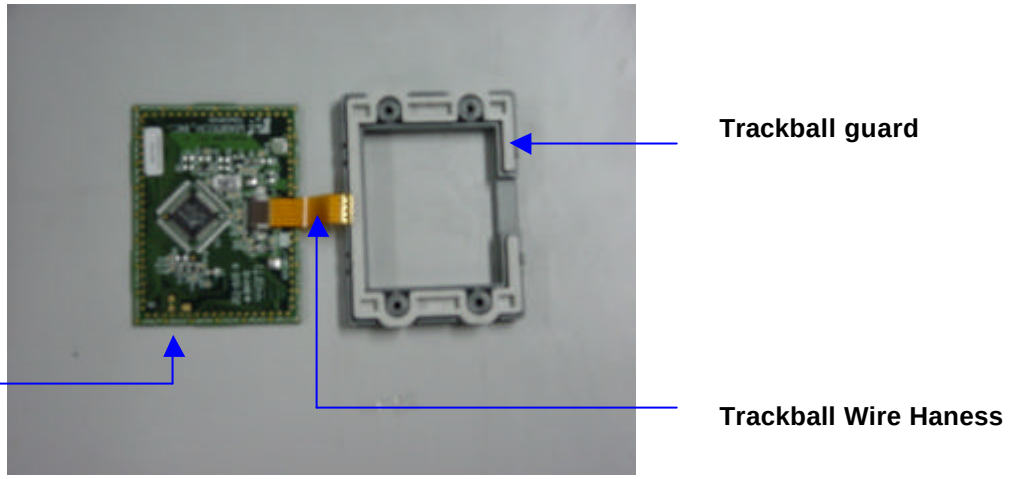


Figure 1.4 Removing the Trackball

7) Trackball Replacement

1.4 PCB Boards Replacement

1.4.1 DSC Board Replacement Method

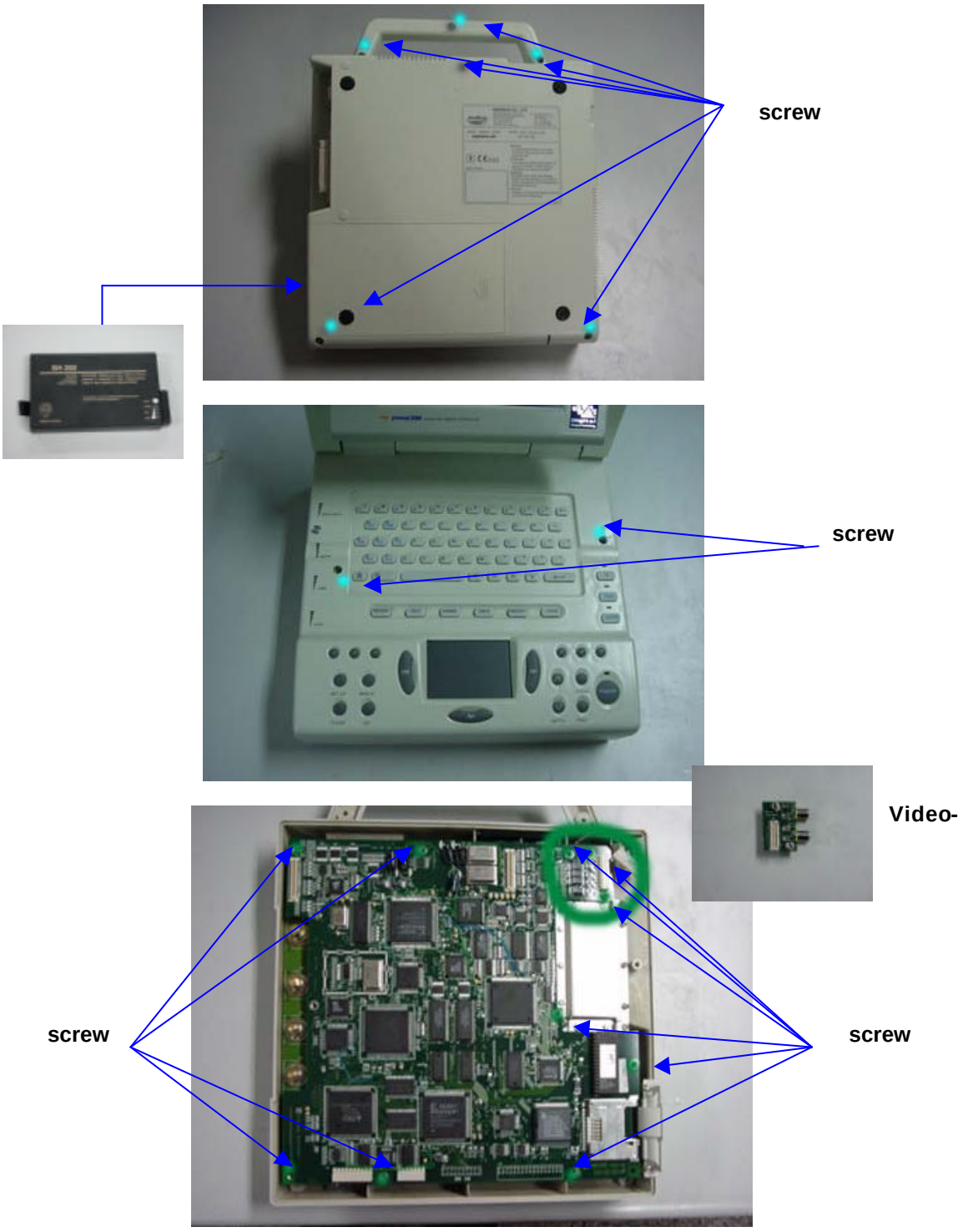


Figure 1.5 Removing the Video-output B/D from DSC B/D

1) Remove battery.
2) When remove 2 screw on the cover body bottom, upper body cover is disconnected.
3) When remove 2 screw on the cover body front, upper body cover is disconnected.
4) Remove 11 screw on the DSC BOARD and Disconnect Video-output B/D.

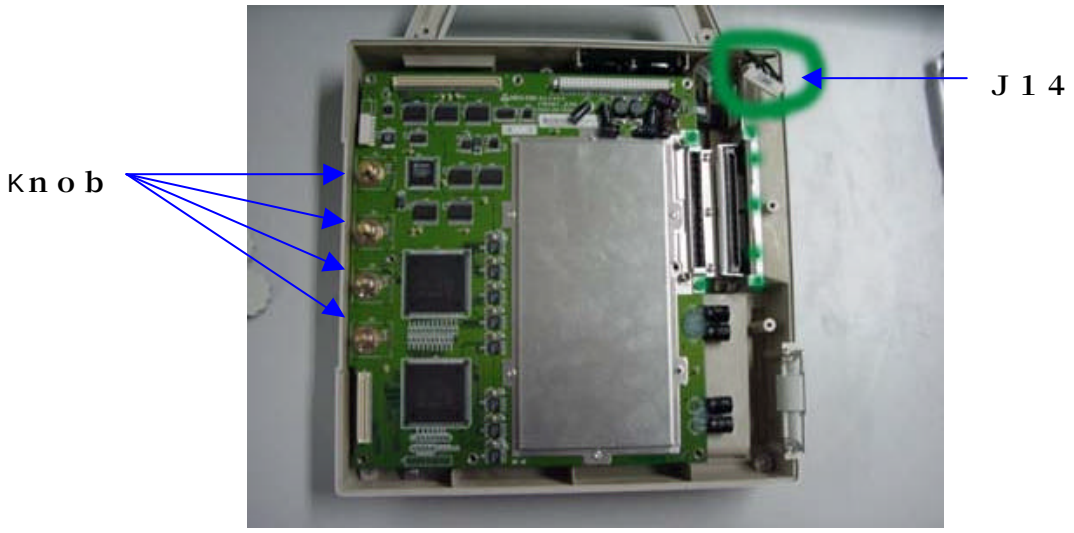


Figure 1.5.1 Removing the Video-output B/D from DSC B/D

5) Remove Knob.
6) Disconnect J14 (9-pin) connector.

1.4.2 Front End Board Replacement Method

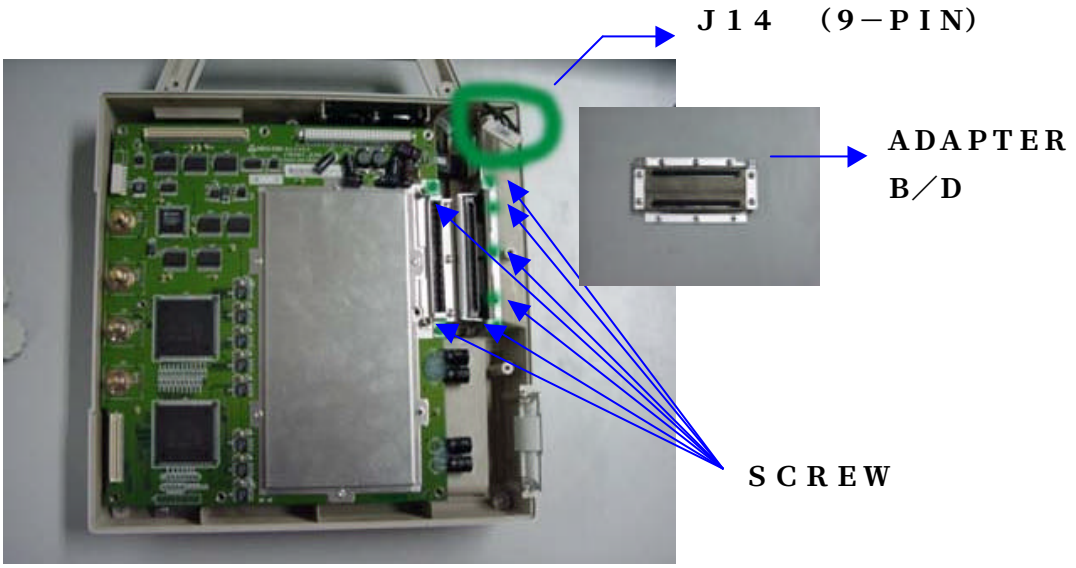
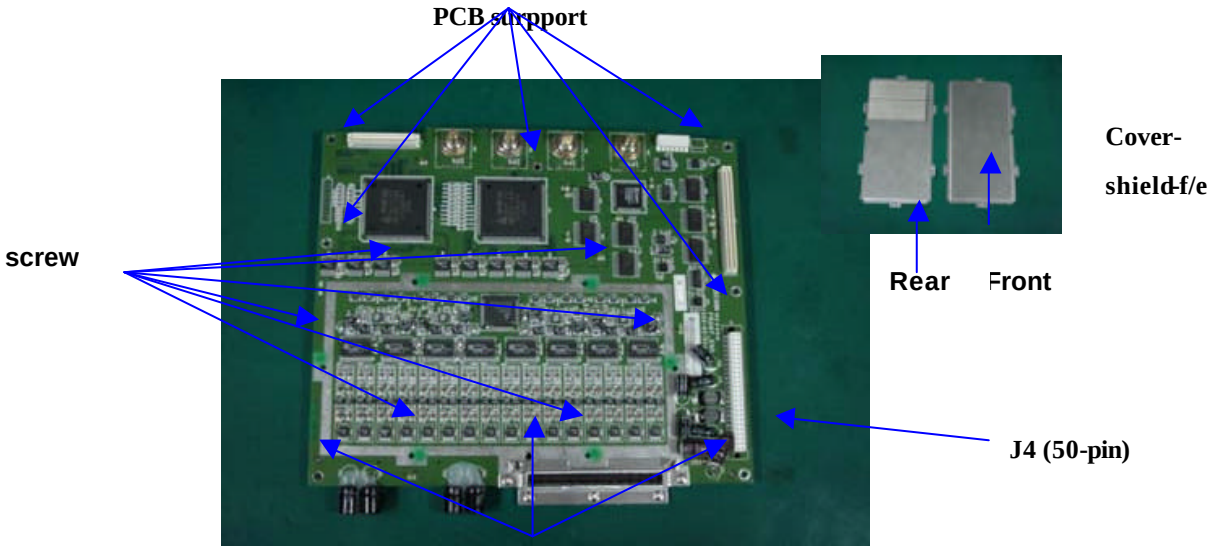


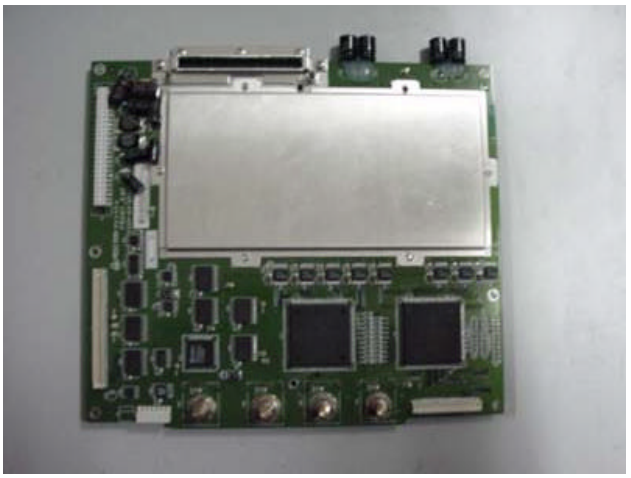
Figure 1.5.2 Removing the Adapter B/D from the Frend End B/D

1) For disconnecting, ADAPTER B/D, to remove 6 screw by "+" screwdriver.
2) For disconnecting, user pulled ADAPTER B/D.

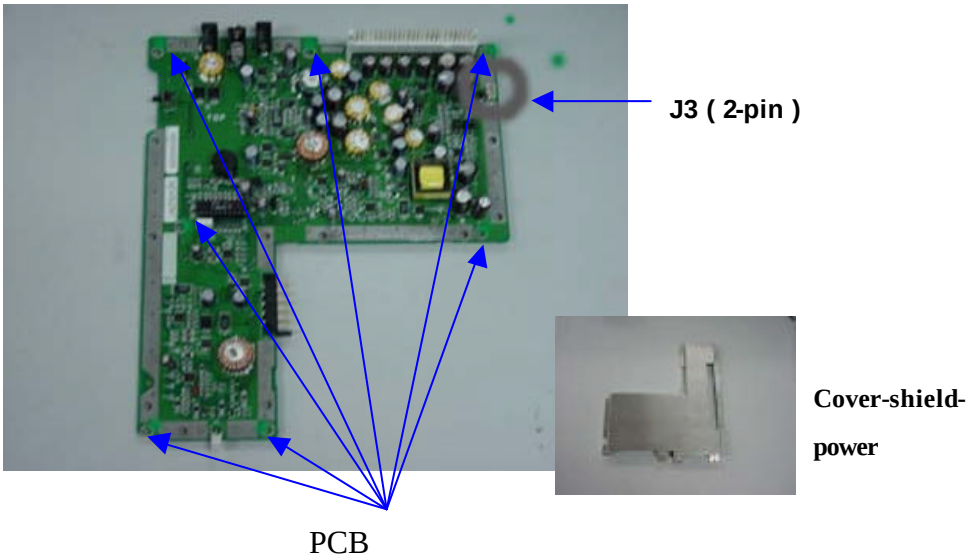


PCB support

3) Remove 8 PCB support on the F/E board.
4) Disconnect the connector which coupled with J4(50-pin) on F/E board and Power board.
5) Disconnect cover-shield-f/e.
6) Replace F/E B/D.



1.4.3 Power Board Replacement Method



1) Remove J3 (2-pin) on the POWER board.
2) Remove 7 PCB support.
3) After remove 13 screw, disconnect cover-shield-power.
4) Replace Power board.

2. Parts List

2.1 Cover Body Bottom Assy Exp.

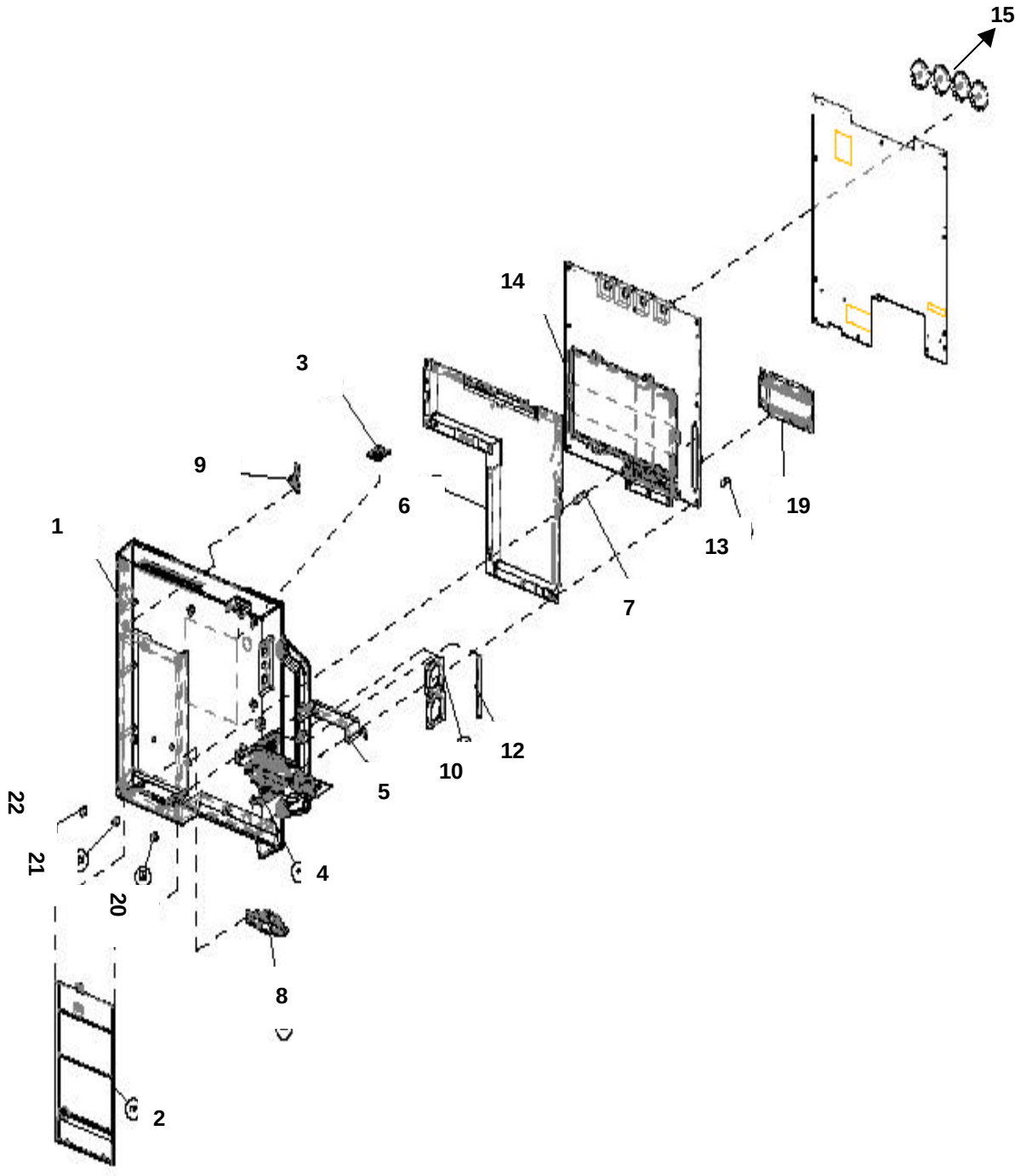


Table 2.1 *Cover Body Bottom Assy Exp.*

No.	Part No.	Description
1	215-M-108	COVER BODY BOTTOM
2	215-M179	COVER-BATTERY-Mysono201
3	262-M-001	KEY-S/W-POWER-Mysono201
4	BD-333-SPC	Mysono201 SPC B/D
5	215-P-205	COVER-SHIELD-SPC-Mysono201
6	AY-333-POWER	Mysono201 201 POWER ASSY
7	EL-HEX3*5	M3*20 SPACER
8		CAP-SMART-MEDISA-Mysono201
9	269-M-040	CAP-PRISM-LED2-Mysono201
10	AY-FAN-333-BACK	Mysono201 FAN ASSY
11	AY-FAN-333-BACK	Mysono201 FAN ASSY
12	313-T-046	CUSHION FANL
13	EL-HEXN3*5	M3*10 SPACER
14	BD-000-F/E	Mysono201 F/E B/D
15	267-M-039	KNOB-ENCORDER-Mysono201
16	267-M-039	KNOB-ENCORDER-Mysono201
17	267-M-039	KNOB-ENCORDER-Mysono201
18	267-M-039	KNOB-ENCORDER-Mysono201
19	BD-333-ADAPTA	Mysono201 ADAPTA B/D
20	311-R-149	RUBBER CAP1-Mysono201
21	311-R-152	RUBBER CAP4-Mysono201
22	311-R-153	RUBBER CAP5-Mysono201
23	EL-MS3*6A3A	M3*5 SCREW
24	EL-MS3*6A3AWA	M3*6 SCREW WITH WASHER
25	EL-MS3*6A3A	M3*8 SCREW

2.2 Power Assy Exp.

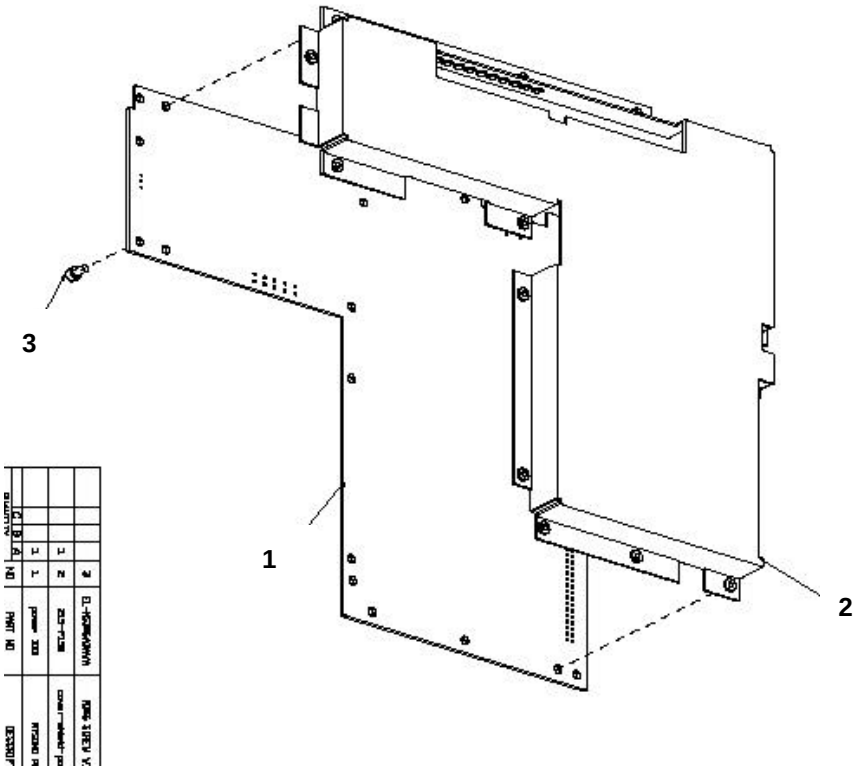


Table 2.2. *POWER ASSY EXP*

No.	Part No.	Description
1	Power 333	Mysono201 Power
2	215-P198	Cover-shield-power-Mysono201
3	EL-MS3*6A3AWA	M3*6 screw with washer

2.3 AY_FE_BOARD_EXP

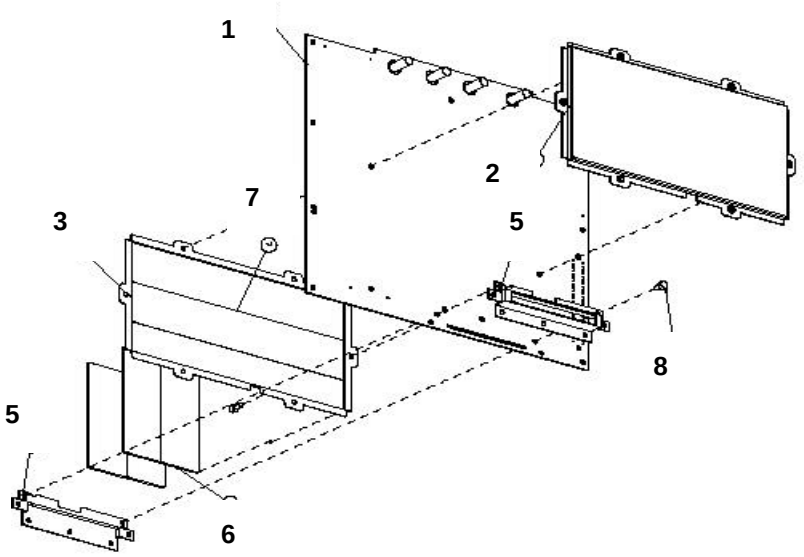


Table 2.3 AY_FE_BOARD_EXP

No.	Part No.	Description
1	BD-333-FE	Board f/e Mysono201
2	215-P-182	Cover-shield-f/e1-Mysono201
3	215-P-183	Cover shield f/e2
4	215-P-203	Cover-shield-f/e3-Mysono
5	215-P-204	Cover-shield-f/e4-Mysono
6	312-Z-029	Gasket F/E
7	323-T-006	Insulator F/E
8	EL-MS3*5A3A	M3*5 Screw

2.4 Adapter B/D Exp.

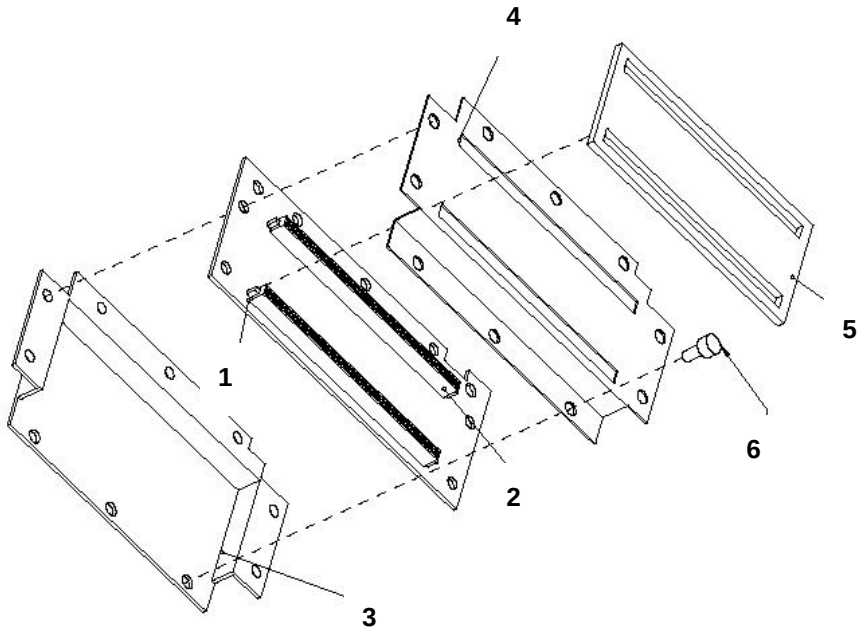


Table.2.4 ADAPTER B/D EXP

No.	Part No.	Description
1	PCB-333-ADAP-0A	Adapter board Mysono201
2		Berg 50*2 female
3	215-P-206A	Cover shield adapt bd1 Mysono201
4	215-P-207	Cover shield adapt bd2 Mysono201
5	312-Z-028	Gasket adapt board Mysono201
6	EL-MS3*4A3A	M3*4 Screw

2.5 Cover Assy Body Top Mysono201 Exp.

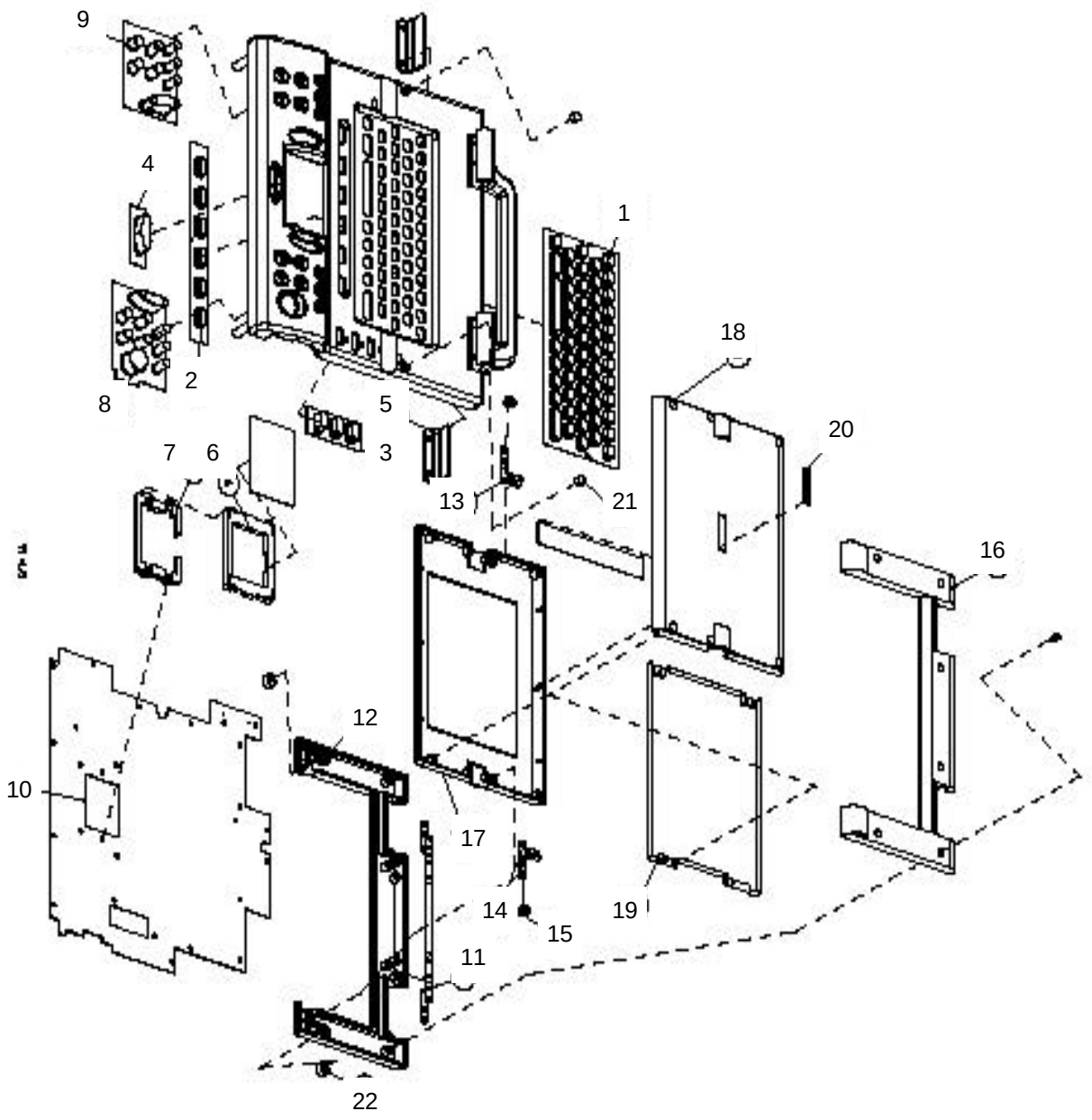


Table.2.5 Cover Assy Body Top Mysono201 Exp.

No.	Part No.	Description
1	311-R-140	KEY S/W RUBBER 1 Mysono201
2	311-R-141	KEY S/W RUBBER 2 Mysono201
3	311-R-142	KEY S/W RUBBER 3 Mysono201
4	311-R-145	KEY S/W RUBBER 6 Mysono201
5	215-M-184	COVER BODY TOP SUB Mysono201
6	213-M-074	CASE LOWER GRID POINT
7	213-M-121	CASE SUPPORT GLIDE/P
8	311-R-143	KEY S/W RUBBER 4 Mysono201
9	311-R-144	KEY S/W RUBBER 5 Mysono201
10	PCB-333-KM-DA	KEY METRIC BOARD Mysono201
11	257-L-011	HINGE TORQUE C Mysono201
12	257-M-186	COVER TOP ARM Mysono201
13	257-L-012	HINGE TORQUE L Mysono201
14	257-L-013	HINGE TORQUE R Mysono201
15	246-M-010	BUSHING TORQUE L/R
16	215-M-185	COVER BOOTOM ARM Mysono201
17	215-M-188	COVER LCD UPPER Mysono201
18	215-M-187	COVER LCD LOWER Mysono201
19	MNT-LCD/LP064V1	LCD TFT MNT Mysono201
20	228-Z-047	PLATE NAME Mysono201
21	254-Z-001	LOCK LATCH MAGNET LCD Mysono201
22	254-Z-002	LOCK LATCH MAGNET LCD Mysono201
23	323-T-007	INSULATOR LCD BOTTOM
24	EL-MS3*6A3A	M3*6 SCREW
25	EL-MS3*6A3A	M3*8 SCREW
26	EL-WDS3*6A3A	3*6 SCREW

2.6 SPC Board Assy Exp.

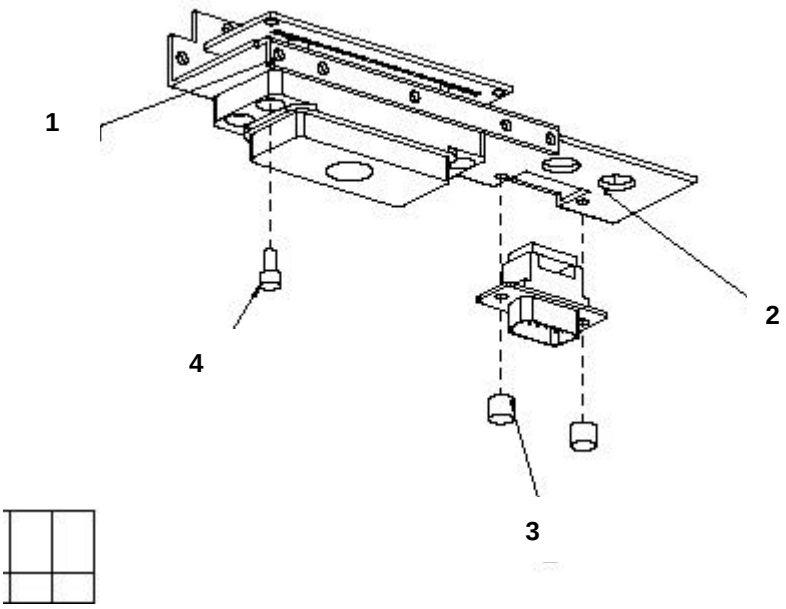


Table.2.6 SPC Board Assy Exp.

No.	Part No.	Description
1	BD 333 SPC	Board spc Mysono201
2	235-P-132	Bracket-connector-Mysono201
3	EL-HEX3*5	M3*5 Spacer
4	EL-MS3*6A3A	M3*6 Screw

1.Specification

1.1 Technical Specification

Physical Dimensions	Width: 255 mm Height: 300 mm Depth: 90 mm Weight: less than 4.0kg
Imaging modes	2D real-time Dual 2D real-time 2D/M-mode M-Mode
Gray Scale	Internal 64 levels, External 256 levels
Channels	16 transmit channels
Focusing	Dynamic transmit focusing, maximum of four points (one point selectable) Digital dynamic receive focusing (continuous)
Probes	Curved Linear Array C2-5/60BD(CLA3.5MHz/60R/60D) C4-7BD(CLA5.0MHz/40R/60D) EC4-9/13CD(CLA6.5MHz/13R/120D) Linear Array L4-7CD(LA5.0MHz/65mm) L5-9CD(LA7.5MHz/40mm) L5-9/60CD(LA7.5MHz/60mm) **Reserved Probes** C4-9 / 10ED (Reserved) C5-8BD (Reserved) VE5-8ED (Reserved) L2-5 / 120CD (Reserved) L2-5 / 150CD (Reserved) L2-5 / 170CD (Reserved) LV4-7AD (Reserved) LV5-9AD (Reserved)
Probe connection	1 probe connector
Monitor	6.4 inch LCD monitor
Peripherals	B/W Printer VCR

	Non-Interlaced B / W Monitor VGA Monitor VHS Monitor HMD
Image Storage	Cine memory (maximum 32 frames) Image Storage (maximum 50 frames)
Application	Fetal, Abdominal, Pediatric, Small organ, Intra-vascular, Peripheral-vascular, Muscular-skeletal, Cardiac, Trans-rectal, Trans-vaginal
Calculation and Quantification	Measurement of various parameters Obstetrical analysis: Standard gestational age tables: BPD, HC, FL, AC, AD, CRL, GS. 6 equations for fetal weight (Osaka University, Merz, Shepard, Hadlock, Tokyo University 1, and Tokyo University 2 method) User-created tables Cardiac analysis: LV, AV, and MV, Heart rate
Signal processing (Pre-processing)	Near, Far, Overall Gain control Dynamic aperture Dynamic apodization Dynamic range control (adjustable) M-mode sweep speed control Frame average Gamma-scale windowing Image orientation (left/right and up/down) White on black
Measurement	Touch pad control of multiple calipers B-mode: Distance, circumference, area, ellipse, volume. M-mode: Velocity, time, slope

Accessories	Coupling gel Power cord Power adaptor Battery (Option) RCA Jack Video output cable Carrying case Operator's manual Smart Media (Option) (Reserved)
Pressure Limits	Operating: 700hPa to 1060hPa Transmit & Storage: 700hPa to 1060hPa
Humidity Limits	Operating: 30% to 75% Transmit & Storage: 20% to 90%
Temperature Limits	Operating: 10 ^{O}C ~ 35 ^{O}C (recommended: 17 ^{O}C ~ 23 ^{O}C) Transmit & Storage: -25 ^{O}C ~ 60 ^{O}C
Electrical	Power adaptor Input: 100-240VAC, 1A, 50/60Hz Power adaptor Output: DC15V, 4A System Input: DC15V, 4A
Battery	Run-Time: Approx. 1.5 hour Recharge Time (System On): Approx. 5 hour Recharge Time (System Off): Approx. 3 hour
LED display	System On without battery: No color During recharge: Orange Recharge completed: Yellow System On without adaptor: Red

1.2 Safety Standard

- **Classification:**

  Class I equipment with Type BF applied parts

  Ordinary Equipment

  Non-AP/APG

- **Electromechanical safety standards met:**

  CSA C22.2 No.601.1, Canadian Standards Association, Medical Electrical Equipment

  EN60601-1, Second Edition, including Amendments 1 and 2, European Norm, Medical Electrical Equipment

EN60601-1-2, First Edition, European Norm, Collateral Standard, Electromagnetic Compatibility

IEC61157: 1992, International Electrotechnical Commission, Requirements for the declaration of the acoustic output of medical diagnostic ultrasonic equipment

UL 2601-1, Underwriters Laboratories, Medical Electrical Equipment

1.3 Range of measurement and accuracy

1.3.1 B mode range and accuracy

Measurement Type	Range	Accuracy (Whichever is greater)
Axial Distance	1 - 250 mm	+/- 2% or +/- 2 mm
Lateral Distance	1 - 250 mm	+/- 2% or +/- 2 mm
Diagonal Distance	1 - 250 mm	+/- 2% or +/- 2 mm
Area	1 - 10,000 mm^2	+/- 4% or 25mm^2
Circumstance	3 - 1,000 mm	+/- 3% or +/- 5 mm

Note:

The accuracy's are using following equations:

Distance error (2% or 2mm) = Image Pixel error (1% or 1mm) + Hardware error (1% or 1mm)

Area error (4%)= Distance 1 x Distance 2

Circumference error (3% or 5mm)= Distance error (2% or 2mm) + Calculation precision (1% or 3mm)

Measurement accuracy is constrained by the cursor placement capability limit in additional to the specifications in the above table

1.3.2 M mode range and accuracy

Measurement Type	Range	Accuracy (Whichever is greater)
Depth	1 - 250 mm	+/- 2% or +/- 2 mm
Time	0.1 - 10.2 sec	+/- 2% or 0.2 sec
Slope	1 - 10,000 mm /sec	+/- 4 %

Note:

The accuracy's are using following equations:

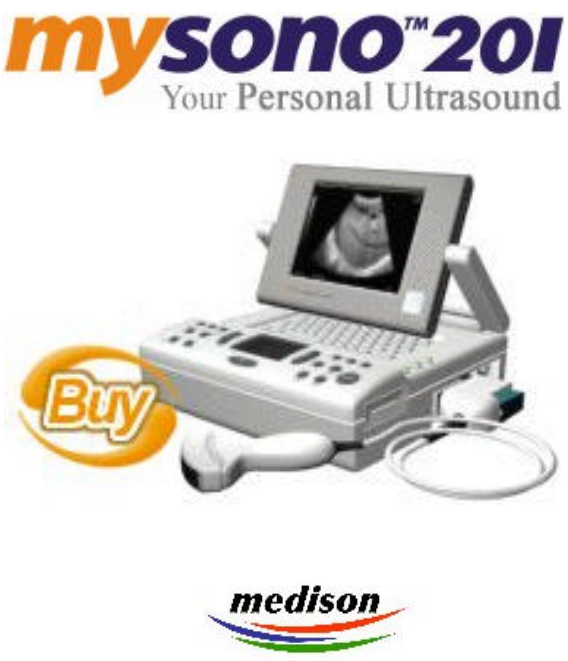
Distance error (2% or 2mm) = Image Pixel error (1% or 1mm) + Hardware error (1% or 1mm)

Time error (2% or 0.2 sec)= Image Pixel error (1% or 0.1 sec) + Hardware error (1% or 0.1 sec)

Velocity error (4%)= Distance / Time

Measurement accuracy is constrained by the cursor placement capability limit in additional to the specifications in the above table

MYSONO201 COMPATIBILITY MATRIX



REVISION STATUS	REV
INITIAL RELEASE	001
Correcting probe information (2000.12.07)	002
DC No : 01-201-001 DSC B/D revision-up to 1A (2001.01.26)	003
DC No : 00-201-010 Power circuit revision-up to 01 (2000.12.26)	004
DC No : 01-201-004 Power circuit revision-up to 02 (2001.02.15)	005

DOCUMENT NUMBER
MSF-QA-801-CM201

APPROVALS	
Originator Y.J.CHOI	Manager S.H.KOH

Please, refer to HOMEPAGE for details: HTTP://WWW.MYSONO.COM

MYSONO201 COMPATIBILITY MATRIX

COMPANY CONFIDENTIAL

Classification	NAME	PART NAME	Rev	HARDWARE COMMENTS	Initial applied S/N of System	S/W VER. 1.00.00	1.00.01	1.00.02	1.01.00H	(VET) 1.01.00V
BOARD	ADAPTER	BD-333-ADAPTER	0A	Initial release(2000.11.11)						
BOARD	DSC	BD-333-DSC	0A	Initial release(2000.11.11)						
			1A	DC No:01-201-002 (2001.01.26)						
				A/W change related to EMI, stability, VGA load						
BOARD	FRONT END	BD-333-F/E	F	Initial release(2000.11.11)						
			0A	DC No: (2000.11.25)						
				Official product for release(Sale)						
			0B	DC No: 00-201-005(2000.12.06)						
				Stablilize TX pulse and delete pull down resistor						
BOARD	KEY MATRIX	BD-333-KEY/M	0A	Initial release(2000.11.11)						
BOARD	POWER	AY-333-POWER	00	Initial release(2000.11.11)						
			01	DC No: 00-201-010(2000.12.26)						
				Correct noise and assembly problem						
			02	DC No: 01-201-004(2001.02.15)						
				Allowable current limit increased (R65,87:10->4.7)						
BOARD	SPC	BD-333-SPC	1A	Initial release(2000.11.11)						

COMPANY CONFIDENTIAL

Classification	NAME	PART NAME	Rev	HARDWARE COMMENTS	Initial applied S/N of System	S/W VER. 1.00.00	1.00.01	1.00.02	1.01.00H	(VET) 1.01.00V
EXT	POWER ADAPTER	AY-333-ADAPTER	0A	Initial release(2000.11.11)						
EXT	LI-ION BATTERY	BT-10.8V-4.8A		Initial release(2000.11.11) SAEHAN BATTERY SH-202						
EXT	LCD	MNT-LCD-LP064V1	0A	Initial release(2000.11.11)						
EXT	SMART MEDIA	OPT-333-S/M (PC-FLASH/PATH)	1A	Initial release(2000.11.11) Flash Disk(2M, 4M, 8M, 16M)	RESERVED					
EXT	BAG	213-Z-125A	00	Initial release(2000.11.11)						
EXT	GLIDE POINT	351-C-003A	00	Initial release(2000.11.11)						

COMPANY CONFIDENTIAL

Classification	NAME	Biopsy Kit	REV	Application (H) : For Human, (V) : For Veterinary	Probe Image	S/W VER. 1.00.00	1.00.01	1.00.02	1.01.00H	(VET) 1.01.00V
PROBE	L4-7CD	BPL-50/65		(H) OB, Abdomen, Pediatric						
	PB-MYL4-7CD			(V) Equine tendon, Bovine back fat, Small ani abdomen						
	L5-9CD	BPL-75		(H) Breast/Thyroid/Testes, C Artery, Noenatal, PV						
	PB-MYL5-9CD			(V) Equine tendon, Bovine back fat, Small ani abdomen						
	L5-9/60CD	BPL-50/65		(H) Breast/Thyroid/Neck/Testes, C Artery, Pediatric						
	PB-MYL5-9/60CD			(V) Equine tendon, Bovine back fat, Small ani abdomen						
	L2-5/120CD									
	PB-MYL2-5/120CD			(V) Porchine pregnancy detection, Abdomen						
	L2-5/150CD									
	PB-MYL2-5/150CD			(V) Porchine back fat and Lean percent						
	L2-5/170CD									
	PB-MYL2-5/170CD			(V) Bovine back fat and marbling score detection						
	LV4-7AD									
	PB-MYLV4-7AD			(V) Large animal pregnancy detection and OB/GYN						
	LV5-9AD									
	PB-MYLV5-9AD			(V) Large animal pregnancy detection and OB/GYN						
	C5-8BD									
	PB-MYC5-8BD			(V) Small animal abdomen						
	C2-5/60BD	BPC-35		(H) OB, GYN, Third Trimester OB, Abdomen						
	PB-MYC2-5/60BD	reserved		(V) Large animal abdomen						
	C4-7BD	BPC-50		(H) OB, GYN, Abdomen, Breast/Thyoid/Testes, Ped						
	PB-MYC4-7BD			(V) Small animal abdomen						
	EC4-9/13CD	BPC-65-E/C		(H) OB, GYN, Third Trimester OB, Abdomen						
	PB-MYEC4-9/13CD									
	C4-9/10ED									
	PB-MYC4-9/10ED			(V) Small animal cardiac and Abdomen						
	VE5-8BD									
	PB-MYVE5-8BD			(V) Large animal OPU						

COMPANY CONFIDENTIAL

Classification	Version	Major Change Description		Initial applied S/N of System	S/W VER. 1.00.00	1.00.01	1.00.02	1.01.00H	(VET) 1.01.00V
PERIPHERAL	B/W PRINTER	SONY 890 MD	OPT-PRT-SONY						
		Mitubish P91E	OPT-PRT-P91E						
		Mitubish P91W	OPT-PRT-P91W						
		Mitubish M90U	OPT-PRT-MITS-1						
		Mitubish M90E	OPT-PRT-MITS-2						
	HMD	HMD-I/GASSES	Virtual I glasses						
			Don't use it in PAL system						
	VCR	VCR	VCR RECORDING AVAILABLE						
	EXTERNAL MONITOR	VGA MONITOR	*						
		B/W MONITOR	*						

				MANUAL REV.
S/W	1.00.00 (2000.11.10)	Initial release for sale		MAN-mysono201-E(D)10000
	1.00.01 (2000.11.15)	Bugs patched		MAN-mysono201-E(D)10000
		CHG key in M mode, LMP reset in ID, Message of Setup store and freeze,		
	1.00.02 (2000.11.18)	Bug patched		MAN-mysono201-E(D)10000
		An error in Doing autorun after deleting a stored image		
	1.01.00 (2000.01.08)	Bugs patched		MAN-mysono201-E(D)10100
		Errors : NTSC/PAL settiing, Saving changed Depth in setup mode		
	1.01.00 only for VET (2000.01.08)	Initial release for VET version		MAN-mysono201V-E(D)10100
		Patient ID, GA table, Bodymark, Cardiac measurement are different from Human use		